# Monolithic Integration of Micron-scale Piezoelectric Materials with CMOS for Biomedical Applications

C. Shi, T. Costa, J. Elloian, and K. L. Shepard
Bioelectronics Systems Laboratory, Columbia University, New York, USA, email: cs3184@columbia.edu

***Abstract*— We present the development of micro-fabrication techniques achieving the monolithic integration of micron-scale piezoelectric ultrasonic transducers in both polyvinylidene difluoride (PVDF) and lead zirconate titanate (PZT) with complementary metal–oxide–semiconductor (CMOS) integrated circuits (ICs). PVDF-CMOS integration is driven by applications in energy harvesting and data telemetry for medical implants, while PZT-CMOS integration is applied to high-resolution two-dimensional (2D) ultrasound imaging. Both of these applications benefit from reduced parasitic capacitances and higher levels of integration possible with monolithic CMOS integration. Characterization results of micro-fabricated devices reveal the preservation of the piezoelectric properties of PVDF and PZT and transducer functionality with co-designed CMOS ICs.**

## I. Introduction

Piezoelectric materials, including PVDF and PZT, have unique properties that allow them to convert electrical energy into mechanical energy and, for that reason, have been utilized for decades as ultrasound transducers in medical imaging. These same materials can also be used to harvest energy from ultrasound waves to power implanted devices and transmit data by modulating information onto an ultrasound carrier. Nearly all of the existing implantable devices and ultrasound imaging systems suffer from large form factors because they primarily package functional piezoelectric transducers and the associated electronics discretely [1, 2]. Reducing transducer size to create piezoelectric ultrasonic transducers as small as ~100 μm can reduce displaced volume for implantable devices and enable superior spatial resolution for ultrasound imaging systems. To effectively interface with these micron-scale piezoelectric transducers, direct integration with CMOS ICs is critical both to achieve the requisite interconnect density and to reduce parasitic capacitances which can divide-down signal levels due to the low intrinsic capacitance of the micron-scale transducers. The far-back-end-of-the-line integration approach pursued here allows these devices to be viewed as "More than Moore" enhancements to CMOS. Here, we report approaches to monolithically integrate micron-scale PVDF and PZT piezoelectric transducers with co-designed CMOS ICs (in a standard 0.18 μm 1.8V/5V CMOS technology) for implantable applications and for imaging applications.

## II. Fabrication Flow

PVDF is a flexible and biocompatible piezoelectric material, but it cannot tolerate temperatures greater than 80 °C due to a low Curie point. In comparison, PZT is a rigid piezoelectric ceramic material with superior electromechanical properties that can tolerate temperatures as high as 150 °C. Process flows for integrating these materials must be tuned to these temperature requirements.

### *A. Piezoelectric transducer integration with CMOS*

In the Van Dyke electrical model for a piezoelectric transducer (**Fig. 1a)**, $C_0$ and $R_0$ represent the parallel plate capacitor and electrical losses of the transducer and the series $R_1$, $L_1$ and $C_1$ capture the mechanical behavior. The circuits interfacing with the PVDF transducers (**Fig. 1b**) for energy harvesting and with the PZT transducers (**Fig. 1c**) for ultrasound imaging greatly benefit from reduced interconnection parasitic capacitances ($C_p$) of less than 200 fF compared to those with discrete implementation (usually on the order of several pF), making impedance matching requirements for maximum power transfer between the PVDF transducers and the half-wave rectifier (**Fig. 1b**) easier and improving the transmit (TX) driver performance with the PZT transducers (**Fig. 1c)**.

Fabrication in both cases starts with bulk PVDF and PZT films, which are mechanically and electrically connected to the CMOS ICs, followed by a subtractive fabrication process to obtain the desired micron-scale pillar structures. The co-designed CMOS ICs for PVDF integration (**Fig. 2**) and for PZT integration (**Fig. 3**) both provide signal and ground terminals on the top-level metal to be connected to the corresponding piezoelectric transducers. Both ICs are initially planarized by etching the polyimide passivation. PVDF and PZT integration then follow different fabrication flows specific to their particular properties.

### *B. Integration of PVDF with CMOS*

The co-designed CMOS chip, contained in a 5 mm × 5 mm die (**Fig. 2a**) with 13 replicas (**Fig. 2b**), has a 150 μm × 95 μm signal pad and a 150 μm × 20 μm ground pad for transducer connections (**Fig. 2c)**. A poled 33-μm PVDF film is used, delivering a mechanical resonance frequency of ~34 MHz but usable over a wide frequency range due to its inherently low quality factor. This PVDF film has its surface treated with $O_2$ plasma to enhance the interfacial adhesion [3]. A 1.6-μm-thick SU-8 2002 adhesive layer is then spun onto the die, bonded to a carrier substrate (**Fig. 4a**). While this introduces a series capacitance of 250 fF (negligible compared to a $C_0$ of 22.5 fF for the PVDF), the more preferable anisotropic conductive adhesives cannot be applied because they typically require curing temperatures above 100 °C. The substrate is then flipped over and gently placed on the pre-treated PVDF film, baked at 70 °C for 30 minutes, and flipped back to be UV cured (**Fig. 4b**). The now-exposed PVDF top surface is also treated with $O_2$ plasma and a ~10-μm layer of AZ-4620 photoresist (PR) is spun, followed by a baking step at 70 °C for 80 minutes. The same spinning-and-baking process is repeated two more times to create a ~30-μm-thick PR layer. Standard UV

photolithography is applied to create PR patterns, used as etch masks, above the signal pads (**Fig. 2c**, **Fig. 4c**). RIE etching of the PVDF and the underlying SU-8 layer is used to define the micron-scale PVDF pillars (**Fig. 4d, Fig. 5a**) with the bottom terminals connected to the signal pads. Photolithography with a ~6-µm layer of AZ-4620 is performed to cover the entire die except the active chip area (**Fig. 4e**). DC sputtering is used to deposit ~1.2-µm of Cu onto the die. Finally, the Cu over the PR layer is removed with a lift-off process, leaving Cu connection between the top terminals of the PVDF pillars and the ground pads (**Fig. 2c**, **Fig. 4f**, **Fig. 5b**). The final PVDF transducers (**Fig. 6**) maintain their longitudinal charge sensitivity (d33) of ~19 pC/N, as measured with a PM300 d33 meter (Piezotest).

### *C. Integration of PZT with CMOS*

The CMOS IC for PZT integration (**Fig. 3a**) features a 2D array of 26 × 26 transmit/receive (TX/RX) channels. Each channel includes a 75 µm × 75 µm signal pad for connection with the PZT transducers (**Fig. 3b)**. The PZT material used here has a thickness of 267 µm, which produces a resonance around 8 MHz. The PZT fabrication steps are illustrated in **Fig. 7**, where the PZT transducer pillars are patterned using a mechanical dicing process [4, 5], which provides a much faster etch rate than RIE for the PZT thickness used in this work. The PZT bulk material is obtained as a 7.24 cm × 7.24 cm sheet with 50 nm of Ni on both sides of the film. The Ni is etched away by dipping the sheet into ferric chloride for 5 seconds. Next, a 10-nm chrome adhesion layer and a 50-nm gold layer are deposited by electron beam (e-beam) evaporation onto both sides of the PZT sheet (**Fig. 7a**) and patterned by lift-off of AZ-1512 PR (**Fig. 7b**). The bottom pattern matches the signal contacts on the CMOS chip (**Fig. 3b**). The PZT sheet is then diced into 4 mm × 4 mm individual dice using a dicing saw with a blade suitable for PZT ceramics (Z09-SD2000-Y1-90) with a kerf of 50 µm (14000 spindle, 3 mm/s feed speed). The PZT die is then diced from the bottom side to about 20% of its thickness by using the same blade and cutting settings (**Fig. 7c**). This defines the shape of the PZT elements from the bottom, which enables the dicing from the top side to go all the way through the PZT without risking damaging the CMOS chip. The PZT die is attached to the CMOS chip with an anisotropic conductive film (TFA220-8, H&S HighTech) as an adhesive and bonded in a FINEPLACER lambda die bonder (Finetech) with fine alignments, using a force of 150 N at 150 °C for 5 seconds (**Fig. 7c**). The PZT is then diced from the top to a depth of 90% of its thickness, which leaves the elements completely free-standing and fully etched (**Fig. 7d**). Microscope images of the 2D array of PZT pillars are shown in **Fig. 8a-c**, while a SEM image of the PZT pillars is shown in **Fig. 8d**. To provide mechanical stability to the array of PZT pillars, the kerfs are filled with the Epo-Tek 301-2 epoxy (Epoxy Technology), as shown in **Fig. 7e**. Finally, the same Cu deposition step, as detailed in Section II.B, is performed on top of the 2D array to implement the common ground connections among all the fabricated micron-scale PZT elements (**Fig. 7f**). In the fully fabricated chips (**Fig. 9**), d33 measurements before and after fabrication show only a 7% loss (398 pC/N for pristine PZT to 370 pC/N for post-fabricated PZT).

## III. Characterization Results

### *A. PVDF integrated on CMOS*

The PVDF transducers were characterized with Raman spectroscopy and atomic force microscope (AFM). The background Raman spectrum due to the IC substrate was subtracted from the absorbance measurements to obtain the PVDF spectrum. The post-fabricated PVDF shows almost the same Raman spectrum as the pristine one with characteristic peaks at 511 $cm^{-1}$, 840 $cm^{-1}$ and 1430 $cm^{-1}$ (**Fig. 10**) [6], demonstrating the preservation of piezoelectric properties. Additionally, AFM was used to measure the surface morphology of the fabricated piezoelectric transducers under voltage excitation. **Fig. 11a** shows the roughness of the PVDF top surface to be close to 100 nm in the absence of voltage excitation. 10-V square wave excitation at 1 Hz and 10 Hz, however, resulted in observable mechanical oscillations in the AFM that scanned at 1 Hz (**Fig. 11b**, **Fig. 11c**). The interfacing on-chip half-wave rectifier (**Fig. 1b**) is functional with a 10 MHz, 1.8V peak-to-peak sinusoidal excitation (**Fig. 12)** after going through the PVDF fabrication processes.

### *B. PZT integrated on CMOS*

To test the integration of PZT with CMOS, a fully-fabricated chip was wire-bonded to a custom printed circuit board in the test setup illustrated in **Fig. 13a**. A container was adhered to the board and then filled with deionized water. A HGL-0200 hydrophone connected to a AG-2010 amplifier (Onda) was placed at the center of the PZT array and connected to an oscilloscope to record the ultrasound waves generated by the transducers. The CMOS IC TX drivers (**Fig. 1c**) were configured to generate a 5-V, 8-MHz square wave and the hydrophone successfully recorded the incoming ultrasound waves for increasing distances from the CMOS chip, in steps of 2 mm (**Fig. 13b**). From the obtained data, the speed of sound in water was measured to be 1530 m/s, which is close to the reference value around 1540 m/s. The recorded pressure amplitude decreases with increasing propagation distance, as expected.

## IV. Conclusion

This work reports on the fabrication approaches to monolithically integrate µm-sized PVDF and PZT transducers with CMOS. Different fabrications steps were employed according to the distinct characteristics of PVDF and PZT. Various characterization results show the successful integration for both materials, where the piezoelectric properties of PVDF and PZT as well as the functionality of the interfacing CMOS ICs are retained throughout both fabrication flows with the introduction of limited capacitive interconnect parasitics.


## Acknowledgment

This work was funded by the DARPA ElectRx program.


## References


[1] C. Dagdeviren *et al.*, *Nat. Biomed. Eng.,*1(10), pp. 807-817, 2017.
[2] T. Gang *et al.*, *J. Micromech Microeng* 22(6) p. 065017, 2012.
[3] J. S. Lee, *et al ACS Appl Mater* 1(12), pp. 2902-2908, 2009.
[4] C. Chen *et al.*, *IEEE Symp VLSI*, pp. 1-2. *2016*
[5] J.-S. Park et al., Sens Actuators A Phys, 108(1), pp. 206-211, 2003.
[6] P. Martins *et al*, *Prog. Polym. Sci.,* 39(4), pp. 683-706, 2014.

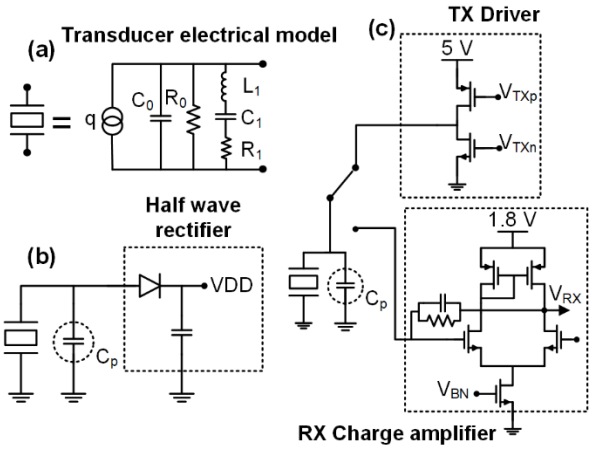


Fig. 1. Simplified schematics of the CMOS circuits that interface with the piezoelectric transducers. (a) electrical model and (b) half-wave rectifier for power harvesting from a PVDF transducer and (c) charge amplifier receiver and transmit driver for PZT-based ultrasound imaging.

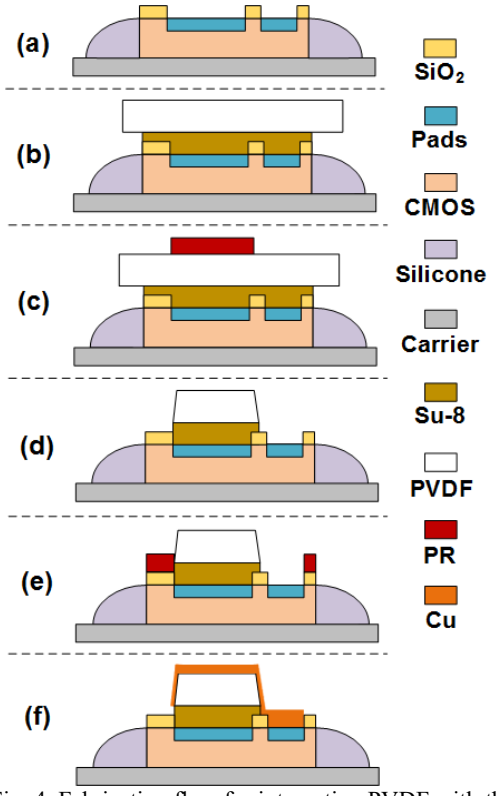


Fig. 4. Fabrication flow for integrating PVDF with the CMOS IC in Fig. 1. (a) Removal of polyimide and bonding of the IC die to a carrier with PMMA and silicone and (b) adhesion of pre-treated PVDF piece and the die with SU-8 and (c) patterning of PVDF areas on top of the chip signal pads and (d) RIE etching to create PVDF pillars and (e) patterning of chip areas and (f) metal deposition and lift-off for ground connection.

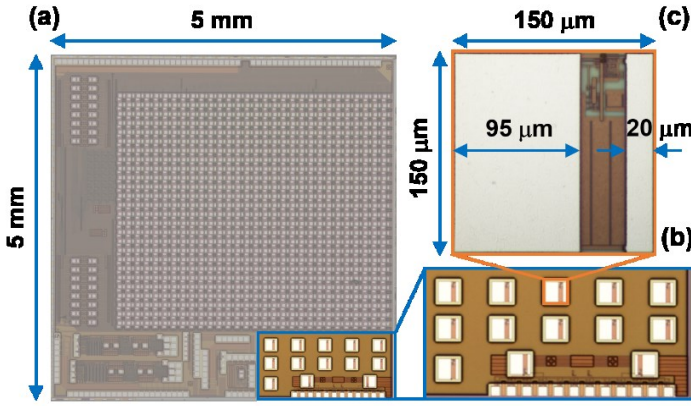


Fig. 2. CMOS IC microphotograph for PVDF integration. (a) Die image and (b) 13 chip replicas contained in one IC and (c) one individual chip.

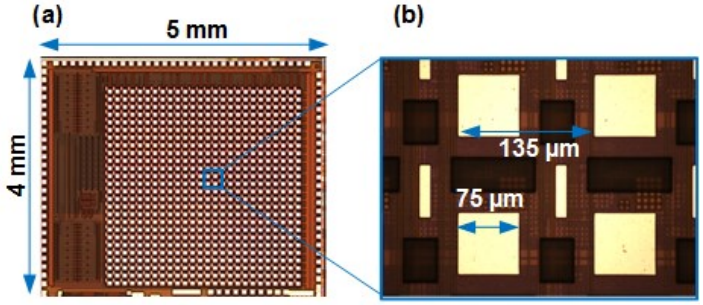


Fig. 3. CMOS IC microphotograph for PZT integration. (a) Die image and (b) transmitter/receiver circuits with the signal pads.

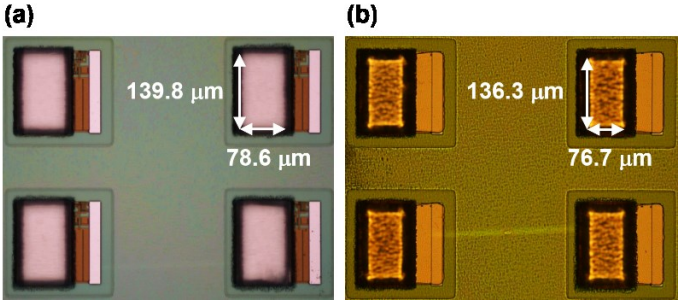


Fig. 5. Microscope photograph of (a) 4 PVDF pillar structures integrated with the chip input pads and (b) 4 fully-integrated PVDF structures with the chips.

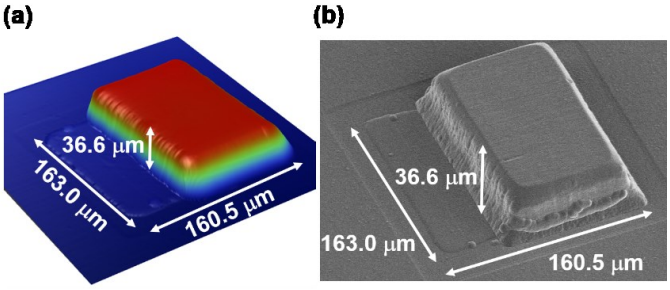


Fig. 6. (a) The profilometer map scan image and (b) the SEM image of one fully-fabricated micron-scale PVDF structure monolithically integrated on-chip.

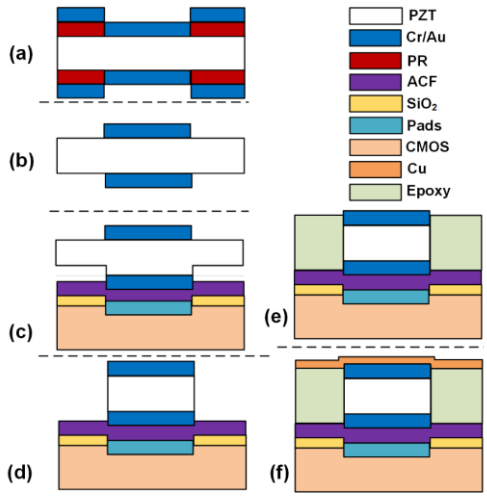


Fig. 7. Fabrication flow for integrating PZT with the CMOS IC in Fig. 2. (a) Patterning of the Cr/Au layer on both sides of the PZT sheet by spin-coating of the PR and the e-beam evaporation and (b) lift-off to define the Cr/Au contacts and (c) PZT diced from the bottom side and adhered to the CMOS IC with ACF and (d) PZT diced from the top side to define the pillar structures and (e) PZT kerfs filled with epoxy and (f) sputtering of Cu for PZT transducer ground connection.

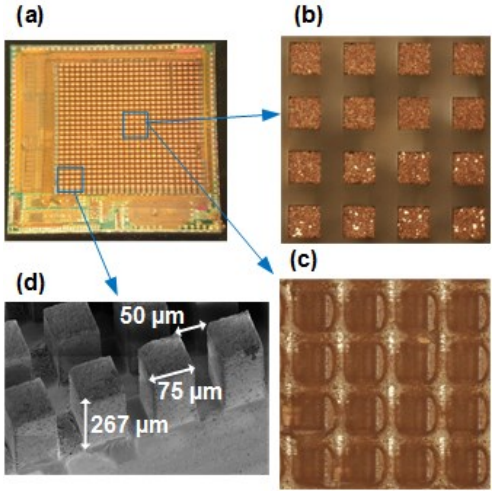


Fig. 8. Microscope photograph of PZT integrated with the CMOS IC chip after top-side dicing. (a) Full chip view and (b) top of the micro-fabricated PZT pillars and (c) surface of the CMOS IC and (d) SEM image of the PZT pillars.

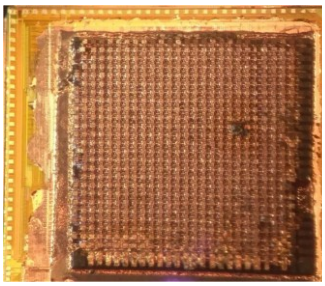

Fig. 9. Microscope photograph of one fully-fabricated CMOS PZT chip.

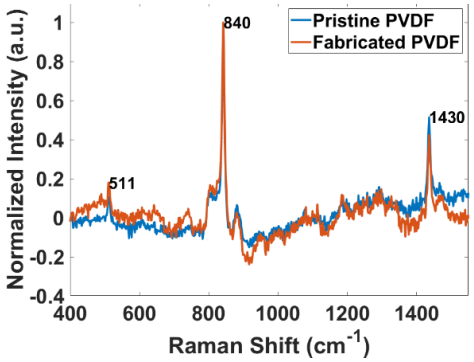


Fig. 10. Raman spectrum of one micro-fabricated PVDF structure in comparison with a pristine PVDF piece.

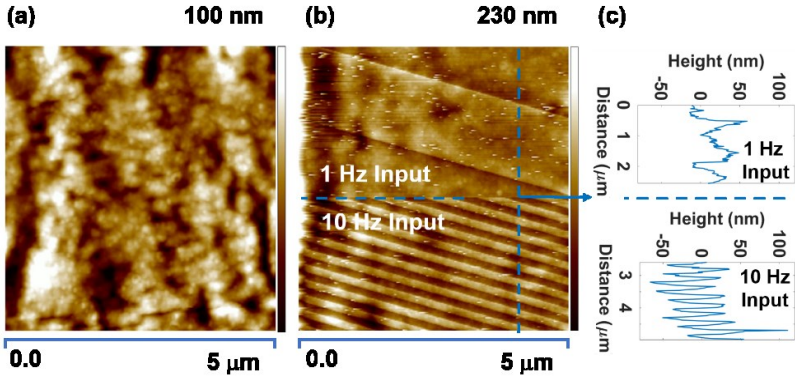


Fig. 11. AFM measurements on one fabricated PVDF structure (a) without voltage excitation and (b) with 1 Hz and 10 Hz 10 V peak-to-peak square wave excitations (c) a height plot along a vertical line on Fig. 11(b).

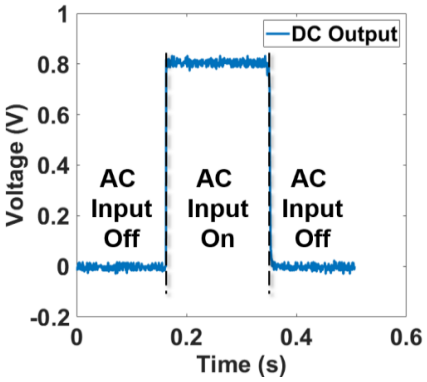


Fig. 12. Output voltage from a post-fabricated on-chip half-wave rectifier.

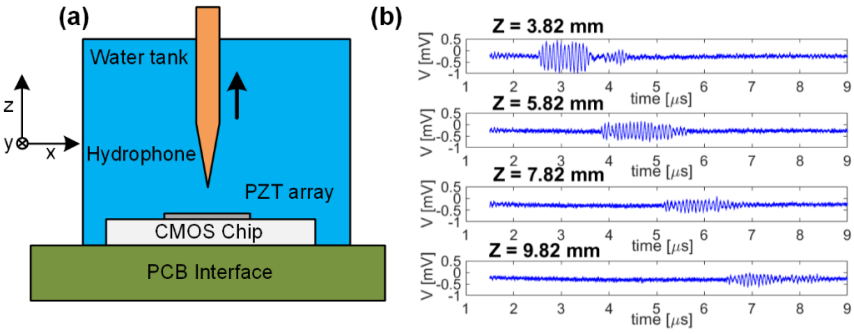


Fig. 13. (a) Measurement setup for characterizing the PZT-integrated CMOS chip and (b) ultrasound measurements with a hydrophone from different distances to the CMOS chip.