Monolithically Integrated CMOS-SMR Oscillator in 65 nm CMOS Using Custom MPW Die-Level Fabrication Process

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***Abstract*— Acoustic resonators, such as thin-film solidly mounted resonators (SMRs) and silicon microelectromechanical systems have been used widely in commercial and research RF communication circuits to implement high-Q oscillators and highly selective filters. Monolithic integration is a promising solution to address the growing demand for such components while continuing the aggressive miniaturization of radios. In this paper, we demonstrate successful monolithic SMR-CMOS co-integration by building a high-Q SMR atop a standard 65-nm CMOS substrate using a custom die-level fabrication process. The approach takes advantage of features in the back-end-of-line to deliver the surface smoothness required for fully supported mechanical resonators, which was not possible using traditional process approaches. This paper marks the first demonstration of SMR integration on 65-nm CMOS. The CMOS die used is more than 400% smaller in area than those in the previous die-level demonstrations of monolithically integrated piezoelectric resonators on CMOS. [2016-0192]**

***Index Terms*— CMOS integrated circuits, acoustic resonators, oscillators, monolithic integrated circuits, SMR.**

I. Introduction

HIGH quality passives are critical to the implementation of filters and oscillators in modern RF and mm-wave communication hardware. Electrical passives, inductors in particular, exhibit large loss factors which limit their utility in implementing stable oscillators and selective low-loss filters with steep transition bands [1]. Acoustic resonators transduce an electrical input signal to the mechanical domain where they perform the filtering operation and convert the signal back to the electrical domain for output. Due to their higher energy storage capability, acoustic passives exhibit significantly lower losses and at least an order of magnitude higher quality factors than their electrical counterparts [2]. As a result, acoustic components enjoy strong adoption in demanding applications such as front-end filters and duplexers where LC filters cannot compete [3]–[5]. Additionally, there is an abundance of research activities in new mechanical resonator topologies and materials specifically targeted for next generation RF systems [6]–[12].

The explosive growth in wireless communications and rapid increase in demand for higher data rates and more communication bandwidth has led to a proliferation of a number of wireless communication standards, each with its dedicated frequency bands. Due to the proximity of such bands, acoustic filters are predominantly used for selecting unwanted interferers/blockers to enable operation of the downstream components in the RF transceiver. In the current state-of-the art, an acoustic BAW/SAW filter is used for each different frequency band [13], [14]. In modern communication handsets, there can be as many as 10 BAW/SAW filters in the front-end [15].

A monolithic integration approach, whereby high quality acoustic passives are built directly atop CMOS circuitry would allow for close integration between acoustic devices and high performance CMOS transistors. This allows increasing levels of integration that can further miniaturize wireless hardware. More importantly, the close interaction between CMOS and acoustic devices, as offered by the integration, can allow new circuit design paradigms whereby the advantages of both components are simultaneously leveraged to gain the best of both worlds [2]. Direct interconnection of CMOS and MEMS acoustic devices allows for optimized co-design of the different components. System impedance levels can be tailored as desired, which is not possible with hybrid interfaces such as wire-bonding and flip-chip, which pose strict and standardized impedance levels [2]. Additionally, CMOS transistors can provide tunability and reconfigurability for the MEMS components. For example, banks of transistors and on-chip capacitors can be used to tune and dynamically configure acoustic resonator structures [16], [17].

To date, there have been some very promising demonstrations of monolithic integration of piezoelectric acoustic resonators on CMOS for applications in RF receiver circuits [18]–[21] and biological sensing [22]–[25]. However, with the exception of [22] and [25] all of these demonstrations

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have been performed on CMOS wafers. Processing full CMOS wafers is cost prohibitive for most researchers. The ability to build acoustic devices atop small dies such as those provided by multi-project wafer (MPW) runs presents a cost effective approach to experiment with the integration of acoustic devices and cutting-edge CMOS circuits.

This work presents an effort to extend previous monolithic integration efforts to small dies and modern processes. The authors present a fully integrated SMR-CMOS oscillator implemented using standard foundry 65 nm CMOS. The integration is performed through a specially designed, custom fabrication flow that allows for fabricating directly on small CMOS dies ($< 2\,\text{mm} \times 2\,\text{mm}$) without requiring the use of full wafers. The flow also takes into account the features of the back-end-of-line (BEOL) which complicate creating a smooth surface for low loss resonators, and modifies the design and process to allow for co-integration without polishing, which is challenging on loose dies. This effort represents more than a 4-fold reduction in die size compared with previous single die demonstrations [22]. The authors demonstrate a small area (511 μm $\times$ 280 μm), monolithically integrated SMR-CMOS oscillator operating in the GHz regime. The resonator is built directly atop the CMOS circuits and marks the first demonstration of SMR integration on a full stack copper/low-K metallization process (65 nm CMOS).

II. SMR Structure and Electrical Model

The device utilized in this work is a piezoelectric thin-film solidly mounted resonator (SMR). SMRs and similar devices (FBARs) are among the most commercially successful acoustic MEMS devices used in front-end filters [3]–[5] and more recently in high-Q oscillators [26]. The SMR structure is comprised of a metal-piezoelectric-metal sandwich. Electrical input to the electrodes sets up a mechanical resonance in the structure through the inverse piezoelectric effect. The resonance can then be sensed electrically via the piezoelectric effect. The mechanical resonance takes place in the longitudinal or thickness axis of the SMR. In this work, zinc oxide (ZnO) is used as the piezoelectric layer and gold (Au) as the electrode material. The resonator is built atop an acoustic Bragg reflector to provide acoustic isolation from the substrate. At this point, it is worth noting that any fabrication performed on the CMOS surface must not damage the underlying CMOS transistor circuitry. Consequently, fabrication operations are limited to a thermal budget below 400°C beyond which the metal interconnect layers degrade [27], [28].

A. Zinc Oxide Piezoelectric Layer

The zinc oxide piezoelectric layer is deposited using RF magnetron sputtering at 150°C, well within the thermal budget of foundry CMOS. High piezoelectric coupling is necessary for achieving high quality, low-loss resonators. In thin film piezoelectrics such as ZnO, piezoelectric coupling is strongly correlated with the degree of crystallinity or internal ordering of the piezoelectric film [29]. To this end, deposition conditions were optimized to produce a well ordered polycrystalline film as characterized through X-ray diffraction (XRD) measurements. The 1.5 μm ZnO layer (targeting a resonance

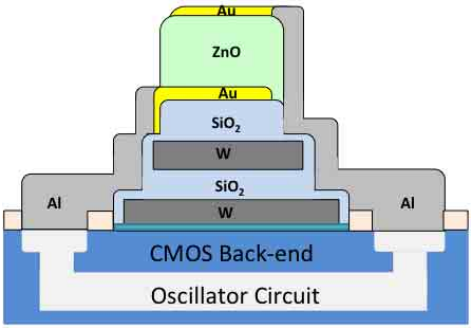


Fig. 1. Proposed SMR cross-section.

around 1.8 GHz) was deposited on 75 nm Au electrodes above a 20 nm titanium (Ti) adhesion layer due to its superior ability to seed well aligned piezoelectric ZnO films when compared with other electrode stacks such as Au/Cr or Al/Cr [29]. Addition of mild heating (150°C) was observed to improve crystallinity of the deposited films. Sputtered films exhibited a full width half maximum (FWHM) value of 0.26° which is comparable to values demonstrated in literature [29].

B. Patterned Reflector and Electrical Contacts

In order to prevent acoustic leakage into the substrate and maintain a high quality factor, the resonator and substrate are decoupled by a two pair silicon dioxide (SiO_2)/tungsten (W) Bragg reflector [30], [31]. At a frequency determined by the thicknesses of the SiO_2 and W layers, the reflector presents a very large reflection coefficient to acoustic waves. This has the effect of decoupling the resonator from the substrate. The reflector layers are deposited through a combination of DC and RF magnetron sputtering. Sputtered tungsten exhibits large residual stress values, therefore sputtering pressure and power were carefully optimized to ensure acceptable stress values that would not cause buckling/cracking of the mirror layers. To prevent delamination of W layers, thin Cr adhesion layers (10 nm) were inserted between the individual W and silicon dioxide SiO_2. Thicknesses of 680 nm and 650 nm were selected for the SiO_2 and W layers respectively to achieve a reflector centered around 2 GHz.

Shown in Fig. 1 is a schematic description of the SMR on CMOS structure. A pyramidal or ziggurat design was adopted for the acoustic reflector, whereby each SiO_2/W pair is slightly wider than the preceding pair. The mirror thickness is on the order of ~ 3 μm with the overall device thickness greater than 4 μm. The pyramidal geometry ensures that the aluminum (Al) metal contacts to the underlying CMOS circuit do not experience any height difference larger than 680*nm* (thickest mirror layer) which is significantly lower than the overall device thickness. This is crucial in reducing the series resistance seen by the resonator to obtain a high electrical quality factor. The top most SiO_2 layer of the reflector blankets the entire reflector stack to avoid electrical shorting between the conductive W layers and gold electrodes.

C. SMR Electrical Model

Initially, 100 μm $\times$ 100 μm, 1.7 GHz-1.8 GHz SMR test devices were fabricated on glass. Following device

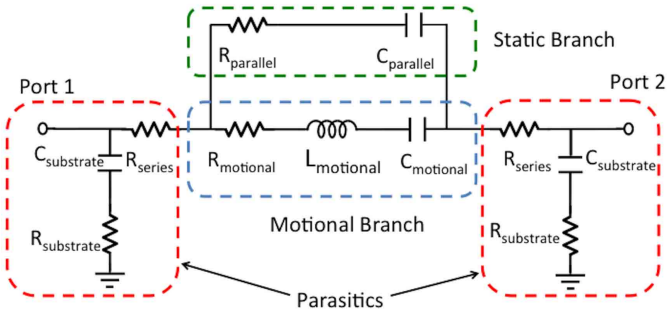


Fig. 2. Modified Butterworth-Van Dyke (mBVD) SMR model including parasitics [32].

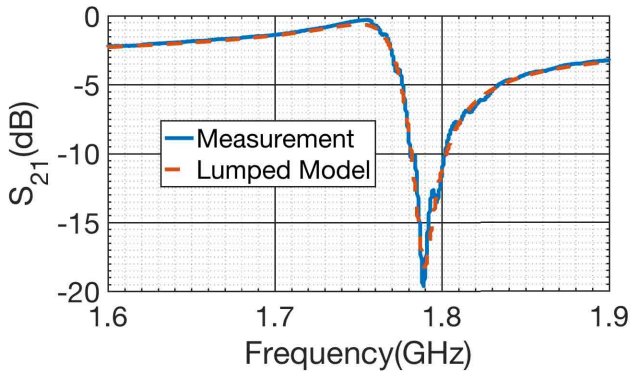


Fig. 3. Fitting of 100 μm × 100 μm glass SMR measurements to lumped model.

fabrication on glass, an electrical model was extracted for use in the subsequent design of a CMOS oscillator integrated circuit (IC). The resonator was characterized using Cascade Microtech GSG RF coplanar probes in a two-port configuration and the the S-parameter response fit to a lumped, modified Butterworth-Van Dyke model (mBVD) [32], [33]. The equivalent mBVD circuit can be seen in Fig. 2 along with both the measured and modeled outputs shown in Fig. 3. The mBVD model is comprised of a core resonator section consisting of "motional" RLC elements that represent the transduction from electrical to mechanical domains (and vice versa), the mechanical resonance and corresponding mechanical losses in the structure. The model also incorporates a static branch representing the parallel plate capacitance of the structure and a section representing extraneous capacitive and resistive parasitics attached to the structure. The electrical performance of the resonator can be quantified by the quality factor $Q = \frac{\omega_0 \times L_{motional}}{R_{motional}}$ and the effective electromechanical coupling coefficient $K^2_{eff} = \frac{\pi}{2}\frac{f_s}{f_p}\left[\frac{1}{tan\left(\frac{\pi}{2}\frac{f_s}{f_p}\right)}\right]$ where f_s and f_p correspond to the series and parallel resonance frequencies respectively [34]. The quality factor quantifies the loss of the resonator and the K^2_{eff} quantifies transduction efficiency. Shown in table I are measured parameters for the fabricated resonators.

The devices fabricated on glass were used as a starting point for the design of a CMOS integrated circuit (IC) for demonstrating SMR-CMOS integration. As mentioned earlier, SMRs are primarily used in filters and oscillators. An SMR-based filter consists of multiple resonators tuned to different resonant frequencies [2]. Therefore, for simplicity, an oscillator circuit was selected as the demonstrator vehicle since a single resonator can be used.

TABLE I
LUMPED MODEL FOR 100 μm × 100 μm SMR ON GLASS

Circuit Parameter	Units	Value
$L_{motional}$	nH	241.70
$C_{motional}$	fF	33.93
$R_{motional}$	Ω	5.30
$C_{parallel}$	fF	950.12
K^2_{eff}	-	4.5%
Q	-	500
R_{series}	Ω	0.2
$C_{substrate}$	fF	54

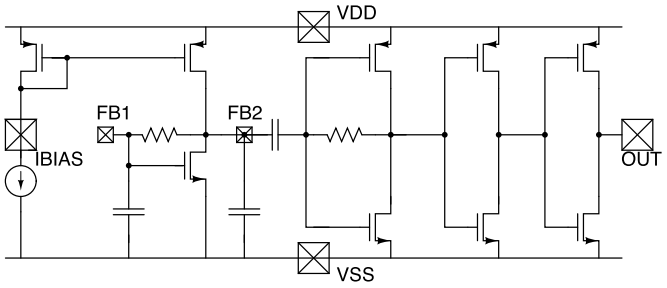


Fig. 4. Overall circuit schematic showing Pierce oscillator core, level shifter and buffer sections. squared crosses denote metal pads for electrical interconnection. FB1 and FB2 denote pads where the SMR is attached to the oscillator circuit. VDD, VSS, IBIAS and OUT denote pads for biasing and measurement of the oscillator output.

III. CMOS INTEGRATED CIRCUIT

A. Pierce Oscillator Circuit Design

To demonstrate SMR-CMOS integration, an oscillator IC was designed and fabricated in a Taiwan Semiconductor Manufacturing Corporation (TSMC) 65 nm CMOS process. The design consists of a single transistor Pierce oscillator [35] with a current mirror biased PMOS active load. The circuit was optimized for a resonator size of 100 μm × 100 μm. The Pierce oscillator output is fed to level shifter followed by an output buffer circuit capable of driving a 50 Ω load to avoid loading the resonant tank and enable external probing using RF coplanar probes. The complete circuit is shown in Fig. 4. Conceptually, the oscillator circuit produces a negative resistance that compensates the resistive losses in the resonator. The oscillator will only startup if the negative resistance exceeds the equivalent resistance of the resonator. Therefore, the oscillator design budgeted extra negative resistance margin to cope with potential SMR performance degradation when building directly on CMOS. Under full parasitic extraction, simulation yielded a maximum negative resistance value around 12 Ω for use with 100 μm × 100 μm SMR as shown in Fig. 5. This value is more than double the required negative resistance ($R_{motional}$ = 5.3Ω) for a 100 μm × 100 μm SMR built on glass from table I.

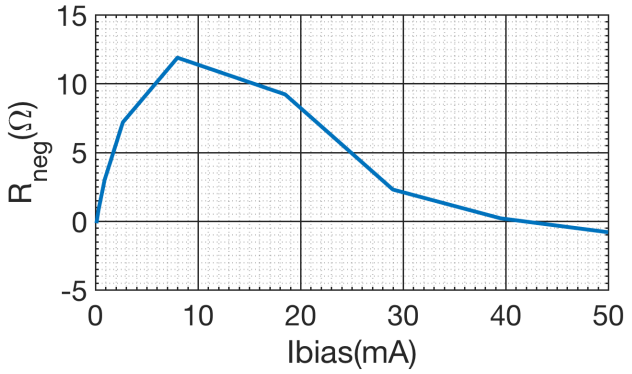


Fig. 5. Simulated negative resistance of the Pierce oscillator as a function of bias current. The simulation was performed at 1.8 GHz.

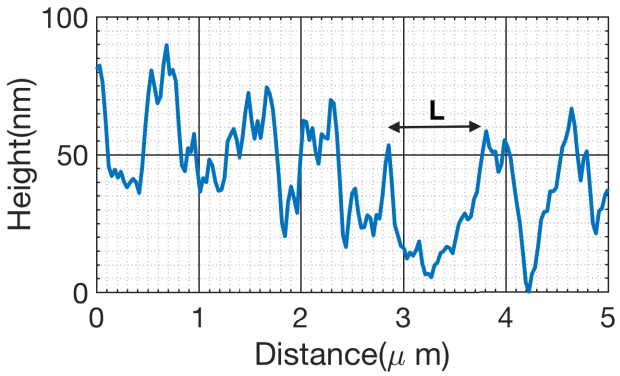


Fig. 6. Representative AFM cross-sectional scan of the surface of a 65 nm CMOS die as received from foundry. The scan length was 5 μm. The figure shows the worst-case lateral extent of the roughness (L).

B. Surface Roughness and Acoustic Losses

Acoustic scattering losses in the resonant device can contribute to significant reductions in quality factor. This is a concern since CMOS substrates typically present a rough top surface. Previous literature has shown a strong correlation between roughness of the the substrate on which the piezoelectric layer is deposited and the measured quality factor of the resonant device [36], [37]. In [36], a reduction in root-mean-square (RMS) surface roughness from 2.81 nm to 1.45 nm led to significant improvement in quality factor of barium-strontium titanate (BST) piezoelectric resonators. The quality factor was improved from 31 to 87 for a resonator operating at 4 GHz. The experiments in [36], [37] utilized BST as the piezoelectric material with an acoustic velocity between 5100 m s^{-1} and 6000 m s^{-1}. The ZnO piezoelectric layer used in this work exhibits a comparable acoustic velocity of 5600 m s^{-1}. Given the strong dependence of scattering losses on frequency and roughness, it is imperative to consider the effects of surface roughness in this work.

Based on the theory of diffuse acoustic scattering, the scattering-limited quality factor due to rough interfaces can be estimated as shown in eq.1 [38], [39]. The expression for the quality factor is:

$$\frac{1}{Q} \approx \left[(1 - exp(-4\pi\beta^2\sigma^2)]\frac{L}{\sigma\sqrt{16\pi^3}}\right] \quad (1)$$

where L corresponds to the lateral extent of the roughness, σ is the standard deviation of the roughness height and β is the wave number at the frequency of operation. It is important to note that the above equation tends to overestimate scattering loss compared with experiments, however it allows for qualitative assessment of the scattering loss dependence on operation frequency and roughness.

Based on the results from an atomic force microscopy (AFM) scan of the surface of a 65nm CMOS die (Fig. 6), a lateral extent of approximately 1 μm is observed and a roughness (σ) of 19.6 nm and a scattering-limited quality factor of 20 are computed. However, if the extent of the roughness (L) can be reduced below to 400 nm and the roughness (σ) can be reduced to 5 nm, eq.1 yields a quality factor of 202. Therefore, based on the above discussion, it is imperative to reduce CMOS surface roughness in order to achieve high quality factor SMR devices.

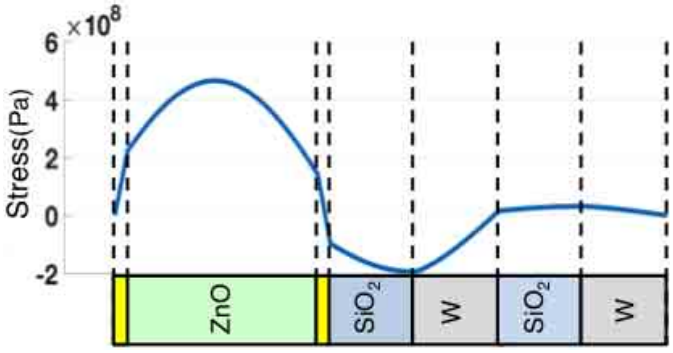


Fig. 7. Simulation showing the stress profile across the SMR structure. In the simulation, a 1.2 V sinusoidal excitation signal was applied to the piezoelectric layer at 1.78 GHz. The layer thicknesses were chosen to match those of test SMR devices fabricated on glass.

C. Acoustic Leakage into CMOS IC

Since the resonator is mechanically vibrating directly above the CMOS IC, acoustic leakage into the CMOS substrate is a concern. Through the piezoresistive effect [40], mechanical stress applied to the the silicon in a CMOS transistor channel can lead to a fractional change in silicon resistivity [41] given by eq.2:

$$\frac{\Delta R}{R} = \Pi\sigma \quad (2)$$

where Π is the transverse piezoresistive coefficient of silicon and σ is uniaxial stress experience by the transistor channel. In order to assess potential piezoresistive coupling between SMR and CMOS transistors, a 1-dimensional acoustic model was developed. Through and acoustic simulation, the uniaxial or longitudinal stress was computed throughout the SMR structure in response to a sinusoidal excitation of 1.2 V at a frequency of 1.78 GHz. The layer thicknesses used in the simulation correspond to those used for the test devices fabricated on glass. Shown in Fig. 7 is a plot of the simulated longitudinal stress component through the SMR structure.

The stress at the bottom of the Bragg reflector is calculated to be 3.2 kPa. Based on experimental measurements of the piezoresistive coefficient in n-type silicon [42], a value of $1200\,\mathrm{TPa}^{-1}$ was selected as a worst-case estimate of Π for lightly doped silicon ($10^{16}\,\mathrm{cm}^{-3}$). The fractional change in silicon resistivity is calculated to be 4 ppm. As a result, it is reasonable to neglect acoustic leakage into the CMOS substrate.

D. IC Layout and Fabrication Considerations

Following the schematic design, the layout of the top most IC layers was implemented with the objective of allowing simple fabrication of SMRs using a lithography based post-process with minimal degradation compared with devices built on glass. Alignment marks were incorporated in the top metal layer layout to allow for fine alignment using a contact-mask aligner. In order to protect the metal contact pads used for probing and interconnection to the oscillator circuit, the native passivation (polyimide) was retained over the pad areas. The passivation shields the pad metal from harsh etchants during the lithography process. A dry plasma etch was developed to remove this passivation layer as described in the following section. More importantly, provisions were made to provide a smooth build surface with low surface roughness.

Typically, CMOS processes do not include planarization of the top most metal and dielectric layers since CMOS dies are not designed as a substrate for microfabrication. As shown in [37], even a slight increase in substrate surface roughness from 3.2 nm to 6.9 nm can lead to a near 60% reduction in resonator quality factor. The increase in roughness contributes to increased scattering at the rough interfaces, which increases mechanical loss and degrades quality factor. Furthermore, rough surfaces interfere with the growth of piezoelectric layers which are typically seeded epitaxially from an underlying crystalline metal electrode. Increased surface roughness can interfere with the textured growth of the piezoelectric layer and lead to poor film crystallinity that directly impacts the piezoelectric strength of the deposited film (necessary for efficient transduction and low loss values) and the quality factor of the resonator. With typical CMOS back-end roughness values in the 10's of nm range, a method is needed to planarize and smooth the surface prior to SMR fabrication. Chemical Mechanical Planarziation (CMP) is a commonly used technique to planarize large silicon wafers to less than 1 nm surface roughness and is widely adopted in CMOS foundries to improve processing yield [43]. Performing CMP on small dies is very challenging and generally irreproducible.

It is worth noting that in virtually all modern CMOS processes, CMP is applied to the planarization of every level of metallization and dielectric with the exception of the top layer [43]. Therefore, the solution adopted in this work took advantage of this planarization by incorporating a sacrificial top metal "bed" in the layout, and using a back-end etching process to remove the topmost metal and dielectric layers and expose the underlying foundry planarized dielectric layer which can be used as an SMR build surface. This approach also reduces the roughness associated with metal fill features on the final metal layer. The specifics of the approach are outlined in the next section. Shown in Fig. 8 is a die photo of the 65 nm CMOS IC showing the layout features. Shown are the contact pads for the the oscillator (FB1 FB2), the probing pads, the lithography alignment marks, and the SMR bed which will be used for surface planarization.

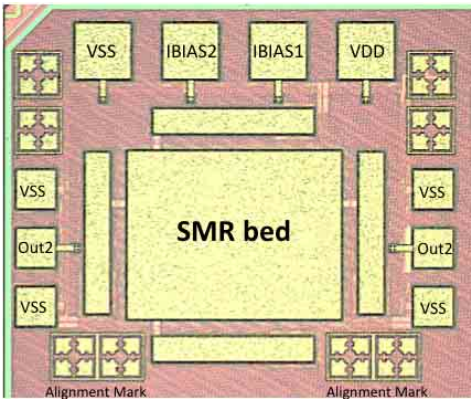
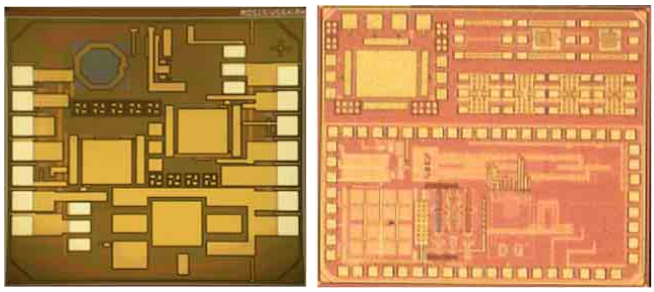


Fig. 8. 65 nm die photo outlining SMR bed, alignment marks and contact pads for oscillator circuit. This is how the die is received from foundry.



(a) (b)

Fig. 9. CMOS dies used in fabrication: (a) 1.5 mm × 1.5 mm 180 nm CMOS die (b) 2 mm × 1.7 mm 65 nm CMOS die

IV. SMR Fabrication on CMOS Substrate

In addition to the 65 nm CMOS dies designed for the SMR-CMOS integration, 180 nm CMOS dies were available for testing the die-level fabrication process before attempting the full integration on the 65 nm dies. Shown in Fig. 9 are both sets of CMOS dies, namely 1.5 mm × 1.5 mm 180 nm CMOS dies and 2 mm × 1.7 mm 65 nm CMOS dies.

A. Lithography and Photoresist Spinning

1) Photoresist Spinning: All patterning steps in this work, were performed using contact-lithography. A key challenge in working with small dies is resist spinning. Due to the small die size, significant beading of resist takes place at the die edges. Edge-beading can result in resist cracking during alignment. This is particularly noticeable when using thick resists. Shown in Fig. 10 is cracking of a 3 μm thick resist layer (Microchem LOR 30B [44]) on a 3 mm × 5 mm CMOS die upon contact alignment. As the die sizes decrease, the edge-bead occupies a larger area of the die surface.

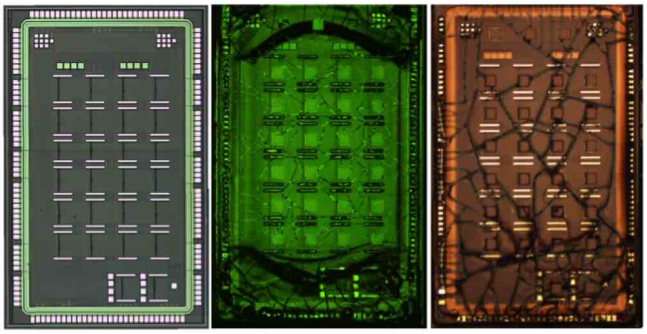
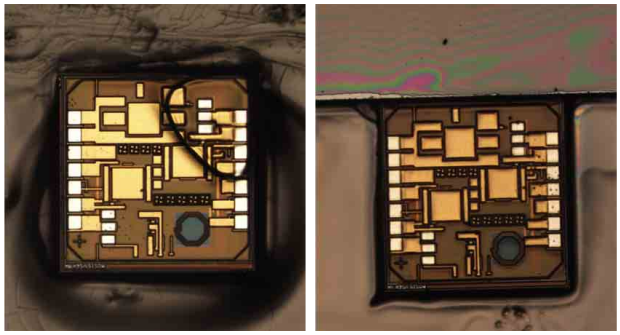


Fig. 10. Resist cracking: (a) 3 mm × 5 mm CMOS die before processing (b) CMOS die showing resist beading at edges (c) Resist cracks emanating from the bondpad ring.



(a) (b)

Fig. 11. Resist spinning on 180 nm die: (a) Beading without abutting die (b) Reduced edged beading with abutting and off-center spinning.

Processing of CMOS dies commenced by bonding the dies to a silicon carrier wafer. A number of bonding agents were explored. The key attributes desired were thermal stability during processing (incurred during resist baking ∼180 °C). Secondly, the bonding agent should be chemically stable in N-methyl pyrrolidinone (NMP), which is a solvent used for lift-off, and stable in tetramethylammonium hydroxide (TMAH)-based photoresist developer.

NMP is a very aggressive solvent and its use rules out most photoresists and epoxies as bonding agents. Furthermore, standard solvents such as acetone and isopropyl alcohol (IPA), which are used for surface cleaning, will generally dissolve most epoxies. Wafer-bonding epoxies such as CR-200 [45] exhibit temporary stability to NMP exposure (∼1 hour in NMP), however the number of lithography steps involved in SMR fabrication in this work can be as high as 12 steps with multiple hour-long soaks in NMP.

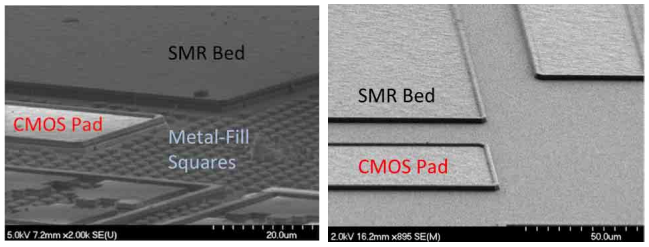
The decision was made to use the SU-8 family of negative epoxies [46] for bonding. SU-8 is a photo-imageable epoxy that exhibits high temperature stability (up to 300°C) and resistance to chemical etching in NMP after cross-link baking at temperatures above 150°C. Furthermore, SU-8 resists exhibit some degree of reflow during baking which allows them to more easily fill voids and imperfections in the CMOS die surface [47] .

To mitigate edge-bead formation, two process strategies were introduced. First, 6 mm × 6 mm bare silicon dies were thinned to the same thickness as the MPW CMOS dies (300 μm ± 10 μm) by etching in an SF_6/O_2 plasma using an OXFORD Plasmalab 80+ etching system. The etch was performed at 20 mtorr with 10 sccm and 10 sccm SF_6 and O_2 flow rates respectively. An ICP power of 50 W was used with an RF power of 250 W. The thinned silicon dies are first bonded to the carrier wafer. Following this, the carrier wafer is coated in SU-8 3005 epoxy and the CMOS die brought into close proximity to the abutting die using vacuum tweezers. Fine, carbon-tipped tweezers were used to gently press the CMOS die against the edge of the abutting die. The die-abutting is performed manually under a digital optical microscope to ensure minimal space between the dies i.e. complete contact along the edge of the dies. From previous experiments, small gaps between the dies (<100 μm) were observed to lead to bubbling of the resist in the area between the die edges. Subsequently, the abutted assembly is baked at 150°C for 5 hours to set both dies in place. The SU-8 bonding layer is spun at 3000 rpm for 45 s at an acceleration of 10 000 rpm s^{-1}.

The abutting die effectively extends the surface of the CMOS die and increases its area leading to much reduced edge-bead formation at the active area. Furthermore, any resulting edge-bead forms far away from the active area of the MPW die and can be easily removed by wiping with solvents. In order to avoid the need for abutting on every corner of the CMOS die, the assembled carrier wafer is mounted such that the CMOS die is positioned approximately 0.5 inches off-center from the center of the spinner chuck. The off-center mounting leads to resist flow primarily in a single direction over the surface of the CMOS die. As shown in Fig. 11, the abutting technique leads to a significant improvement in resist coating and reduction of edge beading even with the 180 nm dies which measure only 1.5 mm × 1.5 mm.

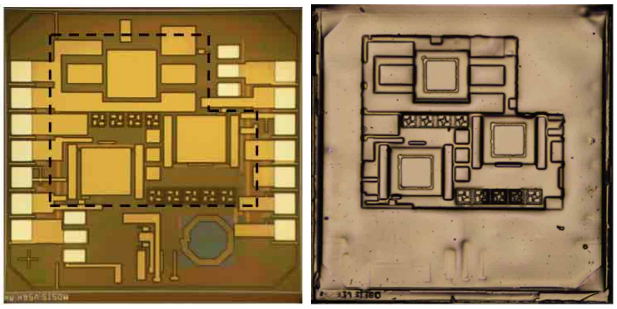
2) Bondpad Protection: For successful SMR-CMOS integration, it is necessary to protect the metal layers of the CMOS bondpads from chemicals used during microfabrication. For the 65 nm dies, the native foundry polyimide passivation was retained to cover the bondpads. In order to access the bondpads for electrical probing at the end of processing, a dry etching recipe was developed for etching the polyimide passivation. The etch is performed using a 1:4 SF_6/O_2 mixture in an Oxford Plasmalab 80+ inductively coupled (ICP) dry etching system. It is crucial to adequately control the etch depth of this process. Over etching can expose underlying layers of the CMOS back-end which can lead to undesired electrical shorting. Fig. 12a demonstrates an over-etched CMOS die showing the dummy metal-fill squares.

In order to optimize the passivation etching, energy dispersive X-ray (EDX) spectroscopy was used. EDX shows a unique peak for each element present in the sample under examination. In the 65 nm CMOS dies, the top metallization layer is copper (Cu). The polyimide passivation is a polymeric compound rich in carbon (C). Initially, the C peak is very large compared with the Cu peak. Upon etching of the polyimide, the C peak reduces in intensity relative to the Cu peak. The optimal number of etch cycles was confirmed by noting when the carbon peak is no longer visible. In performing the etching,



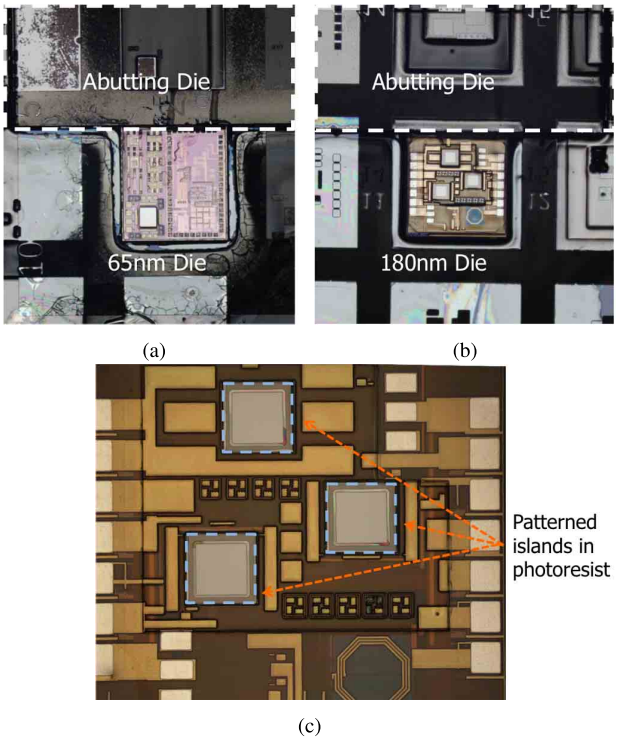
(a) (b)

Fig. 12. 65 nm polyimide passivation etching: (a) Un-optimized passivation etching exposing metal-fill squares. Also shown is the SMR bed and contact pads for CMOS circuit. (b) Optimized passivation etching.



(a) (b)

Fig. 13. 180 nm pad protection: (a) Die before pad protection showing area to be coated in SU-8 (b) Die following SU-8 pad protection. The die is coated in blanket aluminum to allow observation of pad protection ring.



(a) (b) (c)

Fig. 14. Die-abutting: (a) Abutted 65 nm die (b) Abutted 180 nm die (c) Successful lithographic patterning on 180 nm die with no damage to bondpads.

the key goal is prevent damage to the bed area, as that would eliminate any gains from from subsequent planarization. To this end, the copper top metal in the bed area serves as an etch-stop and prevents damage to the underlying planarized CMOS layer. The SF_6/O_2 etch chemistry leads to negligible etching of the copper layer allowing it to serve as a suitable etch-stop layer. For the dielectric layers surrounding the FBAR bed, planarity and low surface roughness are not critical. Therefore, slight over-etching can be tolerated. Consequently with the copper etch-stop, the etch-time was determined by the time necessary to completely the passivation layer with a few added etch cycles ($3 \times 30\,\mathrm{s}$) for over-etching to ensure complete passivation removal. Shown in Fig. 12b is an optimized passivation etch with optimized etch depth reaching the metal layer.

Processing on the 180 nm test sample shows an alternative possible approach to BEOL co-integration. The bondpads of the 180 nm IC were exposed using foundry glass-cuts (bondpad passivation openings) to enable testing upon receipt from foundry. Therefore, as opposed to the 65 nm IC, it was necessary to deposit a passivation coating on the bondpads prior to fabrication. Once again, the choice was made to use SU-8 3005 as a protective coating. SU-8 can resist developer and etchants and can be etched easily, after SMR fabrication, using the recipe developed for polyimide passivation etching. Equally important is the ability to lithographically pattern SU-8. Shown in Fig. 13a is a 180 nm die photo prior to passivation. In Fig. 13b, the SU-8 passivated die is shown. Due to the optical transparency of SU-8, the die is coated in blanket aluminum to increase the contrast between the die surface and SU-8 passivation. As can be observed, the outline of the inductor and bondpads are no longer visible due to the successful reflow of the SU-8 into the bondpad cavities and passivation layer openings or glass-cuts.

Combining the die-abutting and bondpad passivation approaches described above, successful lithographic patterning is achieved on both 65 nm and 180 nm dies. Fig. 14a and Fig. 14b respectively show abutted 65 nm and 180 nm dies with no visible observable beading following resist spinning. Fig. 14c shows lithographically patterned islands on the 180 nm die with no damage to the bondpads. The patterning was performed with a lift-off process based on a bi-layer of Microchem LOR 30B ($\sim 3\,\mu$m) and Shipley S1811 photoresist ($1.2\,\mu$m). This lift-off process was used for all patterning steps in this work (including ZnO patterning) with the exception of the gold top and bottom electrode patterning. In order to facilitate lift-off, a direct sputtering configuration was used which provides more "line-of-sight" deposition appropriate for lift-off. For the electrodes, the LOR 30B was substituted with a thinner coating of LOR 5A ($500nm$). It is worth pointing out that lift-off was primarily used for simplicity. A combination of wet etching and dry etching (using aluminum hardmask) can be used for patterning as well.

B. Surface Planarization

Following resist spinning, the next step is surface planarization to reduce surface roughness. The planarization etching process is shown schematically in Fig. 15. In the 65 nm die, the top metal copper metallization in the SMR bed is coated

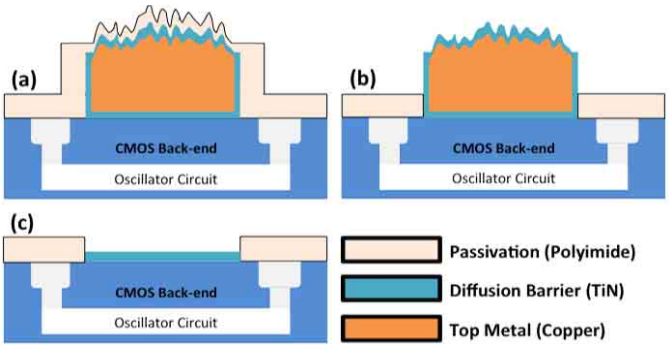
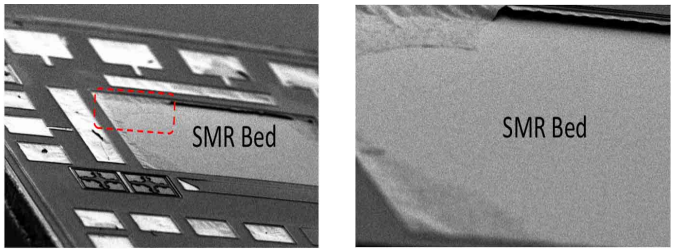


Fig. 15. Schematic of surface planarization. The dies as received (a) are etched to remove the passivation layer and expose the top metal layer (b). The diffusion barrier and top metal are subsequently etched to expose planarized surface as shown in (c).



(a) (b)

Fig. 16. SMR bed etching with insufficient removal of diffusion barrier. Shown in (a) is a microscope image of a processed 65nm die following in complete removal of diffusion barrier. A magnified image of the marked region is shown in (b) showing the diffusion barrier "tents" remaining due to insufficient removal of the barrier layer.

in a titanium nitride (TiN) barrier layer to prevent copper diffusion into the surrounding dielectric [43]. The presence of the TiN layer was confirmed using EDX spectroscopy. Attempting to etch the copper metallization before sufficiently removing the diffusion barrier can lead to diffusion barrier residue or "tents" that may complicate subsequent lithography as shown in Fig. 16a and Fig. 16b. A 2 min ICP chlorine etch (Oxford PlasmaPro System 100 Cobra) was used to remove this barrier layer in alternating 30 s etching and 30 s cooling cycles (Fig. 15b). With the diffusion barrier layer removed, a 4 min wet etch in Transene APS-100 copper etchant was used to selectively strip the exposed copper metal layer without damaging the underlying dielectric layer as shown in Fig. 15c. Shown in Fig. 17a and Fig. 17b are micrographs of the chip surface before and after the planarization etch process.

Using AFM characterization, it was verified that the above process did indeed significantly reduce the roughness of the SMR build surface. The before and after AFM scans in Fig. 17c and Fig. 17d show a reduction in the RMS surface roughness of the CMOS back-end from 20 nm to 5.2 nm. As shown the surface topography evolves from a rough, unstructured one to a smoother, ordered arrangement. The grid-like appearance of the after scan is due to the topology of the underlying dummy metal-fill squares used to improve the yield of the foundry CMP process. In the same manner,

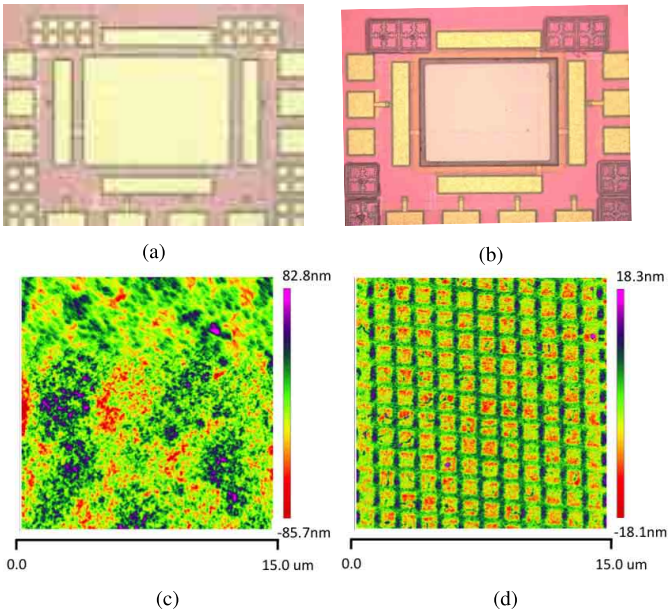


Fig. 17. Roughness reduction through back-end etching. The chip as received in (a) is coated in a polyimide passivation layer. In (b) the polyimide passivation is removed followed by etching of the top metal. AFM scans are also shown before (c) and after planarization etch (d). The RMS surface roughness is reduced from 20 nm in (c) to 5.2 nm in (d).

removing the top metal from the 180 nm dies yields a final surface roughness less than 5 nm.

Shown in Fig. 18 is the complete process flow for fabrication an SMR on the 65 nm CMOS chip. The process starts with the planarization etch described above (Fig. 18a,b). In the following step, the first section of the acoustic reflector is deposited via sputtering and patterned through lift-off (Fig. 18c). The reflector is then blanketed with a 680 nm sputtered silicon-dioxide layer which both serves as the top most reflector layer and also insulates the conductive tungsten layers of the reflector from shorting the subsequent metal electrodes (Fig. 18d). With the reflector complete, the bottom electrode is deposited using e-beam evaporation (Fig. 18e) followed by RF sputtering of the zinc oxide piezoelectric layer (Fig. 18f) and deposition of a gold top electrode (Fig. 18g). In order to access the resonator to the CMOS oscillator circuit, a dry etch is performed to remove the top-most polyimide passivation layer (Fig. 18h). Finally, a thick aluminum contact (2 μm) is sputtered deposited to connect the resonator to the underlying CMOS contact pads of the oscillator (Fig. 18i). Fig. 19 shows an optical micrograph of a completed 100 μm $\times$ 100 μm SMR on the CMOS die. Following SMR fabrication, the integrated oscillator was tested to verify functionality as described in the following section.

C. Electrostatic Discharge (ESD) Issues

Throughout the fabrication process, it is crucial to protect the CMOS transistors from ESD damage during the various plasma etching steps. It is worth noting that the top metal pads connecting the SMR device to the transistor circuitry are only exposed at the very end of the process, immediately before deposition of the final metal contact. Prior to this, the pads are shielded by the thick passivation layer (>1 μm).

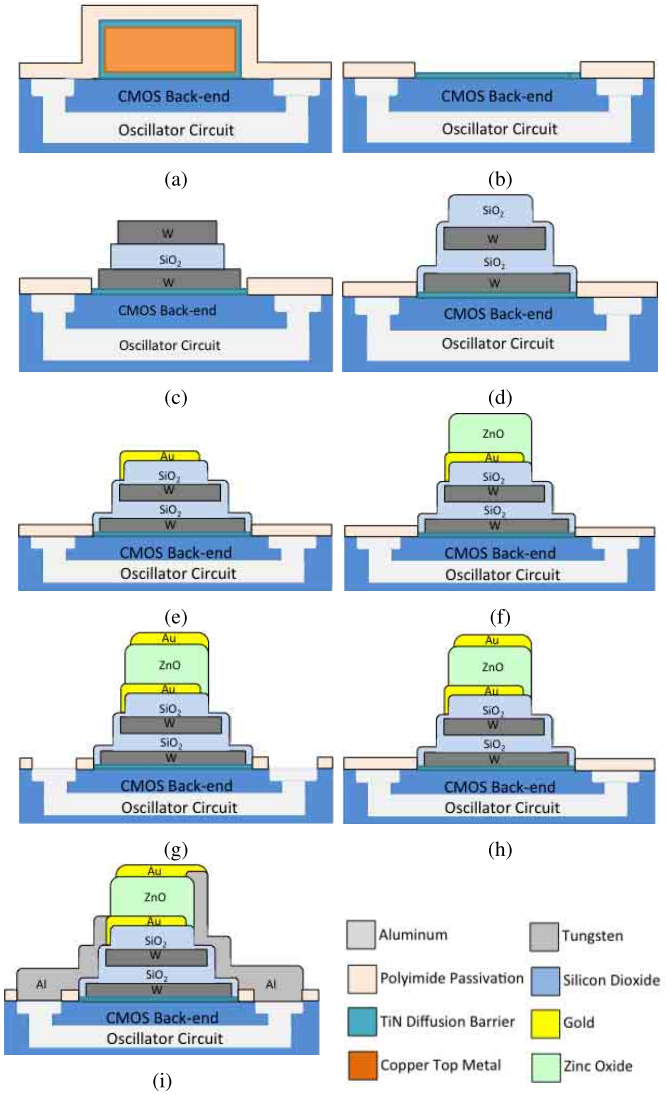


Fig. 18. Process flow for SMR-on-CMOS fabrication. The chip is bonded to the carrier substrate (a), followed by passivation etching and etching of the metal bed (b). The Bragg reflector layers are then patterned and deposited (c),(d) followed by deposition of the bottom electrode (e) and piezoelectric ZnO deposition (f). The top electrode is deposited to complete the resonator structure (g) followed by passivation etching to expose underlying CMOS pads (h). Finally, the SMR is connected to the CMOS circuit with a thick aluminum contact layer (i).

Therefore, any transistor gates connected to the pads only experience plasma processing for a short portion of the overall process. Additionally, ESD protection was applied to all the top metal pads and the circuit simulation was performed including the ESD structures and their corresponding parasitics. Finally, the passivation etching process and the metal sputtering deposition processes were tested on other CMOS dies fabricated in the same 65nm CMOS process and no discernible damage to the underlying transistors (e.g. threshold voltage shift) was observed.

V. Results

A. CMOS Oscillator Measurement

On-chip probing was used to verify functionality of the SMR-CMOS oscillator. This work primarily dealt with a $100\,\mu$m $\times$ $100\,\mu$m SMR circuit. DC power and current biasing for the oscillator circuit were provided through a 4-pin eye pass probe (Cascade Microtech) whereas the oscillator outputs were measured using $125\,\mu$m pitch GSG configuration RF coplanar probes (Cascade Microtech). Using a high-speed oscilloscope, the output waveform was measured at a frequency of 1.75 GHz (Fig. 20a) and a 600 mV (Fig. 20b) peak-peak output swing while driving 50Ω RF probes at a supply voltage of 1.1 V. The output oscillation frequency showed no noticeable frequency variation with Vdd scaling and the frequency corresponded very closely to the target resonant

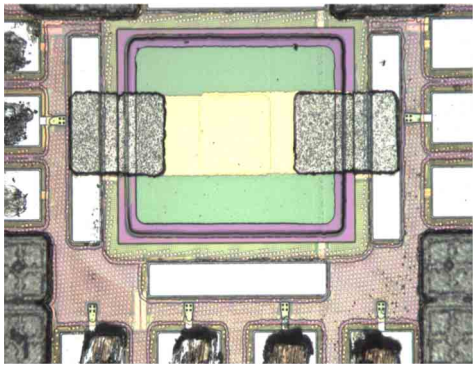
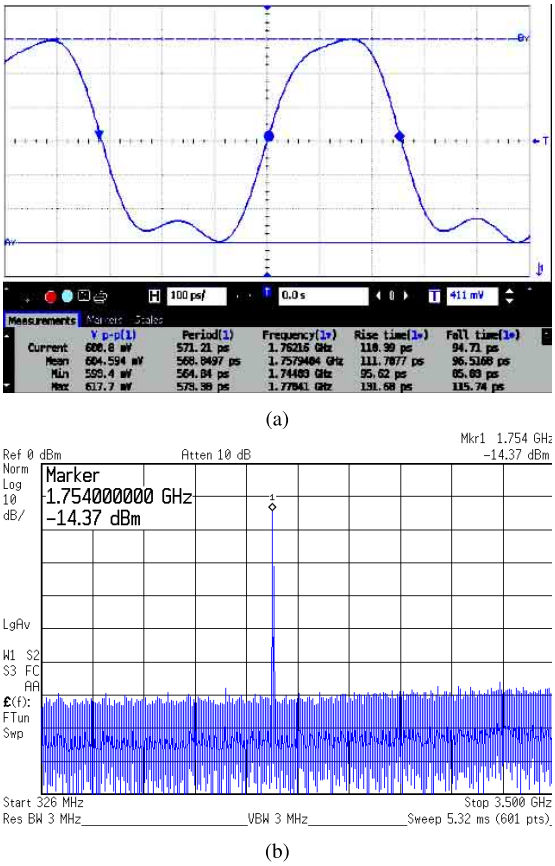


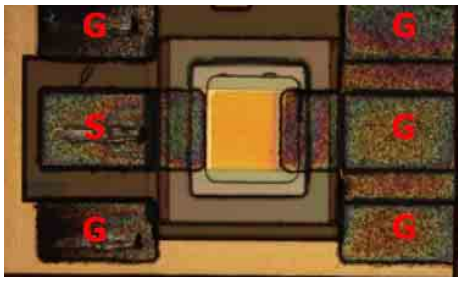
Fig. 19. Completed SMR on 65 nm CMOS die. The scratches on the metal pads are from the RF probes used for electrical testing.



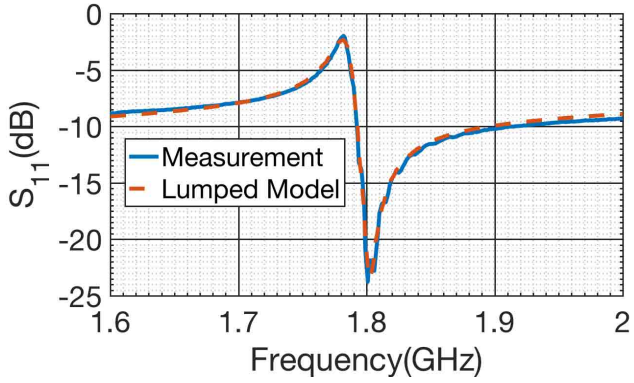
(a)

(b)

Fig. 20. (a) High Speed Oscilloscope and (b) Spectrum Analyzer Measurements of $100\,\mu$m SMR Oscillator.



(a)



(b)

Fig. 21. (a) Completed stand-alone SMR on 180 nm CMOS die. (b) Fitting of 180 nm probeable 100 μm × 100 μm resonator to lumped model.

TABLE II
SMR PERFORMANCE PROGRESSION

	Glass	CMOS
Q	500	460
K^2_{eff}	4.5%	3.3%
$R_s(\Omega)$	0.2	0.4
C_{sub}(fF)	54	300
$R_m(\Omega)$	5.3	6

frequency of the SMR as set by the piezoelectric deposition thickness. The combination of these observations ruled out oscillations caused by parasitic coupling and confirmed the oscillation indeed corresponds to the acoustic resonance of the SMR.

B. Stand-Alone SMR on CMOS

Due to area limitations of the 65 nm CMOS die, it was not possible to fabricate a stand-alone SMR for lumped model fitting and comparison with results from glass devices. However, the 180 nm CMOS provided extra area for a stand-alone SMR fabrication. The device was probed using on-chip using a one-chip GSG configuration. The completed device is shown in Fig. 21a. In order to assess integrity of the on-chip resonator, the resonator measurement was fit to a lumped BVD model as shown in Fig. 21b. The lumped fitting indicated Q values comparable to those measured for resonators on glass and and somewhat lower and K^2_{eff} values as shown in table II.

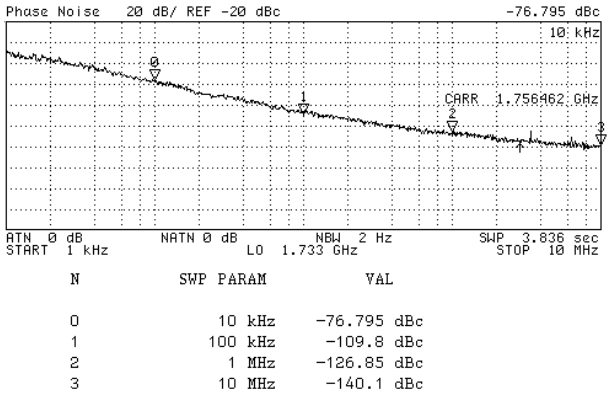


Fig. 22. Measured oscillator phase noise.

TABLE III
PUBLISHED SMR/FBAR OSCILLATORS COMPARISON

Reference	f_{osc}	Power	PN(100 kHz)	SMR	FOM
	GHz	mW	dBc/Hz		dB
[26]	1.9	0.3	-120	Off-chip	210.8
[49]	2.145	12	-124	Flip-chip	199.8
[50]	2.1	58.3	-120	Monolithic	188.8
[18]	5.46	4.59	-117.7	Monolithic	205.8
This Work	1.75	9.9	-109.8	Monolithic	184.7

C. Oscillator Phase Noise

In order to quantitatively assess the performance of the SMR-CMOS oscillator, phase noise measurements were performed. The oscillator shows a phase noise of 109.8 dB/Hz at a 100 kHz carrier offset for a 1.75 GHz oscillation frequency (Fig. 22). The oscillator consumes 9 mA at a supply voltage of 1.1 V. This is the power dissipation of the intrinsic oscillator and not including the power consumed by the output buffer. The overall foot-print of the oscillator including the SMR and transistor circuitry was 511 μm × 280 μm. The SMR is built directly atop the oscillator circuitry with no unshared silicon area. The phase noise performance is compared with other SMR-based oscillators in table III. The figure-of-merit (FOM) is calculated according to the equation below [48]:

$$FOM = 10\log\left(\left(\frac{f_{osc}}{\Delta f}\right)^2 \frac{1}{L\{\Delta f\}P}\right) \tag{3}$$

As shown in table III, the oscillator demonstrates a lower figure of merit than off-chip SMR/FBAR based oscillators due to its high power consumption and approximately 10 dB higher phase noise than comparable SMR oscillators at a 100 kHz carrier offset. The large power consumption is to be expected based on the conservative design of the oscillator circuit to account for required negative resistance values (Fig. 5). The lower phase noise compared with other SMR oscillators can be explained by observing the form of the oscillator phase noise in the $\frac{1}{f^2}$ region shown below [51]:

$$L\{\Delta\omega\} = 10\log\left[\frac{2kT}{P_{sig}}\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2\right] \tag{4}$$

where ω_0 is the oscillation frequency, Q is the quality factor of the resonant tank, $\Delta\omega$ is the offset from the carrier frequency and P_{sig} is the output power of the oscillator.

In [26], an output power of 6 dB corresponding to approximately 1.2 V peak-peak oscillation at 1.917 GHz was measured along with a phase-noise of 120 dB/Hz at 100 kHz carrier offset. An off-chip resonator of quality factor 1200 was used in this case. Contrasting these numbers with the 600 mV peak-peak swing of the 65 nm SMR-oscillator at 1.754 GHz and assuming a quality factor of 450 (based on glass device measurements), eq.4 yields a difference of 10.18 dB. This value agrees with the observed phase noise discrepancy. Therefore, it is clear that an increase in resonator quality factor can improve phase noise.

In this work, the emphasis was on simplicity of the demonstration structure. However, a number of industrially prevalent structural optimizations have been shown to improve the quality factor by more than 200% and these can be applied to the SMR-CMOS platform. In [52], measured resonator quality factor was increased from 400 to 2000 through modifications of the reflector layer thicknesses in what is known as a "Shear Mirror". Furthermore, a move to a suspended membrane device [2] can lead to even larger improvements in resonator quality factor. Finally, the die-level fabrication process presented in this paper for lithographic patterning and layer deposition can be adapted to different piezoelectric and electrode materials such as aluminum nitride (AlN) [2]. The bondpad passivation techniques discussed previously allow for the use of a variety of chemical etchants without damaging the bondpad metal or underlying circuitry.

VI. Conclusion

In this work, we have demonstrated a monolithically integrated SMR-CMOS oscillator on 65 nm CMOS. The fully supported SMR was built directly atop the CMOS transistor circuitry using a custom-developed die level post-process which ensures low-surface roughness through the use of BEOL features to overcome the roughness typically associated with scaled copper-low-K processes. This marks the first demonstration of a monolithically integrated piezoelectric resonator on 65 nm CMOS. Furthermore, the process was demonstrated for a CMOS die size of 2 mm × 1.7 mm which is more than 4 times smaller than previous die-level CMOS-resonator integration demonstrations. Future work will focus on improving resonator quality factor and extending the integration platform to RF filtering applications and low-phase noise RF oscillators.

Acknowledgment

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References

[1] C. Nguyen, *Vibrating RF MEMS for Low Power Wireless Communications*. Cambridge, MA, USA: MIT Microsystems Technology Laboratories, 2002.

[2] K. Y. Hashimoto, *RF Bulk Acoustic Wave Filters for Communications*. Norwood, MA, USA: Artech House, 2009.

[3] R. Ruby, P. Bradley, J. Larson, Y. Oshmyansky, and D. Figueredo, "Ultra-miniature high-Q filters and duplexers using FBAR technology," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2001, pp. 120–121.

[4] S. Mahon and R. Aigner, "Bulk acoustic wave devices–why, how, and where they are going," in *Proc. CS MANTECH Conf.*, 2007, pp. 15–18.

[5] R. C. Ruby, P. Bradley, Y. Oshmyansky, A. Chien, and J. D. Larson, III, "Thin film bulk wave acoustic resonators (FBAR) for wireless applications," in *Proc. IEEE Ultrason. Symp.*, vol. 1. Oct. 2001, pp. 813–821.

[6] L. W. Hung and C. T. C. Nguyen, "Capacitive-piezoelectric AlN resonators with Q greater than 12,000," in *Proc. IEEE Conf. Micro Electro Mech. Syst., (MEMS)*, Jan. 2011, pp. 173–176.

[7] S. Gong and G. Piazza, "Monolithic multi-frequency wideband RF filters using two-port laterally vibrating lithium niobate MEMS resonators," *J. Microelectromech. Syst.*, vol. 23, no. 5, pp. 1188–1197, Oct. 2014.

[8] M. Rinaldi, C. Zuniga, C. Zuo, and G. Piazza, "Super-high-frequency two-port AlN contour-mode resonators for RF applications," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, vol. 57, no. 1, pp. 38–45, Jan. 2010.

[9] R. Tabrizian, G. Casinovi, and F. Ayazi, "Temperature-stable silicon oxide ($SilO_x$) micromechanical resonators," *IEEE Trans. Electron Devices*, vol. 60, no. 8, pp. 2656–2663, Aug. 2013.

[10] L. C. Popa and D. Weinstein, "Switchable piezoelectric transduction in AlGaN/GaN MEMS resonators," in *Proc. Solid-State Sensors, Actuat. Microsyst. Conf., Transducers*, Jun. 2013, pp. 2461–2464.

[11] A. Ansari and M. Rais-Zadeh, "A thickness-mode AlGaN/GaN resonant body high electron mobility transistor," *IEEE Trans. Electron Devices*, vol. 61, no. 4, pp. 1006–1013, Apr. 2014.

[12] R. Abdolvand, G. K. Ho, J. Butler, and F. Ayazi, "ZNO-on-nanocrystalline diamond lateral bulk acoustic resonators," in *Proc. 20th IEEE Int. Conf. (MEMS)*, Kobe, Japan, Jan. 2007, pp. 795–798.

[13] Skyworks Solutions Inc. *SKY13741 Product Datasheet*, accessed on Feb. 26, 2017. [Online]. Available: http://www.skyworksinc.com/Product/3101/SKY13741three

[14] S. Mahon, J. Zepess, M. Andrews, and T. Semiconductor, "BAW flip-chip switched filter bank delivers dramatic form factor reduction," *High Freq Electron*, vol. 7, no. 8, pp. 24–28, Aug. 2008.

[15] Qorvo Semiconductor. *High end 3G/4G Solution*, accessed on Feb. 26, 2017. [Online]. Available: http://www.triquint.com/applications/mobile-devices/4g-lte

[16] K. Y. Hashimoto *et al.*, "Moving tunable filters forward: A 'heterointegration' research project for tunable filters combining MEMS and RF SAW/BAW technologies," *IEEE Microw. Mag.*, vol. 16, no. 7, pp. 89–97, Aug. 2015.

[17] M. E. Hassan, E. Kerherve, Y. Deval, A. A. Shirakawa, P. Jarry, and A. Cathelin, "A study on FBAR filters reconfiguration," in *Proc. 12th IEEE Int. Conf. Electron., Circuits Syst. (ICECS)*, Dec. 2005, pp. 1–4.

[18] M. Aissi, E. Tournier, M.-A. Dubois, G. Parat, and R. Plana, "A 5.4 GHz 0.35 μm BiCMOS FBAR resonator oscillator in above-IC technology," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2006, pp. 1228–1235.

[19] M.-A. Dubois, C. Billard, C. Müller, G. Parat, and P. Vincent, "Integration of high-Q BAW resonators and filters above IC," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2005, pp. 392–394.

[20] M. Dubois *et al.*, "Monolithic above-IC resonator technology for integrated architectures in mobile and wireless communication," *IEEE J. Solid-State Circuits*, vol. 41, no. 1, pp. 7–16, Jan. 2006.

[21] K. E. Wojciechowski, R. H. Olsson, M. R. Tuck, E. Roherty-Osmun, and T. A. Hill, "Single-chip precision oscillators based on multi-frequency, high-Q aluminum nitride MEMS resonators," in *Proc. Int. Solid-State Sens., Actuators, Microsyst. Conf.*, Jun. 2009, pp. 2126–2130.

[22] M. L. Johnston, I. Kymissis, and K. L. Shepard, "An array of monolithic FBAR-CMOS oscillators for mass-sensing applications," in *Proc. Solid-State Sensors, Actuators Microsyst. Conf., Transducers*, Jun. 2009, pp. 1626–1629.

[23] M. Nirschl *et al.*, "CMOS-integrated film bulk acoustic resonators for label-free biosensing," *Sensors*, vol. 10, no. 5, pp. 4180–4193, 2010.

[24] M. L. Johnston, H. Edrees, I. Kymissis, and K. L. Shepard, "Integrated VOC vapor sensing on FBAR-CMOS array," in *Proc. IEEE Conf. Micro Electro Mech. Syst., MEMS*, Jan. 2012, pp. 846–849.

[25] M. L. Johnston, I. Kymissis, and K. L. Shepard, "FBAR-CMOS oscillator array for mass-sensing applications," *IEEE Sensors J.*, vol. 10, no. 6, pp. 1042–1047, Jun. 2010.

[26] B. P. Otis and J. M. Rabaey, "A 300 μw 1.9 GHz CMOS oscillator utilizing micromachined resonators," *IEEE J. Solid-State Circuits*, vol. 38, no. 7, pp. 1271–1274, Jul. 2003.

[27] H. Takeuchi, A. Wung, X. Sun, R. T. Howe, and T.-J. King, "Thermal budget limits of quarter-micrometer foundry CMOS for post-processing MEMS devices," *IEEE Trans. Electron Devices*, vol. 52, no. 9, pp. 2081–2086, Sep. 2005.
[28] F. Carta, S. M. Gates, A. B. Limanov, J. S. Im, D. C. Edelstein, and I. Kymissis, "Sequential lateral solidification of silicon thin films on cu BEOL-integrated wafers for monolithic 3-D integration," *IEEE Trans. Electron Devices*, vol. 62, no. 11, pp. 3887–3891, Nov. 2015.
[29] Y.-H. Hsu, J. Lin, and W. C. Tang, "RF sputtered piezoelectric zinc oxide thin film for transducer applications," *J. Mater. Sci. Mater. Electron.*, vol. 19, no. 7, pp. 653–661, 2008.
[30] W. E. Newell, "Face-mounted piezoelectric resonators," *Proc. IEEE*, vol. 53, no. 6, pp. 575–581, Jun. 1965.
[31] K. Lakin, K. McCarron, and R. Rose, "Solidly mounted resonators and filters," in *Proc. IEEE Ultrason. Symp.*, vol. 2, Nov. 1995, pp. 905–908.
[32] J. D. Larson, III, P. D. Bradley, S. Wartenberg, and R. C. Ruby, "Modified Butterworth-van Dyke circuit for FBAR resonators and automated measurement system," in *Proc. IEEE Ultrason. Symp.*, vol. 1. Oct. 2000, pp. 863–868.
[33] K. Van Dyke, "The electric network equivalent of a piezoelectric resonator," *Phys. Rev*, vol. 25, no. 6, p. 895, 1925.
[34] T. Pensala, "Thin film bulk acoustic wave devices: Performance optimization and modeling," VTT, Espoo, Finland, Tech. Rep. 756, 2011.
[35] G. W. Pierce, "Piezoelectric crystal resonators and crystal oscillators applied to the precision calibration of wavemeters," *Proc. Amer. Acad. Arts Sci.*, vol. 59, no. 4, pp. 81–106, 1923.
[36] G. N. Saddik, J. Son, S. Stemmer, and R. A. York, "Improvement of barium strontium titanate solidly mounted resonator quality factor by reduction in electrode surface roughness," *J. Appl. Phys.*, vol. 109, no. 9, p. 091606, 2011.
[37] A. Vorobiev, J. Berge, S. Gevorgian, M. Löffler, and E. Olsson, "Effect of interface roughness on acoustic loss in tunable thin film bulk acoustic wave resonators," *J. Appl. Phys.*, vol. 110, no. 2, p. 024116, 2011.
[38] S. Gevorgian, A. Tagantsev, and A. K. Vorobiev, *Tuneable Film Bulk Acoustic Wave Resonators*. London, U.K.: Springer-Verlag, 2013.
[39] A. Vorobiev and S. Gevorgian, "Impact of the electrode material and shape on performance of intrinsically tunable ferroelectric FBARs," *IEEE Trans. Ultrason., Ferroelectr., Freq. Control*, vol. 61, no. 5, pp. 840–848, May 2014.
[40] C. S. Smith, "Piezoresistance effect in germanium and silicon," *Phys. Rev.*, vol. 94, no. 1, p. 42, 1954.
[41] Y. Kanda, "Piezoresistance effect of silicon," *Sens. Actuators A, Phys.*, vol. 28, no. 2, pp. 83–91, 1991.
[42] C.-H. Cho, R. C. Jaeger, and J. C. Suhling, "Characterization of the temperature dependence of the piezoresistive coefficients of silicon from–150 °C to +125 °C," *IEEE Sensors J.*, vol. 8, no. 8, pp. 1455–1468, Aug. 2008.
[43] M. J. Madou, *Fundamentals of Microfabrication: The Science of Miniaturization*. Boca Raton, FL, USA: CRC Press, 2002.
[44] Microchem Corporation. *LOR and PMGI Resists Product Datasheet*, Accessed on May 25, 2016. [Online]. Available: http://microchem.com/pdf/PMGI-Resists-data-sheetV-rhcedit-102206.pdf
[45] Brewester Science. *CR-200 Product Datasheet*, Accessed on May 25, 2016. [Online]. Available: http://www.brewerscience.com/wp-content/uploads/2016/06/17.05.01_WaferBOND-CR-200-TDS.pdf
[46] Microchem Corporation. *SU8 3005 Product Datasheet*, Accessed on May 25, 2016. [Online]. Available: http://microchem.com/pdf/SU-8%203000%20Data%20Sheet.pdf
[47] G. Hong, A. S. Holmes, and M. E. Heaton, "SU8 resist plasma etching and its optimisation," *Microsyst. technol.*, vol. 10, no. 5, pp. 357–359, 2004.
[48] P. Kinget, "Integrated GHz voltage controlled oscillators," in *Analog circuit design*. New York, NY, USA: Springer, 1999, pp. 353–381.
[49] S. Razafimandimby, A. Cathelin, J. Lajoinie, A. Kaiser, and D. Belot, "A 2 GHz 0.25 μm SiGe BiCMOS oscillator with flip-chip mounted BAW resonator," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2007, pp. 580–623.
[50] K. B. Ostman, S. T. Sipila, I. S. Uzunov, and N. T. Tchamov, "Novel VCO architecture using series above-IC FBAR and parallel LC resonance," *IEEE J. Solid-State Circuits*, vol. 41, no. 10, pp. 2248–2256, Oct. 2006.
[51] T. H. Lee and A. Hajimiri, "Oscillator phase noise: A tutorial," *IEEE J. Solid-State Circuits*, vol. 35, no. 3, pp. 326–336, Mar. 2000.
[52] S. Marksteiner, J. Kaitila, G. G. Fattinger, and R. Aigner, "Optimization of acoustic mirrors for solidly mounted BAW resonators," in *Proc. IEEE Ultrason. Symp.*, vol. 1. Sep. 2005, pp. 329–332.

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