On-chip transistor characterisation arrays for variability analysis

V. Wang and K.L. Shepard

A high-throughput on-chip transistor characterisation macro that can be used to efficiently and accurately characterise large, dense arrays of transistors for variability studies is designed. The prototype macro is used to perform current–voltage characterisation of a 2.8 mm^2, 1600-transistor array with digital interfaces.

Introduction: Process variability [1] is a critical concern in nanometre-scale CMOS, owing to random device fluctuations [2] (dopant fluctuation, line-edge roughness) and also reticle and proximity effects, which have difficult-to-predict impacts on device characteristics. Traditionally, process variability is characterised by one of two methods: either individual devices with pads are characterised on an automated wafer stepper or a 'silicon dense' structure of ring oscillators [3] is used to find correlations between frequency and variation. The first method provides high accuracy at the cost of large area overhead and low information throughput. The second method, although providing higher throughput, 'integrates' all the characteristics of multiple devices into one measured number dramatically reducing information content. Recent methods focus on multiplexed transistor arrays [4] because they provide high-density access to multiple devices for characterisation. These designs have been limited by slow and difficult characterisation through off-chip analogue measurement and complexities associated with removing the effects of switch resistances.

This Letter presents the design of an on-chip current–voltage characterisation system that allows for rapid characterisation of a large, dense array of multiplexed devices, eliminating the effects of switch resistances and allowing for current measurement from 100 nA (minimum resolvable current) to 3 mA (full-scale range). On-chip data conversion allows fully digital output from the measurement circuits.

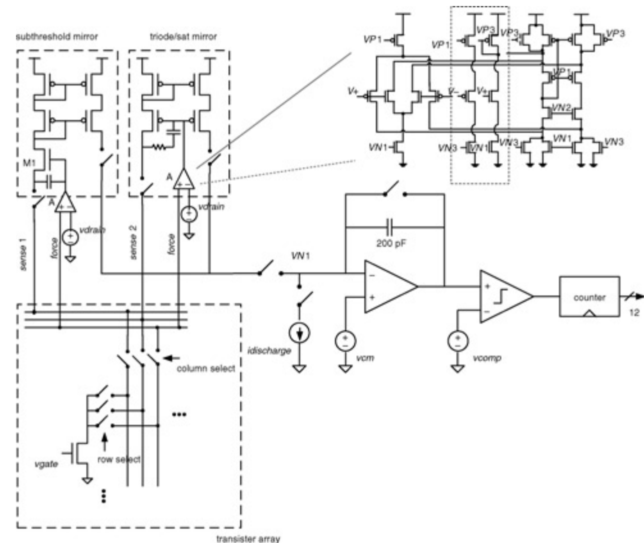

Fig. 1 *System block diagram of measurement circuits*

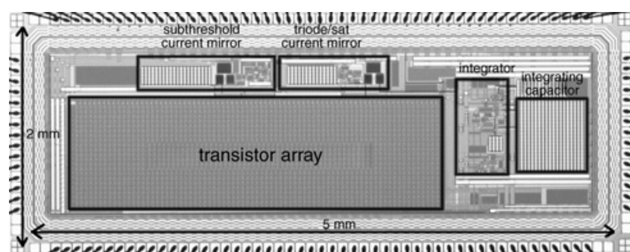

Fig. 2 *Chip micrograph showing device array and measurement circuits*

System design: The block diagram of the on-chip measurement system is shown in Fig. 1. The die photo of the design as implemented in a 0.25 μm 2.5 V CMOS technology is shown in Fig. 2. A custom layout generator is used to form the transistor array, containing 80 × 20 NMOS devices with a total area of 2.8 mm^2. The switches, implemented with thick-oxide devices, are incorporated into the array layout and consume <60% of the area of the array. Test structures for this array include devices of various sizes, of varying orientations (horizontal or vertical), in the presence or absence of parallel dummy poly, and with gates covered or uncovered by first-level metal.

One device-under-test (DUT) is selected for measurement with row-select and column-select scan chains. The gate voltage is applied directly to the DUT, while a force-sense technique is used to apply the drain voltage. Separate force and sense leads connect to each transistor channel in the array. This allows the current mirror to mirror the device current (*isense*), while ensuring (through the negative feedback of the current mirror) that the drain voltage of the selected transistor is at *vforce* despite voltage drops across the switches. The cascoded current mirror is necessary to boost the output resistance of the mirror and avoid significant gain errors. Data conversion is implemented with an integrating amplifier and high-gain comparator. An integrating capacitor value of 200 pF is used to accommodate the full current range. The ADC conversion has a linearity which exceeds 10 bits for all input current ranges and has 8 bits of absolute accuracy including current mirrors.

For low *isense* current levels associated with subthreshold operation of the DUT, the 'triode/sat mirror' in Fig. 1 has stability problems. The very large subthreshold small-signal resistance of the DUT makes the pole at the drain of the DUT significant. The addition of M1 to the 'subthreshold mirror' serves to stabilise the feedback loop by reducing the impedance looking into the mirror.

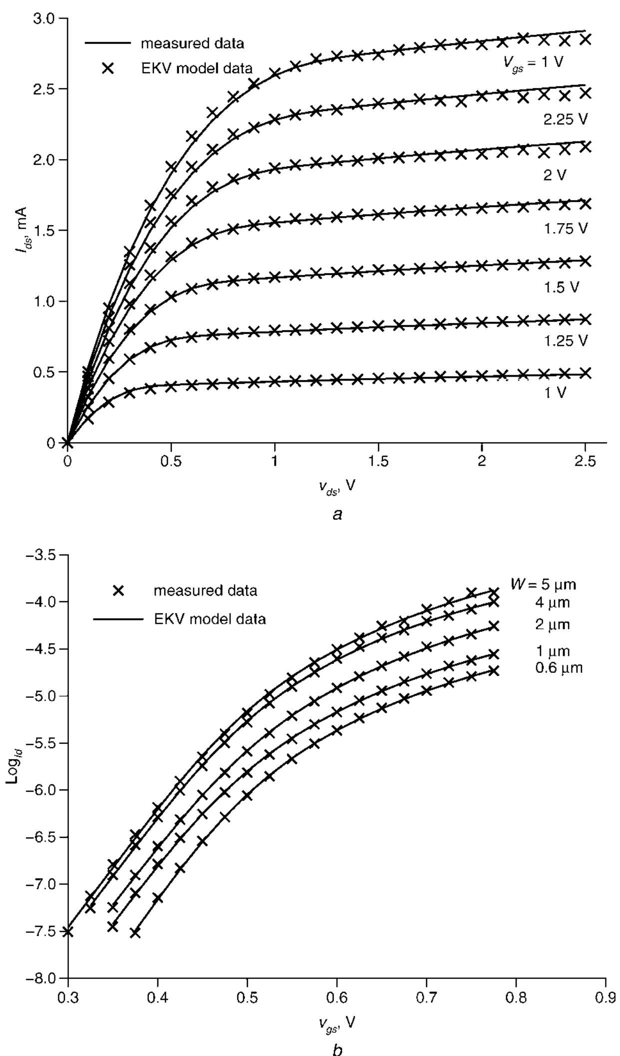

Fig. 3 *I_d against V_{ds} for NMOS $W/L = 0.5/0.25$ μm; and subthreshold current for $W = 0.6$, 1.0, 2.0, 4.0 and 5.0 μm*

a I_d against V_{ds}
b Subthreshold current

The amplifier A used in both current mirrors has a DC gain of 80 dB with a common-mode input range designed to operate across the full

supply. This is accomplished with both NMOS and PMOS input differential pairs in a folded cascode amplifier [5]; when one pair cuts off, the other continues to operate. Gain variation over the common-mode input range is mitigated by the action of transistors highlighted with the dotted box in Fig. 1, which increases the current bias through the cascode near the extremes of the common-mode input range when only one pair is active. Both the current mirrors and amplifier A are fabricated with thick-oxide devices (enabling straight-forward migration to more advanced technologies). The current mirrors each operate with a supply voltage above 4 V. This ensures sufficient headroom to allow device characterisation up to 2.5 V.

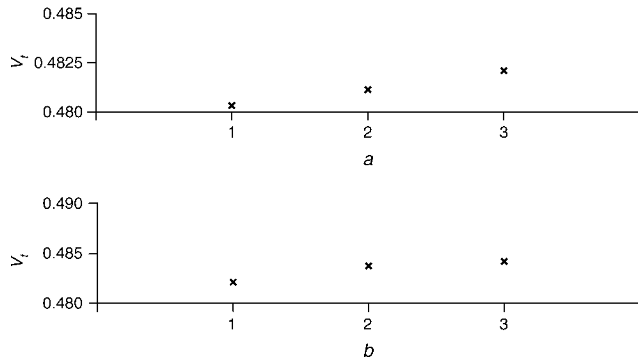

Fig. 4 *Effects of V_T for spacings of (1) 0.8 µm, (2) 1.2 µm, and (3) no dummy and Vt for (1) 0%, (2) 50% and (3) 100% overlap*

a Dummy poly to active poly spacing
b First-level over active poly

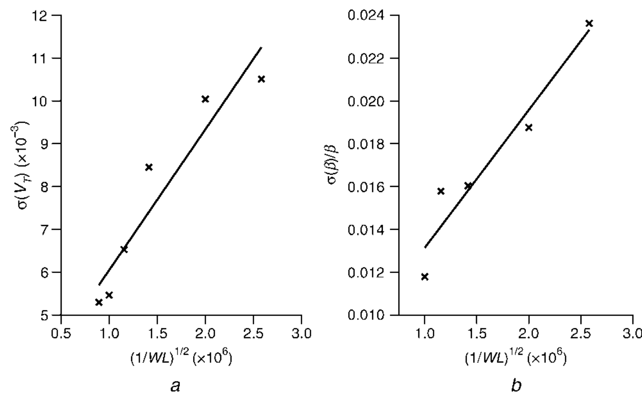

Fig. 5 *Standard deviation of VT and current factor β*

a V_T
b β

Results: Measurements were performed on 1600 devices on six individual dice spread across a single wafer. Fig. 3*a* shows representative measured characteristics of an NMOS device of $W/L = 5/0.24$ µm. The subthreshold characteristics in Fig. 3*b* reflect typical characteristics for each of the unique device widths in the test array. We chose to regression fit to the EKV MOSFET [6] model because it has a relatively small number of device parameters and has a well-behaved, non-stochastic, model-fitting behaviour. Only parameters VTO, DP, THETA, UCRIT, LAMBDA, GAMMA, and LETA are varied in the fit. GAMMA (the body effect parameters) allows subthreshold characteristics to be matched, even though V_{BS} is not varied in the experimental data. In Fig. 3, the solid curves are the EKV model fits, while the discrete points reflect the actual data. Statistical analysis was performed on two parameters, V_T and β, ignoring any potential correlation between these two parameters.

Systematic effects are explored as a function of device sizes, dummy poly spacing, and metal-one overlap. We explore each function space one variable at a time recognising that a more complex multidimensional function is being probed. Fig. 4 shows V_T variation for a single die as a function of poly spacing and metal-one coverage. Fig. 4*a* shows the average threshold voltage for three different spacings to dummy poly. Fig. 4*b* shows the same average threshold voltage for different amounts of M1 gate coverage. *F*-tests of the former ($F_{2,213} = 1.47$ and $p = 0.23$) and latter ($F_{2,213} = 2.94$ and $p = 0.06$) indicate possible significance for poly spacing trends and strong statistical significance for metal-one coverage. Migrating this design to more aggressive technology nodes can be expected to result in more statistically significant local layout effects owing to subwavelength lithography and stress [3]. Figs. 5*a* and *b* show random residuals $\sigma(V_T)$ and $\sigma(\beta)/\beta$ against device size. These show the well-known $1/\sqrt{WL}$ dependence associated with random, short-length-scale fluctuations [2].

The measurement techniques described here allow for high-throughput device characterisation with digital interfaces, while eliminating the parasitics effects of multiplexing circuits. The data volume available with these high throughput techniques will enable fundamental variability studies in advanced technologies.

© The Institution of Engineering and Technology 2007

14 January 2007
Electronics Letters online no: 20070017
doi: 10.1049/el:20070017

V. Wang and K.L. Shepard (*Department of Electrical Engineering, Columbia University, New York, NY 10027, USA*)

E-mail: shepard@ee.columbia.edu

References

1 Nassif, S.: 'Delay variability: sources, impacts, and trends'. Proc. Int. Solid-State Circuits Conf., 2000, pp. 368–369
2 Pelgrom, M., Duinmaijer, A.C.J., and Welbers, A.P.G.: 'Matching properties of MOS transistors', *IEEE J. Solid-State Circuits*, 1989, **24**, pp. 1433–1440
3 Pang, L.-T., and Nikolic, B.: 'Impact of layout on 90 nm CMOS process parameter fluctuations'. Symp. on VLSI Circuits, 2006, pp. 69–70
4 Agarwal, K., Liu, F., McDowell, C., Nassif, S., Nowka, K., Palmer, M., Acharyya, D., and Plusquellie, J.: 'A test structure for characterizing local device mismatches'. Symp. VLSI Circuits, 2006, pp. 67–68
5 Bananezhad, J.: 'A rail-to-rail CMOS op amp', *IEEE J. Solid-State Circuits*, 1988, **23**, pp. 1414–1417
6 Mucher, M., Lallement, C., Enz, C., Theodoloz, F., and Krummenacher, F.: 'The EPFL-EKV MOSFET model equations for simulation', http://legwww.epfl.ch/ekv/pdf/ekv_v262.pdf