CAD Issues for CMOS VLSI Design in SOI *

Kenneth L. Shepard
Columbia Integrated Systems Lab, Columbia University, New York, NY 10027
and CadMOS Design Technlogy, San Jose, CA
shepard@ee.columbia.edu

Abstract

This paper reviews recent progress in making circuit-level CAD tools for the design of digital integrated circuits SOI-aware, specifically transistor-level static timing and static noise analysis tools. This involves abstracting the SOI device physics of the floating body, allowing estimates of the body voltage variation under various switching activity assumptions. These body voltage estimates are then applied as "initial conditions" in the constituent simulations of the static analyses. Results are presented for a prototype static timing analysis tool and a commercial static noise analysis tool.

1 Intoduction

Partially-depleted silicon-on-insulator (PD-SOI) has emerged as a leading technology for high-performance, low-power deep-submicron digital integrated circuits[1, 2, 3, 4, 5, 6]. The characteristic feature of this process is that all devices are dielectrically isolated from each other with the body of each transistor separated from the substrate by a buried oxide. PD-SOI technology delivers two main advantages for digital applications: the reduction of the parasitic capacitance associated with source and drain diffusions and the reduction of the reverse-body effect in FET series connections. Acting together, these effects result in the faster switching of stack structures in PD-SOI than in bulk CMOS. In addition to higher speed (or lower power) operation, PD-SOI also enables the possibility of greater logic function from a given channel-connected component (CCC).

The reduced reverse-body effect in stack structures comes about because the body of the transistors is floating. At the device and circuit level, however, this floating-body effect poses major challenges in the successful use of this technology. There is a parasitic bipolar effect which can result in noise failures if not correctly considered[7]. In addition, there can be large "uncertainties" in the body potential, and consequently the threshold voltage, of devices due to unknown past switching activity. Without special effort, the design margining required in timing analysis to protect against this uncertainty erodes much of the potential performance advantage under nominal operation. Similarly, without special effort in noise analysis, many circuit styles in which noise margin is strongly determined by threshold voltage (e. g. dynamic circuits) could be significantly overdesigned because of conservative body-voltage margining. Static timing[8] and static noise[9] analysis tools, which have become central to the verification of leading-edge digital designs, must be enhanced to understand the unique features of SOI technology. In particular, they must provide accurate bounds on the floating-body potentials of the devices from known switching and circuit topology information. These bounds provide the necessary "initial conditions" for the constituent simulations of the static analysis. Where these bounds are not adequate to prevent overdesign, the tools should provide options for reducing the potential body voltage variation.

Much of the CAD effort to date in SOI technology has focussed on the device modelling issues[10, 11, 12, 13, 14], in particular the ability to calculate the floating-body effects over long periods of time properly in circuit simulation. In this review, we consider recent work toward making higher-level CAD tools SOI-aware (i. e., transistor-level static timing and noise analysis tools)[15, 16]. This involves an abstraction of the SOI device physics of the floating body described in Section 2. Section 3 describes how these body-voltage estimates are applied to static timing analysis with results presented from a prototype tool. Section 4 considers the special issues associated with static noise analysis. Results are presented for a commercial static noise analysis tool.

2 PD-SOI device physics and body-voltage estimation

The body potential of a PD-SOI FET is determined by capacitive coupling of the body to the gate, source, and drain, by diode currents at the source-body and drain-body junctions [including gate-induced drain leakage (GIDL)[17]], by impact ionization currents produced by current flow through the device (sometimes referred to as the on-state impact ionization current), and (for deeply-scaled FETs) leakage through the gate oxide.[1] Moreover, it is convenient to distinguish "fast" and "slow" processes. Fast processes can change the body potential on time scales on the order of or less than the cycle time, while slow processes require time scales much longer than the cycle time (up to milliseconds) to affect the body voltage. There are two fast mechanisms at work: switching transitions on the gate, source, or drain which are capacitively coupled to the body (which we call *coupling displacements*), and forward-bias diode currents across source-body and drain-body junctions with voltages exceeding the diode turn-on voltage (which we call *body discharge*). The slow processes involve charging or discharging the body through reverse-biased or very weakly forward-biased diode junctions and through impact ionization.

As a (usually) dynamic circuit node, the floating body has "memory." To model the switching history determining the body voltage of a particular device, we use the state diagram abstraction shown in Figure 1. (This diagram applies to the nFET. The state diagram of the pFET is the "dual" of this, in which the gate is high rather than low in states 3, 4, and 5; and low rather than high in states 1, 2, and 6.) The states denoted with solid circles represent "static" states, states in which the FET can be stable, in constrast with the "dynamic" states 6a and 6b, which are only present transiently during switching events. For example, state 1 corresponds to the case in which the gate is high and both the source and drain are low. Arrows indicate possible state transitions produced by switching events in the circuits containing these FETs. If the device is allowed to remain in one state for a very long time, the body voltage

*This work was supported in part by the National Science Foundation under grant CCR-97-34216 and by a grant from the IBM Corporation.

[1] We will not consider gate-leakage effects here.

0-7695-1025-6/01 $10.00 © 2001 IEEE

in each state i will achieve a dc value, denoted as s_i.

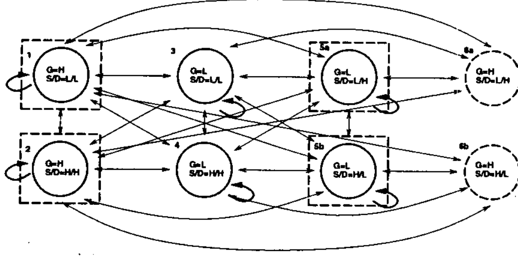

Figure 1: State diagram for a PD-SOI nFET.

We can represent the charge stored on the body as the value of the body voltage in one particular state of Figure 1, the *reference state*, which we choose to be state 2 for the nFET and state 1 for the pFET. From this reference body voltage (V_B^{ref}), we can then determine the corresponding body voltage in each state i (V_B^i) according to:

$$V_B^i = V_B^{ref} + d_i(V_B^{ref})$$

The displacements, $d_i(V_B^{ref})$, are explicitly shown to be dependent on the reference body voltage because of the strong voltage-dependence of the capacitances of the source-body, drain-body, and gate-body. Figure 2 shows these displacements as a function of V_B^{ref} for an example technology.

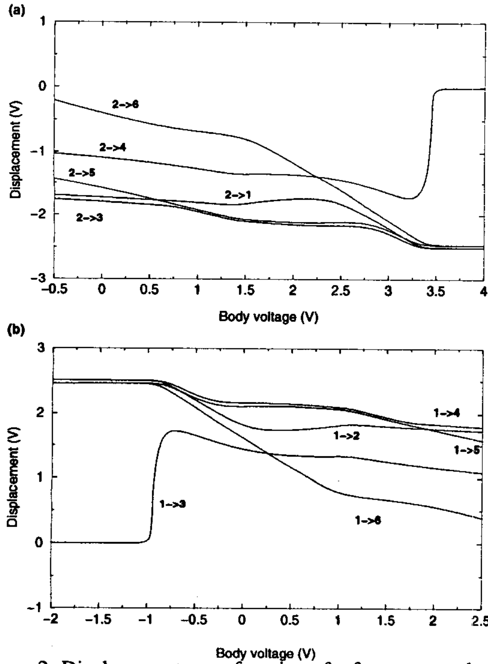

Figure 2: Displacements as a function of reference state body voltage at a 2.5-V supply for both the nFET (a), for which the reference state is state 2 and the pFET (b), for which the reference state is state 1.

With the reference body voltage as a "state-independent" way of representing the charge trapped on the body, we proceed to characterize each state i in Figure 1 by two values of this reference voltage, V_i^{zero} and $V_i^{forward}$. V_i^{zero} represents the steady-state value of the reference body voltage, achieved by remaining in state i for a long time. This follows immediately from the s_i in each state.

$$s_i = V_i^{zero} + d_i(V_i^{zero}) \tag{1}$$

$V_i^{forward}$ represents the value of the reference body voltage for the nFET (pFET) to which the body would be very quickly pulled down (up) as a result of body discharge (charge), if state i were accessed with a higher (lower) reference body voltage than $V_i^{forward}$. These $V_i^{forward}$ values presume that the fast body discharge will bring the forward-biased-junction bias down to a turn-on voltage of 0.6 V. (It is important to note that fast body discharge can trigger parasitic bipolar leakage between source and drain for FETs in state 5.) Table 1 shows V_i^{zero} and $V_i^{forward}$ for an example technology in a 2.5 V supply. In this technology, for instance, this means that if a FET which reached a dc steady-state in state 4 (with a V_4^{zero} of 3.43 V) switches into state 2, the reference body voltage will quickly discharge to $V_2^{forward} = 3.1V$. If the FET subsequently remains in state 2 for a long time, V_B^{ref} will eventually decrease to $V_2^{zero} = 2.5V$.

Reference [15] uses this information to provide two modes of body voltage "estimation." In "full-uncertainty" analysis, we assume that we have no knowledge of the switching activity of the circuit. We must choose maximum and minimum possible values of the body voltage that cover all possible stimulus and history. We say that a state is *accessible* if the circuit topology allows the state to be visited. (For example, for the nFET of an inverter, those states with the source high would not be accessible, because the source of the nFET is tied to ground.) We let $\mathcal{A}$ represent the set of such accessible states, including possibly the dynamic state 6. In this case, the minimum and maximum body voltages are given by:

$$(V_B^{ref})_{max} = \max_{j \in \mathcal{A}} V_j^{zero} \tag{2}$$

$$(V_B^{ref})_{min} = \min_{j \in \mathcal{A}} V_j^{zero} \tag{3}$$

If, however, one is assured that every accessible state is visited with reasonable frequency (i. e., on a time scale that is faster than the "slow" body-voltage mechanism), then the $V_j^{forward}$ values for the nFET (pFET) will cap the maximum (minimum) possible value of the body voltage. This is referred to as "accessibility" body-voltage estimation. For the nFET,

$$(V_B^{ref})_{min} = \min_{j \in \mathcal{A}} V_j^{zero} \tag{4}$$

$$(V_B^{ref})_{max} = \min(\max_{j \in \mathcal{A}} V_j^{zero}, \min_{j \in \mathcal{A}_{static}} V_j^{forward}) \tag{5}$$

while for the pFET,

$$(V_B^{ref})_{min} = \max(\min_{j \in \mathcal{A}} V_j^{zero}, \max_{j \in \mathcal{A}_{static}} V_j^{forward}) \tag{6}$$

$$(V_B^{ref})_{max} = \max_{j \in \mathcal{A}} V_j^{zero} \tag{7}$$

where $\mathcal{A}_{static}$ is the set of all accessible *static* states (i. e. states 1 through 5). State 6 is not included in this "accessibility" analysis because it is visited only "quickly" during a transition and cannot be assured to be active long enough to complete a discharge. Reference [15] shows how it is possible to refine this estimate even further with stochastic techniques. These require more detailed knowledge of signal timing and probabilities, which are, in practice, difficult to obtain and verify. This approach will not be considered more here.

i	nfet			pfet			nfet			pfet		
	s_i	V_i^{zero}	$V_i^{forward}$	s_i	V_i^{zero}	$V_i^{forward}$	s_i	V_i^{zero}	$V_i^{forward}$	s_i	V_i^{zero}	$V_i^{forward}$
1	0	1.77	2.41	0.0	0.0	-0.6	0	0.53	1.13	0	0	-0.6
2	2.5	2.50	3.1	2.5	0.73	0.12	1.0	1.0	1.6	1.0	0.469	-0.127
3	0	2.15	2.85	0	-0.92	-0.98	0	0.87	1.5	0	-0.75	-0.907
4	2.5	3.43	3.5	2.5	0.35	-0.30	1.0	1.75	1.906	1.0	0.14	-0.5
5	0.437	2.58	2.79	2.068	-0.045	-0.23	0.278	1.12	1.47	0.722	-0.118	-0.47
6	0.711	1.60	1.60	1.976	1.24	1.24	0.357	0.61	0.85	0.722	0.467	0.17

Table 1: Values of s_i, V_i^{zero}, and $V_i^{forward}$ for the nFET and pFET of our example technology.

While accessibility analysis does not require detailed switching knowledge, it does require that there is enough switching activity that every accessible state is visited with a minimum frequency. At times, this, too, may be difficult to ensure. We, therefore, propose a *modified accessibility analysis*. In this approach, signals in the design can be marked as *active*. This means that these particular signals are assured to switch with regular frequency. Clock nets are immediately obvious active nets. We then use these active net tags to come up with a set of constraints that must be satisfied by a modified accessibility set of states $\mathcal{A}_{ma}$. The body voltage will then be determined by equations identical to those used for accessibility analysis except that $\mathcal{A}_{static}$ is replaced by $\mathcal{A}_{ma}$. For the nFET,

$$(V_B^{ref})_{min} = \min_{j \in \mathcal{A}} V_j^{zero} \tag{8}$$

$$(V_B^{ref})_{max} = \min(\max_{j \in \mathcal{A}} V_j^{zero}, \min_{j \in \mathcal{A}_{ma}} V_j^{forward}) \tag{9}$$

while for the pFET,

$$(V_B^{ref})_{min} = \max(\min_{j \in \mathcal{A}} V_j^{zero}, \max_{j \in \mathcal{A}_{ma}} V_j^{forward}) \tag{10}$$

$$(V_B^{ref})_{max} = \max_{j \in \mathcal{A}} V_j^{zero} \tag{11}$$

Modified accessibility analysis reduces to accessibility analysis in the case that *all* of the nets are marked as active. Furthermore, it reduces to full-uncertainty analysis when *none* of the nets are marked as active. $\mathcal{A}_{ma}$ will be the accessibility set for the nFET (pFET) which satisfies the contraints while ensuring the maximum (minimum) value of the body voltage. These constraints are derived from the following rules:

- If the gate of the FET is an active net, then there must be a state in $\mathcal{A}_{ma}$ with the gate high and a state in $\mathcal{A}_{ma}$ with the gate low.
- If the source of the FET is connected to ground (supply) through a succession of transistors all of whose gates are active nets, then $\mathcal{A}_{ma}$ must contain a state with the source low (high).
- If the drain of the FET is connected to ground (supply) through a succession of transistors all of whose gates are active nets, then $\mathcal{A}_{ma}$ must contain a state with the drain low (high).
- Same-signal correlations must be considered and can result in stronger constraints. For example, if the gate of the current FET is marked as an active net, but must be high for a path to ground from the source to be present through a path of active-gate FETs, then $\mathcal{A}_{ma}$ must contain a state in which both the gate is high and the source is low.

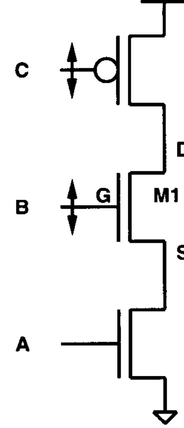

Figure 3: Example to demonstrate modified accessibility analysis.

We demonstrate modified accessibility analysis with the example shown in Figure 3. Nets C and B (marked with the arrows) are active nets. For transistor $M1$, therefore, there must be a state in $\mathcal{A}_{ma}$ with the source and gate both high, with the gate low, and with the drain high. To find $\mathcal{A}_{ma}$ that satisfies these constraints and achieves the maximum value of V_B^{ref}, we refer to Table 1 and begin with the state of largest $V_i^{forward}$. Adding state 4 to $\mathcal{A}_{ma}$ satisfies the drain-high constraint and the gate-low constraint. We next drop to state 2, which satisfies the constaint that there must be a state with the source and drain both high. Therefore, $\mathcal{A}_{ma}$ = {4, 2} and $(V_B^{ref})_{max} = 3.1V$.

3 Static timing analysis

Transistor-level static timing analysis devolves into a set of constituent CCC simulations. In bulk CMOS, this involves setting the values of all of the inputs of the gate to "sensitize" the delay associated with the switching of one input.[2] In SOI, in addition to established the CCC input values, the body voltages of all of the FETs of the CCC must be initialized.

Modified accessibility analysis can be used to determine the minimum and maximum possible value the reference body voltage can have for each FET of the CCC under analysis. For the given sensitization of the CCC for delay calculation, each FET is in a known state, the minimum or maximum body voltage of which can be determined by a displacement from the reference voltage. These body voltage values are then used as the "initial conditions" for the

[2] We are ignoring the possibility of simultaneously switching inputs.

required delay simulation. For push-pull logic, early-mode calculation for rising transitions sensitizes the nFETs (pFETs) of the pull-up path to be maximum (minimum) and (to reduce the "fight" during switching) the nFETs (pFETs) of the pull-down path to be minimum (maximum). This same sensitization applies to late-mode falling transitions. Early-mode calculation for falling transitions sensitizes the nFETs (pFETs) of the pull-down path to be maximum (minimum) and the nFETs (pFETs) of the pull-dup path to be minimum (maximum). The same sensitization applies to late-mode rising transitions.

As an example, we time the paths through the 4-2 compressor circuit shown in Figure 4 with the prototype transistor-level static timing analyzer described in Reference [15]. We specifically consider the long delay path, I4-Ap-C-D-E-F-S. To compare our static timing results with SPICE, we choose "50% duty cycle" input waveforms for the circuit simulations that sensitize this long path; that is, we keep all of the inputs of the circuit actively switching. Figure 5 compares the cumulative long path delay for rising I4 between SPICE and static timing analysis under full-uncertainty (modified accessibility analysis with no active net tags) and accessibility (modified accessibility analysis with all nets marked active) conditions. A scaled 1-V supply is used for these delay calculations and the technology has a threshold voltage of approximately 0.5 V. This small transistor overdrive (corresponding to low-power operation) emphasizes delay variation with threshold voltage.

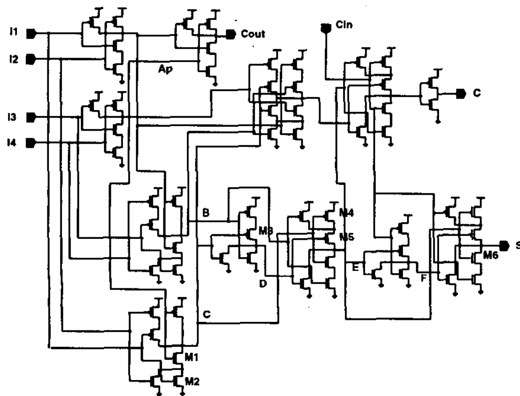

Figure 4: 4-2 compressor circuit

4 Static noise analysis

In addition to verifying the timing of a circuit, one must also perform signal integrity verification. References [18, 9] introduce the idea of transistor-level static noise analysis as a key technology for verifying the functionality of large digital integrated circuits in the presence of noise. The approach involves decomposing the design into a collection of channel-connected components (CCCs), transistors that are connected together through their sources and drains. The maximum noise that is possible on each net is calculated as a time-domain waveshape. This worst-case noise considers all significant noise sources: leakage, charge-sharing noise, coupling though the interconnect, and power-supply noise and is done with a careful choice of vectors on the driving CCCs, the *sensitization*, which produces this worst case noise. Noise can also propagate from CCC-input to CCC-output (*propagated noise*). Noise failures are determined by the *noise stability*, a type of AC noise margin analysis, of each CCC given the worst case noise appear-

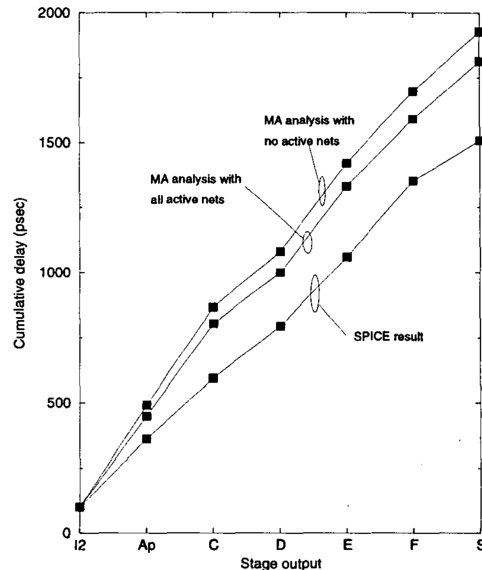

Figure 5: Timing results for the longest path of the 4-2 compressor circuit of Figure 4. SPICE results are compared with static timing analysis using the modified accessibility analysis for body voltage determination.

ing at its inputs. This involves calculating the transient sensitivity of the output noise with respect to the dc-level of the input noise. Here we consider only the special considerations associated with applying static noise analysis to PD-SOI circuits[16] and refer the reader to Reference [9] for more details on static noise analysis generally.

There are two important considerations for static noise analysis for PD-SOI circuits. The first (as for static timing analysis) is that all of the body voltages must be initialized as part of the CCC analysis used to calculate the noise on each node as well as the CCC analysis used to determine the noise stability of the gate. The second is that special consideration must be taken of parasitic bipolar leakage.

The "initial-condition" body voltages are calculated using the modified accessibility analysis described in Section 2. The algorithm for initializing the body voltages is straightforward and depends on the noise type being calculated. Following Reference [15], we calculate two types of noise on each CCC output, V_H noise, which is noise that pulls the output down from the supply level and V_L noise, which is noise that pulls the output up from ground. This noise is then checked against the noise margins of the receiving circuits. When calculating V_H noise on a CCC output (or when verifying noise stability in the case that V_H noise is introduced at the output), all of the devices in the pull-down stack are initialized to maximize the device strength by minimizing threshold voltages (maximum body voltages for nFETs and minimum body voltages for pFETs). This increases the strength of these devices in introducing noise. Similarly, all the devices in the pull-up paths are initialized to minimize device strengths by maximizing threshold voltages (maximum body voltages for pFETs and minimum body voltages for nFETs). This reduces the strength of these devices

in maintaining the output at the logic high level. For V_L noise, the situation is just the opposite, minimizing device strengths in the pull-down stack and maximizing device strengths in the pull-up stack.

In calculating propagated noise and in verifying noise stability, a parasitic bipolar leakage current may also be activated with an associated rapid charging or discharging of the body. Because of this, to achieve the worst-case noise, one must vary the arrival time of the input noise to maximize the output noise; that is, make sure that the noise introduced by parasitic bipolar leakage is superimposing maximally with the propagated noise and that the MOS drain current induced by the propagated noise is maximum (noise on the gate "sees" the most body-affected threshold voltage).

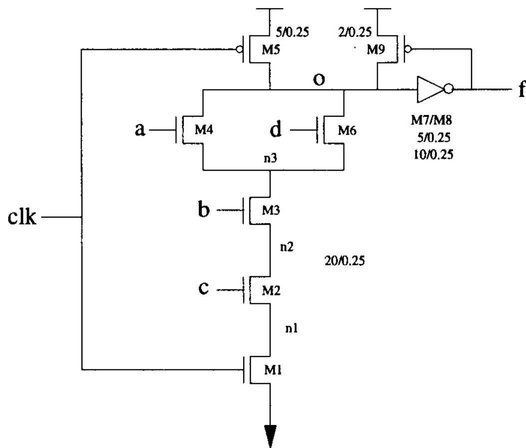

Figure 6: Four-input domino gate.

These "SOI-aware" extensions have been made to the transistor-level static noise analysis tool, Pacific[19]. In Figure 6, we show a sample four-input domino gate analyzed by PacifIC. We assume that input a has the V_L noise shown in Figure 7(a). In the case that only the clock is marked as *active*, PacifIC flags a failure at node o. This worst-case noise occurs as a result of the propagation of V_L noise on a to V_H noise on o (b, c are sensitized high, a, d are sensitized low). The body voltages on *m4* and *m6* are preconditioned to 0.97 V by PacifIC in this case.[3] This failure is indicated by a sensitivity that exceeds unity magnitude in the pull-down network of the domino gate as shown in Figure 8(b). PacifIC generates a "SPICE trace" that can be used to duplicate the conditions producing the noise failure. The result of this simulation is shown in Figure 7. Figure 7(a) shows the voltages on nodes a, o, and f. Figure 7(b) shows the body voltage on transistor *m4* and Figure 7(c) shows the drain current on transistor *m4*.

If, however, a, b, and c are marked as active, PacifIC does not record a failure. The body voltages of transistors *m4* and *m6* are preconditioned in this case to 0.46 V. The worst-case noise reported on node o by PacifIC results from charge-sharing between node o and node n3. Figure 9 shows the noise calculated by PacifIC on nodes o and f and the noise sensitivity recorded for the output inverter.

[3]The node voltage on O always recovers in the PacifIC simulation because the half-latch feedback is broken and the gate of transistor *m9* is held high.

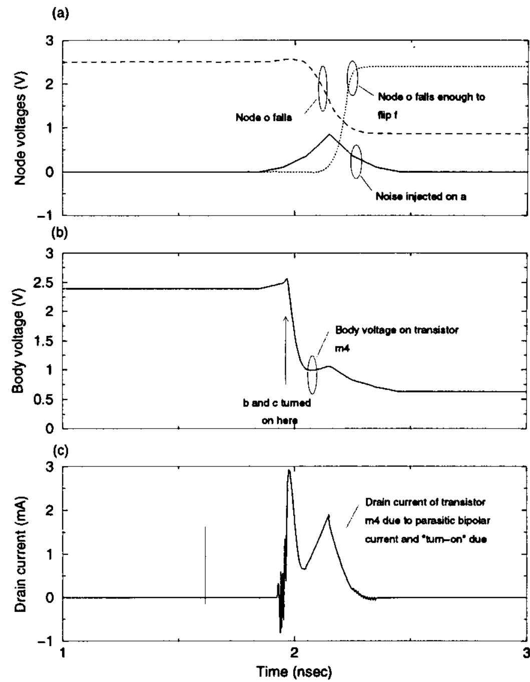

Figure 7: SPICE results using the "SPICE trace" reported by PacifIC for the failure of Figure 8.

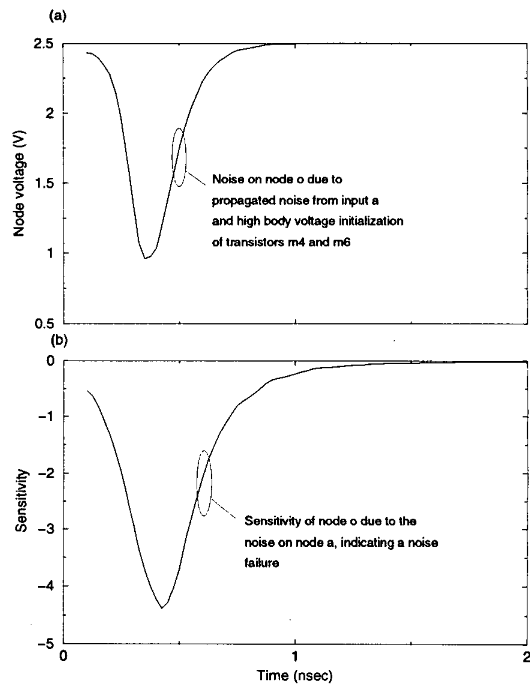

Figure 8: Noise failure for the domino gate of Figure 6, as reported by PacifIC, with only clk marked active. The failure is due to propagated noise from input a and parasitic bipolar leakage.

5 Conclusions

In this paper, we have considered techniques for estimating body-voltage variation in digital PD-SOI circuits. These techniques have then been appleid to transistor-level static timing and static noise analysis tools.

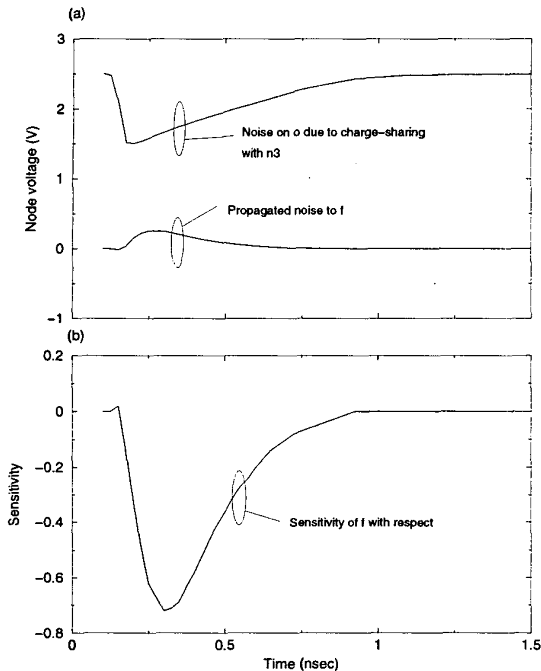

Figure 9: Maximum noise on node o of the domino gate of Figure 6, as reported by PacifIC, with clk, a, b, and c all marked as active. The maximum noise in this case comes from charge-sharing noise and does not produce a failure.

6 Acknowledgement

We gratefully acknowledge the significant contributions of S. Chan and D.-J. Kim to this work. We also acknowledge discussions with C.-T. Chuang, D. Hathaway, F. Assaderaghi, and R. Puri.

References

[1] C. T. Chuang, P.-F. Lu, and C. J. Anderson. SOI for digital CMOS VLSI: Design considerations and advances. *Proceedings of the IEEE*, 86:689 – 720, 1998.

[2] M. Canada et al. A 580MHz RISC microprocessor in SOI. In *Digest Tech. Papers, ISSCC*, pages 430 – 431, 1999.

[3] D. H. Allen et al. A 0.20 μm 1.8 V SOI 550 MHz 64b PowerPC microprocessor with Cu interconnects. In *Digest Tech. Papers, ISSCC*, pages 438 – 439, 1999.

[4] C. T. Chuang and R. Puri. SOI digital CMOS VLSI – a design perspective. In 36th *ACM/IEEE Design Automation Conference*, pages 709 – 714, 1999.

[5] R. Puri and C. T. Chuang. Hysteresis effect in pass-transistor-based partially-depleted SOI CMOS circuits. In *Proceedings of the International SOI Conference*, 1998.

[6] M. M. Pelella, C. T. Chuang, J. G. Fossum, C. Tretz, B. W. Curran, and M. G. Rosenfield. Hysteresis in floating-body PD/SOI circuits. In *Proc. Tech. Papers, Int. Symp. on VLSI Technology, Systems, and Applications, Taipei, Taiwan*, 1999.

[7] Pong-Fei Lu et al. Floating-body effects in partially depleted SOI CMOS cicuits. *IEEE Journal of Solid-State Circuits*, 32(8):1241–1253, August 1997.

[8] N. P. Jouppi. Timing analysis and performance improvement of MOS VLSI designs. *IEEE Trans. CAD*, 6:650 – 665, 1987.

[9] K. L. Shepard, V. Narayanan, and R. Rose. Harmony: Static noise analysis for deep-submicron digital integrated circuits. *IEEE Trans. CAD*, pages 1132–1150, August 1999.

[10] J. Gautier and J. Y.-C. Sun. On the transient operation of partially depleted SOI NMOSFET's. *IEEE Electron Device Letters*, 16:497 – 499, 1995.

[11] J. G. Fossum, R. Sundaresan, and M. Matloubian. Anamalous subthreshold current-voltage characteristics of n-channel SOI MOSFET's. *IEEE Electron Device Letters*, 8:544 – 546, 1987.

[12] H.-K. Lim and J. G. Fossum. Current-voltage characteristics of thin-film SOI MOSFETs in strong inversion. *IEEE Transactions on Electron Devices*, 31(4):401 – 408, 1984.

[13] L. T. Su, D. A. Antoniadis, M. I. Flik, and J. E. Chung. Measurement and modeling of self-heating effects in SOI nMOSFETs. In *Proceedings of the IEDM*, pages 357 – 360, 1992.

[14] L. T. Su, J. B. Jacobs, J. Chung, and D. A. Antoniadis. Deep-submicrometer channel design in silicon-on-insulator (SOI) MOSFETs. *IEEE Electron Device Letters*, 15(5):183 – 185, 1994.

[15] K. L. Shepard and D. Kim. Body-voltage estimation in digital PD-SOI circuits and its application to static timing analysis. In *Proceedings of the IEEE/ACM International Conference on Computer Aided-Design*, pages 531–538, 1999.

[16] K. L. Shepard and D.-J. Kim. Static noise analysis for digital integrated circuits in partially-depleted silicon-on-insulator technology. In *ACM/IEEE Design Automation Conference*, 2000.

[17] S. A. Parke, J. E. Moon, H. C. Wann, P. K. Ko, and C. Hu. Design for suppression of gate-induced drain leakage in LDD MOSFETs using a quasi-two-dimensional analytical model. *IEEE Transactions on Electron Devices*, 39(7):1697 – 1703, 1992.

[18] K. L. Shepard and V. Narayanan. Noise in deep submicron digital design. In *Proceedings of the IEEE/ACM International Conference on Computer-Aided Design*, pages 524–531, San Jose, CA, November 1996.

[19] See http://www.cadmos.com/pacific.htm for datasheets and a sample output report. Technical report.