Static Noise Analysis for Digital Integrated Circuits in Partially Depleted Silicon-on-Insulator Technology

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***Abstract*—This paper extends transistor-level static noise analysis to consider the unique features of partially depleted silicon-on-insulator (PD-SOI) technology: floating-body-induced threshold voltage variations and parasitic bipolar leakage currents. This involves a unique state-diagram abstraction of the device physics determining the body potential of PD-SOI FETs. Based on this picture, a simple model of the body voltage is derived which takes into account modest knowledge of which nets have dependable regular switching activity. Results are presented using a commercial static noise analysis tool incorporating these extensions and comparisons are made with SPICE.**

***Index Terms*—Noise, signal integrity, silicon-on-insulator.**

I. Introduction

PARTIALLY DEPLETED silicon-on-insulator (PD-SOI) has emerged as a leading technology for high-performance low-power deep-submicron digital integrated circuits [1]–[4]. PD-SOI technology delivers two main advantages for digital applications: the reduction of the parasitic capacitance associated with source and drain diffusions and the reduction of the body effect in FET series connections. Acting together, these effects result in faster switching of stack structures in PD-SOI than in bulk CMOS. Because of this improved stack performance, PD-SOI also enables the possibility of greater logic function from a given channel-connected component (CCC), i.e., transistors that are connected together through their sources and drains.

The reduced body effect in stack structures comes about because the body of the transistor is floating. At the device and circuit level, however, this floating-body effect poses major challenges in the successful use of this technology. There is a parasitic bipolar effect which can result in noise failures if not correctly considered [2], [5], [6]. In addition, there can be large uncertainties in the body potential and, consequently, the threshold voltage of devices due to unknown past switching activity. Without special effort in noise analysis, many circuit styles in which noise margin is strongly determined by threshold voltage (e.g., dynamic circuits) could be significantly overdesigned because of conservative body voltage margining. Static noise analysis tools [7], which have become central to the verification of leading-edge digital designs, must be enhanced to understand the unique features of SOI technology. In particular, they must provide accurate bounds on the floating body potentials of the devices from known switching and circuit topology information. These bounds provide the necessary initial conditions for the constituent simulations of the static analysis. Where these bounds are not adequate to prevent overdesign, they should provide options for reducing the potential body voltage variation.

In this paper, we work with BSIMPD [8] models for an IBM partially depleted SOI technology described elsewhere [9]. Devices have a 0.25-μm effective channel length, 5-nm gate oxide, 350-nm buried oxide, and 140-nm thin silicon film.[1] A supply voltage of 2.5 V is used. While the detailed results we present here apply to this technology, the techniques are generally applicable to any PD-SOI technology.

Reference [10] presents techniques for body voltage estimation in PD-SOI circuits and applies them to transistor-level static timing analysis. Reference [7] considers the techniques and methods of transistor-level static noise analysis. In this paper, we combine these approaches in order to address the unique issues of static noise analysis for PD-SOI circuits [11].

The organization of this paper is as follows. In Section II, we review the device physics determining body voltage and parasitic bipolar effects. We do this from the perspective of a circuit-centric state-diagram abstraction introduced in [10]. We consider possible approaches for body voltage estimation, including the techniques discussed in [10], as well as a new approach more suitable for static noise analysis. In Section III, we review the essentials of transistor-level static noise analysis and then consider the special issues associated with noise analysis of PD-SOI circuits: body voltage initialization and parasitic bipolar effects. In Section IV, we compare the results obtained from an SOI-aware commercial static noise analysis tool PacifIC [12] with SPICE. Section V offers conclusions and directions for future work.

II. PD-SOI Device Physics

The body potential of a PD-SOI FET is determined by capacitive coupling of the body to the gate, source, and drain, by diode currents at the source-body and drain-body junctions (including gate-induced drain leakage (GIDL) [13]) and by impact ionization currents produced by current flow through the device (sometimes referred to as the on-state impact ionization

Manuscript received April 4, 2000; revised March 1, 2002. This work was supported in part by the National Science Foundation under Grant CCR-97-34216, by the IBM Corporation, and by Cadence Design Systems, Inc. This paper was recommended by Associate Editor R. Saleh.

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Publisher Item Identifier 10.1109/TCAD.2002.800461.

[1] We modified the device parameters of the model slightly to reduce the impact ionization current at 2.5-V supply. They, therefore, differ slightly from those used in [10].

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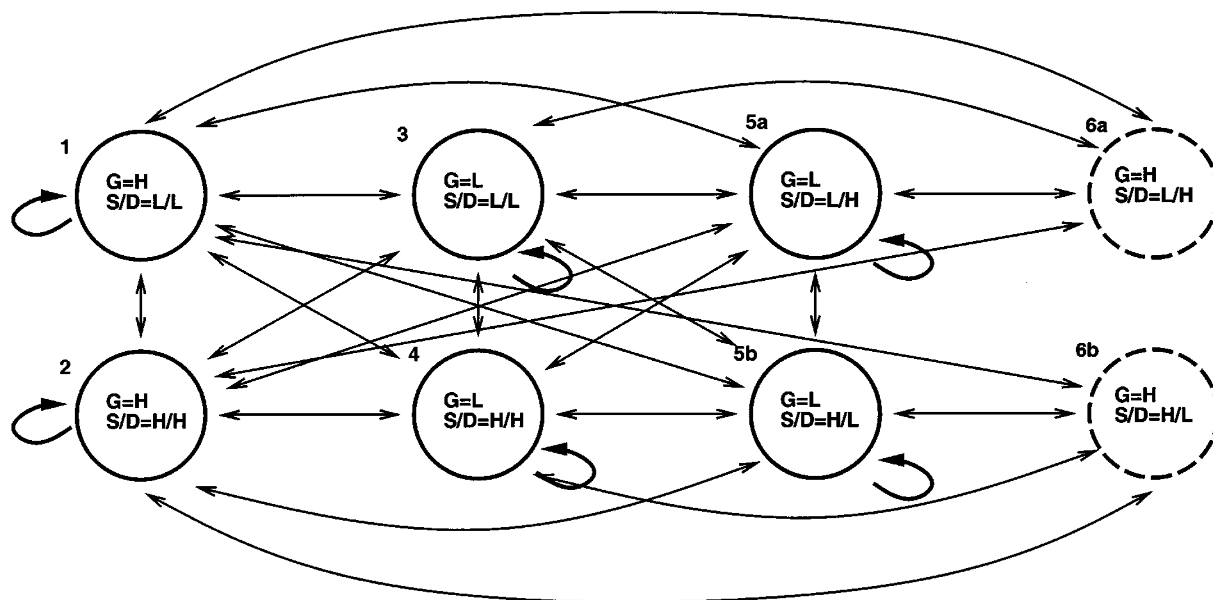

Fig. 1. State diagram for a PD-SOI nFET.

current).[2] Moreover, it is convenient to distinguish "fast" and "slow" processes. Fast processes can change the body potential on time scales on the order of or less than the cycle time, while slow processes require time scales much longer than the cycle time (up to milliseconds) to affect the body voltage. There are two fast mechanisms at work: switching transitions on the gate, source, or drain which are capacitively coupled to the body (which we call *coupling displacements*) and forward-bias diode currents across source-body and drain-body junctions with voltages exceeding the diode turn-on voltage (which we call *body discharge*). The slow processes involve charging or discharging the body through reverse-biased or very weakly forward-biased diode junctions and through impact ionization.

As a (usually) dynamic circuit node, the floating body has memory. To model the switching history determining the body voltage of a particular device, we use the state diagram abstraction shown in Fig. 1 for an nFET. The states denoted with solid circles represent "static" states, states in which the FET can be stable, in contrast with the "dynamic" states 6a and 6b, which are only present transiently during switching events. For example, state 1 corresponds to the case in which the gate is high and both the source and drain are low. Arrows indicate possible state transitions produced by switching events in the circuits containing these FETs. These switching events can represent transitions from the logic state at the end of the previous cycle to the logic state at the end of the current cycle or can represent hazards that occur transiently within a cycle. States 5a and 5b can usually be treated equivalently as state 5; similarly, states 6a and 6b can usually be treated equivalently as state 6. The diagram in Fig. 1 applies only to the nFET. The state diagram of the pFET is the "dual" of this, in which the gate is high rather than low in states 3, 4, and 5 and low rather than high in states 1, 2, and 6.

[2]Gate leakage is an emerging influence on the body voltage in deeply scaled CMOS but will not be considered in this paper.

TABLE I
VALUES OF s_i, V_i^{zero}, AND V_i^{forward} FOR THE NFET AND PFET OF OUR EXAMPLE TECHNOLOGY AT A 2.5-V SUPPLY

i	nfet			pfet		
	s_i	V_i^{zero}	$V_i^{forward}$	s_i	V_i^{zero}	$V_i^{forward}$
1	0	1.78	2.37	0.0	0.0	-0.6
2	2.5	2.50	3.1	2.5	0.736	0.12
3	0	2.16	2.79	0	-0.9315	-0.9505
4	2.5	3.43	3.45	2.5	0.349	-0.275
5	0.421	2.54	2.72	2.079	-0.026	-0.225
6	0.560	1.3	1.36	2.078	1.373	1.15

If the device is allowed to remain in one state for a very long time, the body voltage in each state will achieve a dc value, denoted as s_i. The dc voltages in states 1 and 3 (s_1 and s_3) are zero, while the dc voltages in stages 2 and 4 (s_2 and s_4) are given by the supply voltage. s_5 is determined by the steady-state balance between a weakly forward-biased junction drawing current from the body and a reverse-biased junction, leaking current to the body, enhanced by GIDL currents. Similarly, s_6 is determined by the steady-state balance between a weakly forward-biased junction drawing current from the body and charging current due to reverse leakage of the other diode junction and on-state impact ionization. These values of s_i are shown for our example technology in Table I.

In the absence of body discharge, the coupling displacements that occur with each transition in Fig. 1 are completely reversible on "fast" time scales; that is, if one begins in state 1 and traverses the state diagram, returning to state 1 on a time scale much faster than any of the "slow" leakage mechanisms, the body voltage on return will be the same as the initial body voltage, a simple result of charge conservation. We can therefore represent the charge stored on the body as the value of the body voltage in one particular state, called the *reference state*. We choose state 2 for the nFET and state 1 for the pFET to be this reference state and denote the body voltage in these

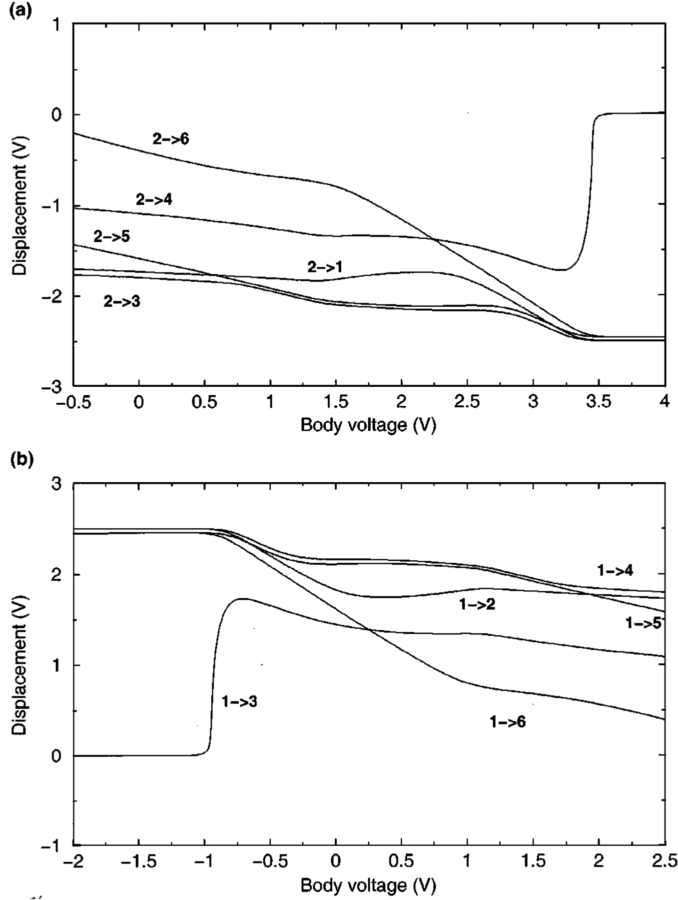

Fig. 2. Displacements as a function of reference state body voltage at a 2.5-V supply for (a) the nFET, for which the reference state is state 2 and (b) the pFET, for which the reference state is state 1.

two states as V_B^{ref}. For any nonreference state i, the body voltage V_B^i can be determined according to the following:

$$V_B^i = V_B^{\text{ref}} + d_i\left(V_B^{\text{ref}}\right). \quad (1)$$

The displacements, $d_i(V_B^{\text{ref}})$, are explicitly shown to be dependent on the reference body voltage because of the strong voltage dependence of the source-body, drain-body, and gate-body capacitances. Fig. 2 shows these displacements as a function of V_B^{ref} for our example technology.

With the reference body voltage as a "state-independent" way of representing the charge trapped on the body, we proceed to characterize each state i in Fig. 1 by two values of the reference body voltage, V_i^{zero} and V_i^{forward}, shown in Table I for our example technology. V_i^{zero} represents the steady-state value of the reference body voltage, achieved by remaining in state i for a long time. From (1) and the definitions of s_i, V_i^{zero}, and d_i, the following relation holds:

$$s_i = V_i^{\text{zero}} + d_i\left(V_i^{\text{zero}}\right). \quad (2)$$

For example, consider an nFET in state 4, where Table I shows that $V_4^{\text{zero}} = 3.43$ V. From Fig. 2, we see that for the $2 \rightarrow 4$ transition, a reference body voltage of 3.43 V will result in $d_4(3.43) = -0.93$ V. Equation (2) confirms that $s_4 = 2.5$ V since $V_4^{\text{zero}} + d_4(V_4^{\text{zero}}) = 3.43 - 0.93 = 2.5$ V.

V_i^{forward} represents the value of the reference body voltage for the nFET (pFET) to which the body would be very quickly pulled down (up) as a result of body discharge (charge), if state i were accessed with a higher (lower) reference body voltage than V_i^{forward}. The values shown in Table I for our example technology presume that the fast body discharge will bring the forward-biased-junction bias down to a turn-on voltage of 0.6 V. It is important to note that fast body discharge can trigger parasitic bipolar leakage between source and drain for FETs in state 5. This means, for example, that if an nFET which reached a dc steady state in state 4 (with a V_4^{zero} of 3.43 V) switches into state 2, the reference body voltage will quickly discharge to $V_2^{\text{forward}} = 3.1$ V. If the FET subsequently remains in state 2 for a long time, V_B^{ref} will eventually decrease to $V_2^{\text{zero}} = 2.5$ V.

The V_i^{forward} values in Table I are determined in a similar way as the V_i^{zero} values. For example, an nFET in state 4 has source and drain high, so no source body or drain body junction will be strongly forward biased if the body voltage remains below 3.1 V. From Fig. 2, we see that if $V_B^{\text{ref}} = 3.45$ V then $d_4(3.45) = -0.35$ V. And so by (1), $V_4^{\text{forward}} = 3.1 - (-0.35) = 3.45$ V.

Reference [10] uses the information in Table I to provide two modes of body voltage estimation. In "full uncertainty" analysis, we assume that we have no knowledge of the switching activity of the circuit. We must choose maximum and minimum possible values of the body voltage that cover all possible stimulus and history. We say that a state is *accessible* if the circuit topology allows the state to be visited. For example, for the nFET of an inverter, those states with the source high would not be accessible because the source of the nFET is tied to ground. We let $\mathcal{A}$ represent the set of such accessible states, including possibly the dynamic state 6. In this case, the minimum and maximum body voltages are given by

$$\left(V_B^{\text{ref}}\right)_{\max} = \max_{j\in\mathcal{A}} V_j^{\text{zero}} \quad (3)$$

$$\left(V_B^{\text{ref}}\right)_{\min} = \min_{j\in\mathcal{A}} V_j^{\text{zero}}. \quad (4)$$

If, however, one is assured that every accessible state is visited with reasonable frequency (i.e., on a time scale that is faster than the "slow" body voltage mechanism), then the V_j^{forward} values for the nFET (pFET) will cap the maximum (minimum) possible value of the body voltage. For example, suppose that the set of accessible states for an nFET are 1, 3, and 5. If these states are visited with reasonable frequency, $(V_B^{\text{ref}})_{\max}$ will be limited to 2.37 V by V_1^{forward} since the body will be discharged to 2.37 V each time state 1 is entered. For the nFET then

$$\left(V_B^{\text{ref}}\right)_{\min} = \min_{j\in\mathcal{A}} V_j^{\text{zero}} \quad (5)$$

$$\left(V_B^{\text{ref}}\right)_{\max} = \min\left(\max_{j\in\mathcal{A}} V_j^{\text{zero}},\ \min_{j\in\mathcal{A}_{\text{static}}} V_j^{\text{forward}}\right) \quad (6)$$

while for the pFET

$$\left(V_B^{\text{ref}}\right)_{\min} = \max\left(\min_{j\in\mathcal{A}} V_j^{\text{zero}},\ \max_{j\in\mathcal{A}_{\text{static}}} V_j^{\text{forward}}\right) \quad (7)$$

$$\left(V_B^{\text{ref}}\right)_{\max} = \max_{j\in\mathcal{A}} V_j^{\text{zero}} \quad (8)$$

where $\mathcal{A}_{\text{static}}$ is the set of all accessible *static* states (i.e., states 1–5). State 6 is not included because it is visited only briefly

during a transition and cannot be assured to be active long enough to complete a discharge. Body voltage estimation using (5)–(8) is referred to as "accessibility" analysis. Reference [10] shows how it is possible to refine accessibility analysis even further with stochastic techniques. This requires more detailed knowledge of signal timing and probabilities, which are difficult to obtain and assure in the context of noise analysis.

While accessibility analysis does not require detailed switching knowledge, it does require that there is enough switching activity that every accessible state is visited with a minimum frequency. At times, this, too, may be difficult to ensure. We, therefore, propose a *modified accessibility analysis* that we will apply in the context of static noise analysis. In this approach, signals in the design can be marked as *active*. This means that these particular signals are assured to switch with regular frequency. The clock net is one immediately obvious active net. We then use these active net tags to come up with a set of constraints (*active-net constraints*) that must be satisfied by a modified accessibility set of states $\mathcal{A}_{\rm ma}$. The body voltage will then be determined by equations identical to those used for accessibility analysis except that $\mathcal{A}_{\rm static}$ is replaced by $\mathcal{A}_{\rm ma}$. For the nFET

$$\left(V_B^{\rm ref}\right)_{\rm min} = \min_{j\in\mathcal{A}} V_j^{\rm zero} \tag{9}$$

$$\left(V_B^{\rm ref}\right)_{\rm max} = \min\left(\max_{j\in\mathcal{A}} V_j^{\rm zero},\ \min_{j\in\mathcal{A}_{\rm ma}} V_j^{\rm forward}\right) \tag{10}$$

while for the pFET

$$\left(V_B^{\rm ref}\right)_{\rm min} = \max\left(\min_{j\in\mathcal{A}} V_j^{\rm zero},\ \max_{j\in\mathcal{A}_{\rm ma}} V_j^{\rm forward}\right) \tag{11}$$

$$\left(V_B^{\rm ref}\right)_{\rm max} = \max_{j\in\mathcal{A}} V_j^{\rm zero}. \tag{12}$$

$\mathcal{A}_{\rm ma}$ will be the accessibility set for the nFET (pFET) which satisfies the active-net constraints while ensuring the maximum (minimum) value of the body voltage. As in accessibility analysis, modified accessibility analysis explicitly excludes the dynamic state 6 from $\mathcal{A}_{\rm ma}$.

These active-net constraints on $\mathcal{A}_{\rm ma}$ are derived from the following rules.

- If the gate of the FET is an active net, then there must be a state in $\mathcal{A}_{\rm ma}$ with the gate high and a state in $\mathcal{A}_{\rm ma}$ with the gate low.We demonstrate modified accessibility analysis with the example shown in Fig. 3. Nets C and B (marked with the arrows) are active nets. For transistor $M1$, therefore, there must be a state in $\mathcal{A}_{\rm ma}$ with the source and gate both high, with the gate low, and with the drain high. To find $\mathcal{A}_{\rm ma}$ that satisfies these constraints and achieves the maximum value of $V_B^{\rm ref}$, we refer to Table I and begin with the state of largest $V_i^{\rm forward}$. Adding state 4 to $\mathcal{A}_{\rm ma}$ satisfies the drain-high constraint and the gate-low constraint. We next drop to state 2, which satisfies the constraint that there must be a state with the source and drain both high. Therefore, $\mathcal{A}_{\rm ma} = \{4, 2\}$ and $(V_B^{\rm ref})_{\rm max} = 3.1$ V.
- If the source of the FET is connected to ground (supply) through a succession of transistors all of whose gates are active nets, then $\mathcal{A}_{\rm ma}$ must contain a state with the source low (high).

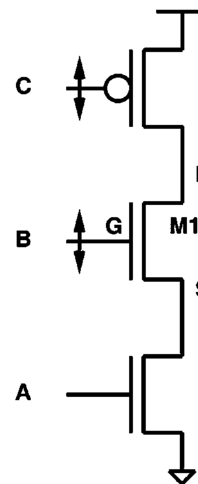

Fig. 3. Example to demonstrate modified accessibility analysis.

- If the drain of the FET is connected to ground (supply) through a succession of transistors all of whose gates are active nets, then $\mathcal{A}_{\rm ma}$ must contain a state with the drain low (high).
- Same-signal correlations must be considered and can result in stronger constraints. For example, if gate of the current FET is marked as an active net, but must be high for a path to ground from the source to be present through a path of active-gate FETs, then $\mathcal{A}_{\rm ma}$ must contain a state in which both the gate is high and the source is low.

III. Static Noise Analysis

References [7], [14] introduce the idea of transistor-level static noise analysis as a key technology for verifying the functionality of large digital integrated circuits in the presence of noise. The approach involves decomposing the design into a collection of CCCs. The maximum noise that is possible on each net is calculated as a time-domain waveshape. This *worst case noise analysis* considers all possible noise sources: leakage, charge-sharing noise, coupling through the interconnect, and power-supply noise. This is done with a careful choice of vectors on the driving CCCs, referred to as the *sensitization*, which produces this worst case noise. Noise can also propagate from the output of one CCC to the input of the following CCC (*propagated noise*).

Noise failures are determined by the *noise stability*, a type of ac noise margin analysis, of each CCC given the worst case noise appearing at its inputs. This involves calculating the transient sensitivity of the output noise with respect to the dc level of the input noise, as shown for an inverter in Fig. 4. The noise $v_{\rm in}(t)$ "biases" the inverter, producing an output waveform $v_{\rm out}(t)$. The time-domain dc-noise sensitivity $S(t)$ is given by

$$S(t) = \left.\frac{\partial v_{\rm out}(t)}{\partial V_{\rm dc}}\right|_{V_{\rm dc}=0}. \tag{13}$$

This sensitivity examines the subsequent amplification of additional fluctuations of the lowest possible frequency content (i.e., purely dc). If the magnitude of $S(t)$ ever exceeds one, then the

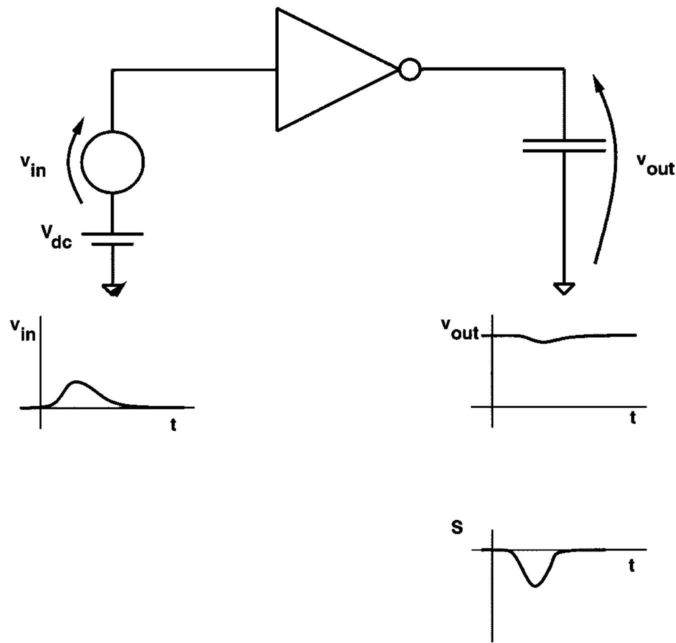

Fig. 4. Calculating the dc-noise sensitivity for a CMOS inverter. $v_{\rm in}(t)$ on the input propagates to $v_{\rm out}(t)$ on the output. The dc-noise sensitivity $S(t)$ is negative because the gate is inverting. When the magnitude of the sensitivity is greater than one, the gate is noise unstable.

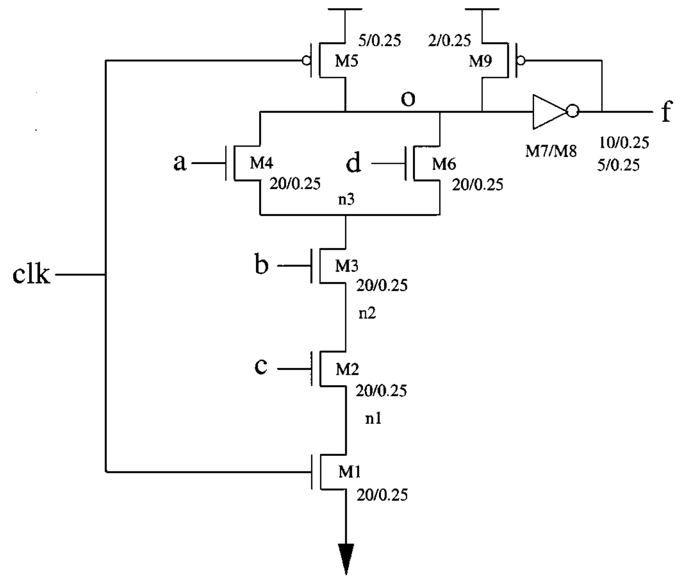

Fig. 5. A four-input domino gate which exhibits parasitic bipolar noise on node o due to the body of FET M4 floating high.

gate is noise unstable, and the associated $v_{\rm in}(t)$ violates the dynamic noise margins of the gate. The basis for this metric is to prevent any feedback configuration of restoring logic gates (i.e., a latch) from being biased by noise to have a loop gain greater than one and, therefore, to switch to an erroneous value. Because it is a condition applied to every restoring logic gate, rather than to just latches, it is conservative. We will demonstrate this more in the examples of Section IV.[3] In this paper, we wish to consider only the special considerations associated with applying static noise analysis to PD-SOI circuits and refer the reader to [7] for more details on the noise stability metric and static noise analysis.

There are two important considerations in static noise analysis for PD-SOI circuits. The first is that all of the body voltages must be initialized as part of each CCC analysis. And second, special considerations have to be made for potential parasitic bipolar leakage.

A. Body Voltages Initialization

Body voltage initialization must be part of the sensitization for all CCCs analyzed since the transistor bodies are, in general, floating nodes and hold state. For the given sensitization of a CCC, each FET is in a known state (the *target state*). The target state body voltage of the FET can be determined by the displacement [see (1)] from the reference body voltage. These body voltages are then used as the initial conditions for the required noise simulations.

Additional heuristics guide whether the minimum or maximum value is used for each FET. Following [7], we calculate two types of noise on each CCC output, V_H noise, which is noise that pulls the output down from the supply level, and V_L noise, which is noise that pulls the output up from ground. When calculating V_H noise on a CCC output, all the devices in the pull-up paths are initialized to minimize device strengths by maximizing threshold voltages (minimum body voltages for nFETs and maximum body voltages for pFETs). This reduces the strength of these devices in maintaining the output at the logic high level. All of the devices in the pull-down paths are initialized to maximize the device strength by minimizing threshold voltages (maximum body voltages for nFETs and minimum body voltages for pFETs). This increases the strength of these devices in introducing noise. The situation is just the opposite for V_L noise. Devices in the pull-down paths are weakened (minimum body voltages for nFETs and maximum body voltages for pFETs), while devices in the pull-up paths are strengthened (maximum body voltages for nFETs and minimum body voltages for pFETs).

Although this simple heuristic works well in nearly all cases, there are situations that require more detailed analysis. For example, pass transistors are problematic since they are in both the pull-up and pull-down paths. In these cases, both minimum and maximum strength possibilities must be tried in order to determine the worst case noise.

B. Parasitic Bipolar Noise

As reported in the literature [2], [5], [6], PD-SOI FETs are susceptible to transient parasitic bipolar currents. The impact of this parasitic bipolar noise on various circuit families is discussed in [5] and [6]. Reference [2] reports a functional failure, uncovered during the remapping of a RISC microprocessor to an SOI technology, due to parasitic bipolar noise propagating from one stage in a dynamic adder to the following stages, with each stage contributing its own bipolar noise.

In order to illustrate the parasitic bipolar effect, consider the four-input domino gate shown in Fig. 5. If transistor M4 is off, its body can easily float to a high potential when: 1) dynamic

[3]It is possible to propagate noise to latches and to check stability only at latches. While this feature is implemented in the commercial static noise analysis tool we use, we will not consider it further in this paper.

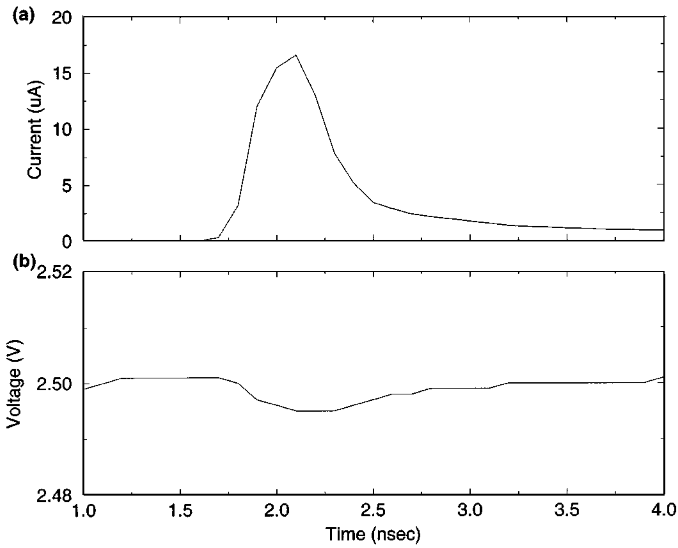

Fig. 6. (a) Parasitic bipolar current flows through FET M4 from Fig. 5 and (b) results in V_H noise on output node o.

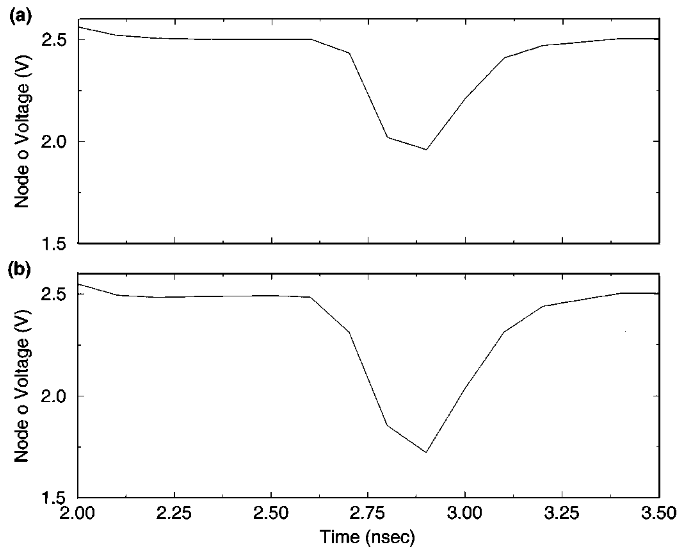

Fig. 7. (a) Propagated noise acting alone and (b) propagated noise superimposed with parasitic bipolar noise on FET M4 from Fig. 5.

node o is high; 2) transistor M6 is on; and 3) at least one of the transistors in the rest of the pull down stack is off. If node $n3$ is subsequently pulled down to ground with M4 and M6 off, a transient parasitic bipolar current flows through M4. Fig. 6(a) shows the parasitic bipolar current that results (device sizes are shown in Fig. 5). The V_H noise that results on node o is shown in Fig. 6(b).

A far more serious noise concern, however, is when parasitic bipolar noise is acting on a FET with propagated noise on its input, as was reported in the case of the adder failure in [2]. In these situations, the output is more sensitive to the propagated noise because of the reduced threshold voltage of the input FET. Since parasitic bipolar leakage current is present here as well, noise failures become a real possibility. The example circuit from Fig. 5 can be used to show more clearly the effect when these two noise sources are acting together.

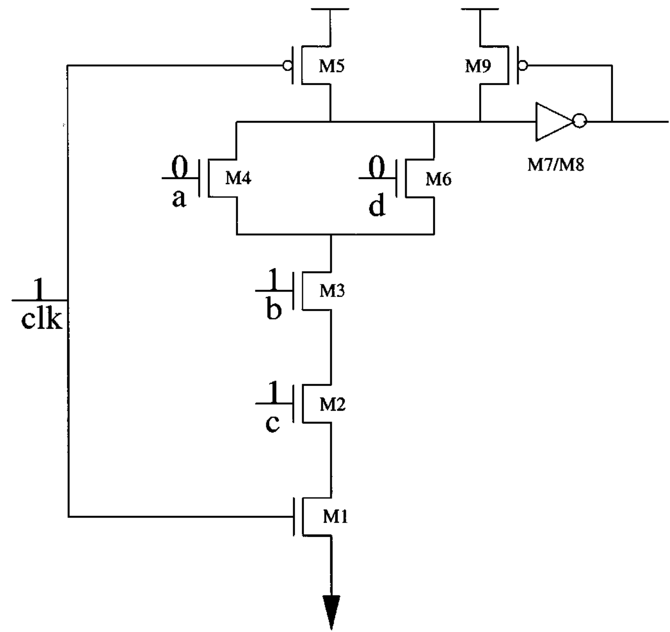

Fig. 8. The same vector is used in static noise analysis to sensitize for propagated noise on node a and for parasitic bipolar noise from FET M4.

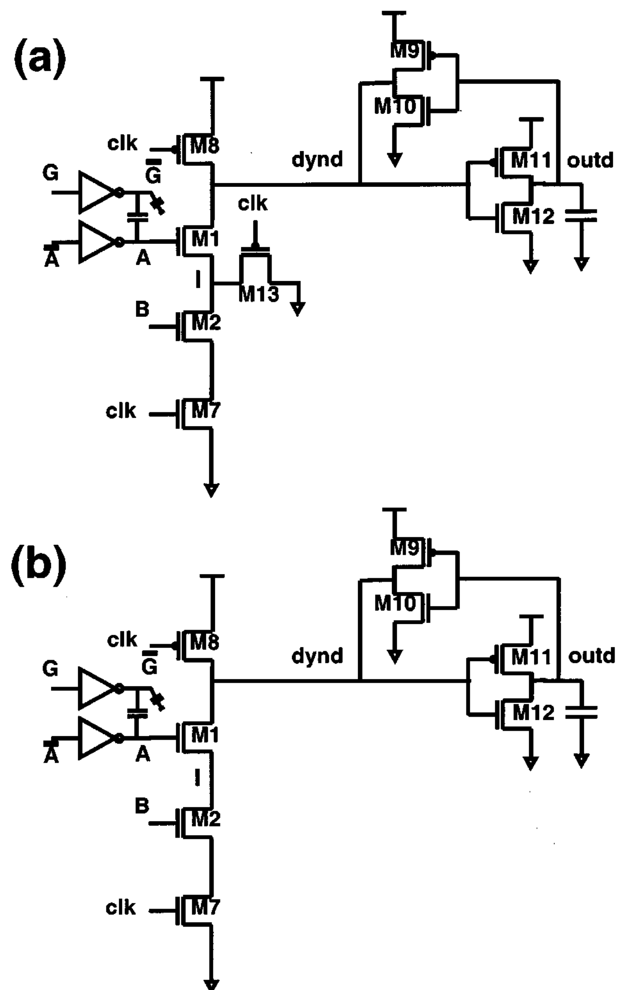

Fig. 9. Two circuit examples: (a) domino gate with predischarge FET on the internal node of pull-down stack and (b) domino gate with no predischarge FET.

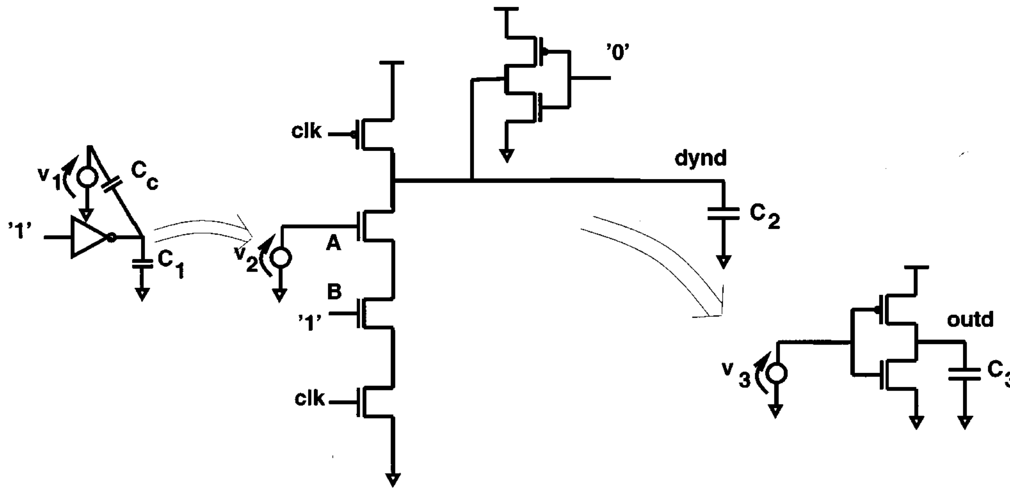

Fig. 10. CCC decomposition used for static noise analysis of the circuit in Fig. 9.

Suppose V_L propagated noise appears on net a. Fig. 7 shows how this propagated noise affects output node o under two different conditions: when transistor M4's body voltage is initialized to ground [Fig. 7(a)] and when the body voltage is initialized to $V_{\rm dd}$ [Fig. 7(b)]. The noise is much worse when the body is initialized to $V_{\rm dd}$ due to parasitic bipolar leakage current and reduced FET threshold voltage.

The sensitization vector used in static noise analysis for propagated noise and parasitic bipolar noise is always the same. Fig. 8 shows the vector used to sensitize for the propagated and the bipolar noise shown in Fig. 7(b). Since the sensitization vectors are always the same, combined analysis requires no special effort on the part the analyzer (i.e., when propagated noise is being sensitized, any parasitic bipolar noise present will be sensitized for as well). Note that in order to achieve the worst case effects, as is required in static noise analysis, the arrival time of the propagated noise must be adjusted to maximize the output noise. That is, the noise introduced by parasitic bipolar leakage must be superimposed maximally with the propagated noise.

IV. Results

We have applied SOI enhancements to a commercial static noise analysis tool, PacifIC, that is currently being used for bulk CMOS designs. We focus our results on the two domino circuits shown in Fig. 9. These simple examples illustrate most of the PD-SOI specific noise analysis issues and allow tractable validation of the results against SPICE. Note that although domino gates typically have their dynamic nodes held by a half latch rather than a full latch, the latter is used here because it creates an unambiguous failure criterion for the circuits in SPICE simulation, the switching of the latch. The two circuits in Fig. 9 differ only in that a predischarge FET is present in the top circuit.

A. Initialization

Each static noise analysis run begins with a quick technology characterization in which $V_i^{\rm zero}$ and $V_i^{\rm forward}$ are calculated for each state, for every unique transistor model. These values are then used to determine the maximum and minimum reference body voltages for each transistor. Later, during noise analysis simulation, reference body voltages are translated using (1) to target state body voltages. In many cases, these target state body voltages are not easily determined with direct simulation of a transition from the reference state. For example, reference body voltages for an nFET greater than about 3.1 V would result in strongly forward-biased body drain and body source junctions, making it difficult to distinguish between the displacements due to the transition from state 2 and the body discharge. As a result, target state body voltages are instead determined by isolated evaluation of the MOS C–V model (i.e., no charge loss from the body is allowed). The overhead required to characterize a technology, including translating reference body voltages to target state body voltages, is extremely small compared to the total static noise analysis run time. For test cases on the order of 100 000 FETs, less than 5% of the simulations are due to SOI related technology characterization.

TABLE II
Active Net Tagging and Circuit Used for Cases 1–6

Case	Circuit	Net tagging		
		clk	A	B
1	Figure 9(a)	-	-	-
2	Figure 9(a)	active	-	-
3	Figure 9(a)	active	active	-
4	Figure 9(b)	active	-	-
5	Figure 9(b)	active	active	-
6	Figure 9(b)	active	active	active

Fig. 10 shows how static noise analysis decomposes the circuit of Fig. 9 into three CCCs. As part of this decomposition, the (linearized) gate capacitance of the subsequent stage is included in capacitors C_1 and C_2. In this case, we show the propagation of coupling noise on A to $\rm dynd$ and subsequently to $\rm outd$. The action of the switching aggressor G is modeled as an ideal saturated-ramp voltage source, v_1, acting through the coupling capacitance on node A. The V_L noise calculated across C_1 is then applied to the next stage through the action of voltage source v_2. Similarly, the V_H noise calculated on $\rm dynd$ is propagated to the next stage through the action of voltage source v_3. The feedback path from $\rm outd$ to $\rm dynd$ through the $M9$–$M10$ inverter is broken as part of the CCC decomposition. This is an acceptable

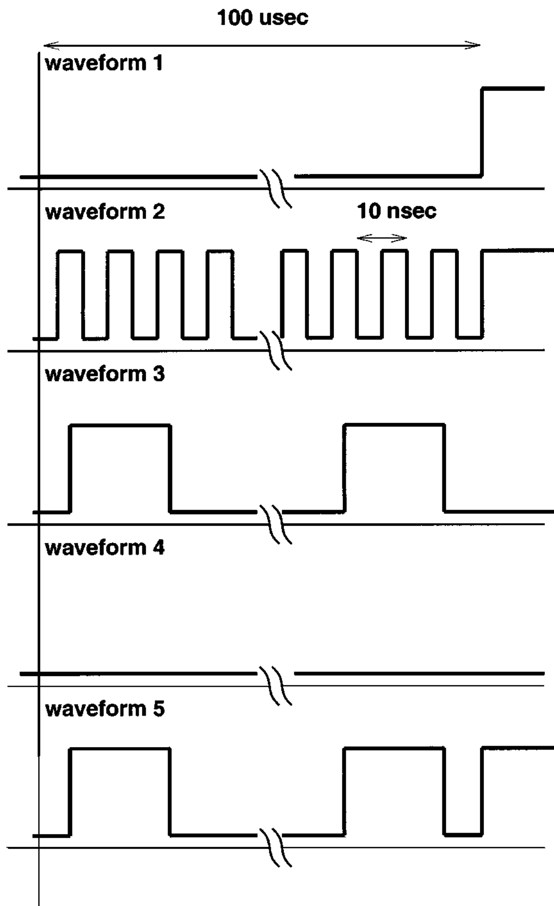

Fig. 11. Waveforms applied for SPICE simulation.

TABLE III
WAVEFORMS FROM FIG. 11 USED FOR SPICE SIMULATIONS

Case	waveform: clk	A	B
1 (active: none)	1	4	1
2 (active: clk)	2	4	1
3 (active: clk A)	2	3	1
4 (active: clk)	2	4	1
5 (active: clk A)	2	3	1
6 (active: clk A B)	2	3	5

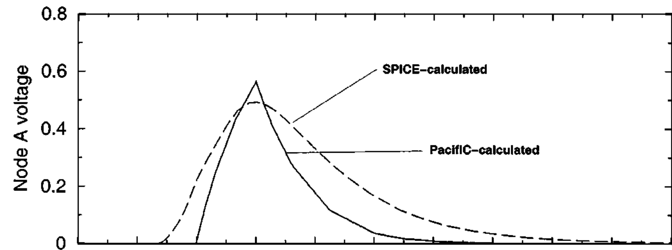

Fig. 12. V_L coupling noise on A due to switching of G for $C_c = 55$ fF.

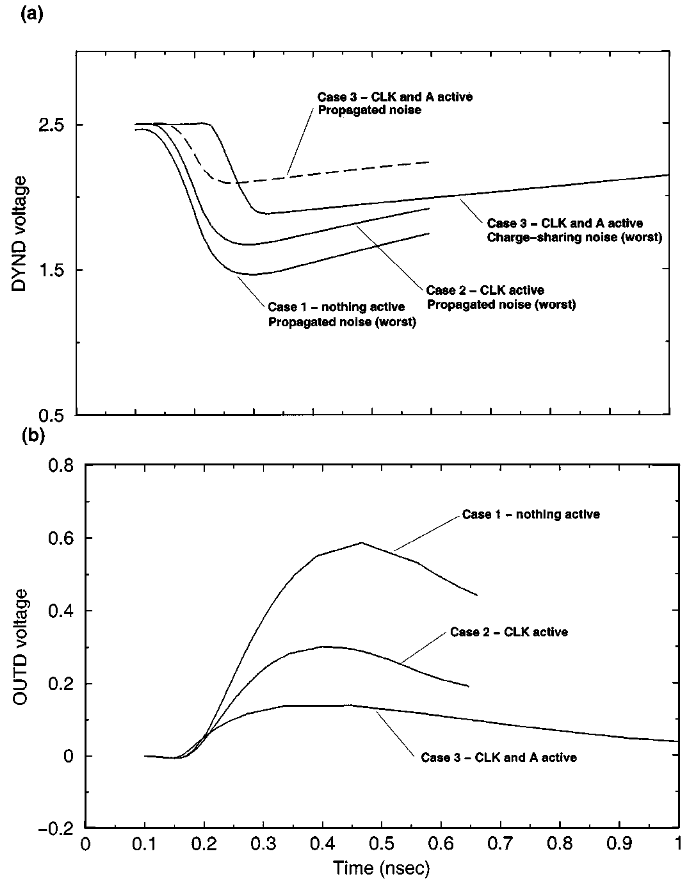

Fig. 13. Noise on net (a) dynd and (b) outd as calculated by static noise analysis for Cases 1–3.

simplification because the V_L noise on outd never grows large enough (without producing a failure) to significantly impact the V_H noise calculation on dynd through the reduced holding strength of $M9$. The reader is referred to [7] for more discussion of the static noise analysis techniques. Direct sensitivity calculation required for evaluation of (13) is supported natively in the noise-analysis circuit simulation engine.

Table II outlines six different static noise analysis runs done with the two circuits of Fig. 9 under different active net tagging conditions. In Case 1, the circuit of Fig. 9(a) is run with no active net tags, tantamount to "full uncertainty" body-voltage estimation. In all the other cases, some active net tagging is employed to reduce the pessimism in the body-voltage initial conditions. Case 6, which has all the nets of the "main" CCC of the domino gate marked active, is tantamount to "full accessibility" body voltage estimation.

Cases 1–6 from Table II are reproduced in SPICE by applying vectors which attempt to mimic the specified net activities for each case. For example, Case 3 shows clk and A as active. Therefore, in our SPICE simulation for Case 3, we include a "prelude" where nets clk and A are switched with regularity. A 100-μs prelude is used in all cases so that the body voltage of each transistor may reach steady state.

Fig. 11 shows the set of waveforms to which we may assign to each net in the circuit. Waveform 1 is used for clk not active and waveform 2 is used for clk active. Note that the clock period is 10 ns. Waveforms 3 and 5 are used for A and B active, respectively (both have a $0 \rightarrow 1$ transition every other clock cycle). Waveforms 4 and 1 are used for A and B not active, respectively. Table III shows the waveform assignments used for each of the six cases from Table II.

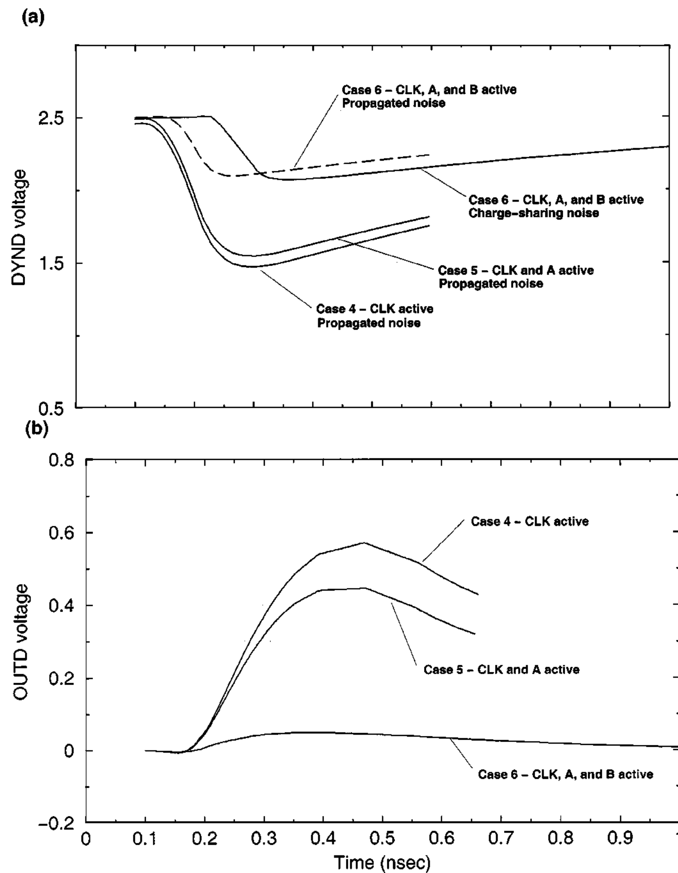

Fig. 14. Noise on net (a) dynd and (b) outd as calculated by static noise analysis for Cases 4–6.

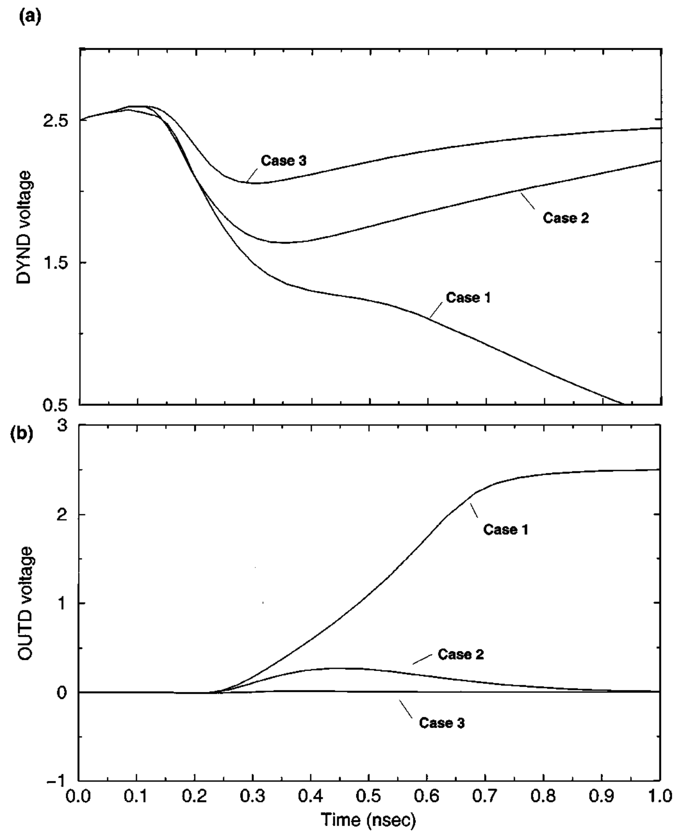

Fig. 15. Noise on net (a) dynd and (b) outd as calculated by SPICE for Cases 1–3.

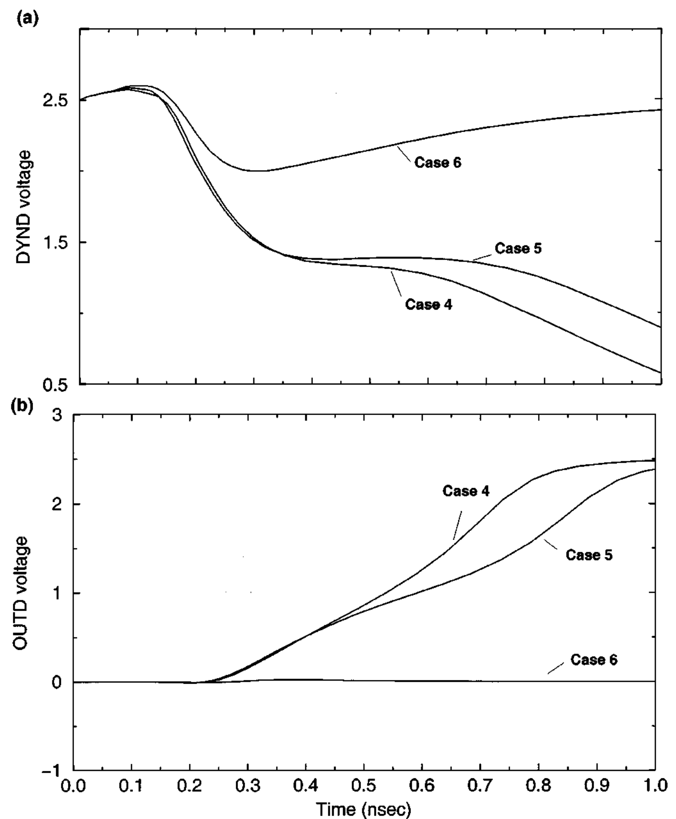

Fig. 16. Noise on net (a) dynd and (b) outd as calculated by SPICE for Cases 4–6.

After each prelude, B is set high, A is set low, and clk is set high so that V_L coupling noise may be introduced on A by the switching of G. The V_L coupling noise on A as calculated by static noise analysis is shown in Fig. 12 for $C_c = 55$ fF. The actual coupled noise on A calculated by SPICE is shown as a dashed curve. The two waveforms differ slightly because in static noise analysis, aggressors are modeled as saturated-ramp voltage sources. The differences are minor enough so that comparison of body voltages, peak noise values, and stability can still be made between SPICE and static noise analysis.

B. Peak Noise and Stability

The noise waveforms obtained from static noise analysis and SPICE are shown in Figs. 13–16. Fig. 13 shows Cases 1–3 and Fig. 14 shows Cases 4–6 for static noise analysis. Figs. 15 and 16 show SPICE results for Cases 1–3 and 4–6, respectively. Both the noise on the dynamic node, dynd, and the noise at the gate output node, outd, are shown.

For Cases 1, 2, 4, and 5, the peak noise on dynd occurs when coupling from net A propagates to dynd. For Cases 3 and 6, however, the peak noise on dynd is due to charge sharing from the switching of A. The propagated noise for Case 3 and 6 is shown as a dashed curve in Figs. 13(a) and 14(a) for reference (the SPICE results for Case 3 and 6 are from charge sharing noise). In Cases 1 and 4, a small, but not negligible, component of the V_H noise on dynd is due to parasitic bipolar current.

TABLE IV
PEAK NOISE FROM STATIC NOISE ANALYSIS AND SPICE

Method	Case	Net	Peak (V)
Static noise analysis	1	*dynd*	1.04
SPICE	1	*dynd*	1.15
Static noise analysis	1	*outd*	0.59
SPICE	1	*outd*	0.57
Static noise analysis	2	*dynd*	0.83
SPICE	2	*dynd*	0.87
Static noise analysis	2	*outd*	0.30
SPICE	2	*outd*	0.27
Static noise analysis	3	*dynd*	0.617
SPICE	3	*dynd*	0.45
Static noise analysis	3	*outd*	0.14
SPICE	3	*outd*	0.10
Static noise analysis	4	*dynd*	0.43
SPICE	4	*dynd*	0.50
Static noise analysis	4	*outd*	0.57
SPICE	4	*outd*	0.47
Static noise analysis	5	*dynd*	0.96
SPICE	5	*dynd*	0.98
Static noise analysis	5	*outd*	0.45
SPICE	5	*outd*	0.46
Static noise analysis	6	*dynd*	1.03
SPICE	6	*dynd*	0.97
Static noise analysis	6	*outd*	0.049
SPICE	6	*outd*	0.023

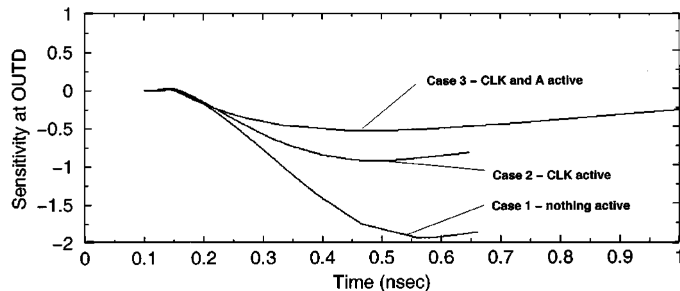

Fig. 17. The sensitivity, as determined by static noise analysis, of node outd with respect to the noise appearing on node dynd for Cases 1–3.

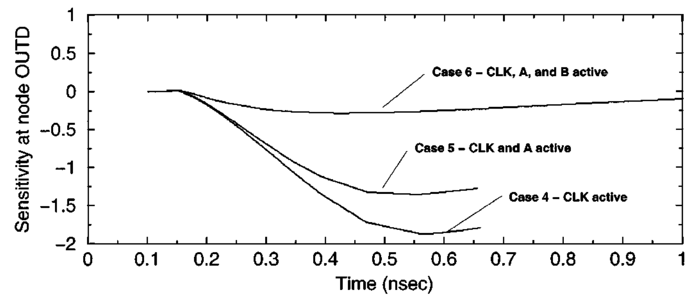

Fig. 18. The sensitivity, as determined by static noise analysis, of node outd with respect to the noise appearing on node dynd for Cases 4–6.

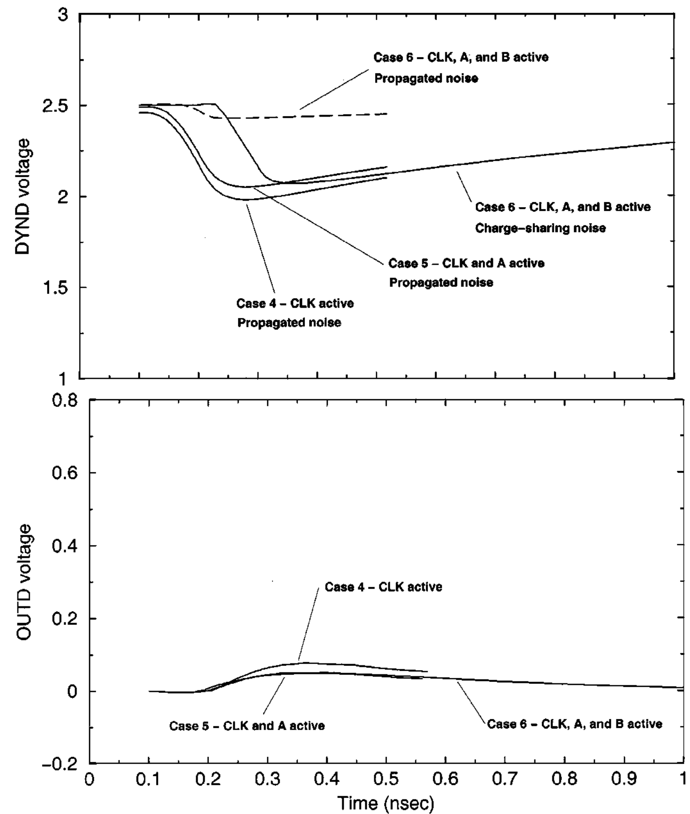

Fig. 19. Noise on net (a) dynd and (b) outd as calculated by static noise analysis for Cases 4–6, when the coupling capacitance on net A has been reduced.

Comparing static noise analysis and SPICE (Figs. 13 versus 15 and Figs. 14 versus 16), we see good agreement in the noise waveforms. However, in Cases 1, 4, and 5, the latch switches in SPICE simulation, but since the feedback path is broken in static noise analysis, the waveforms differ once the noise on dynd exceeds the switching threshold of the latch.[4] Peak noise values (i.e., maximum deviation from nominal supply or ground) are tabulated for each waveform in Table IV. There exists a range of differences between static noise analysis and SPICE, but they typically are less than 10%.[5] Since PacifIC has a SPICE-based simulation engine and uses the same BSIMPD models as SPICE, the difference in Table IV is mainly due to slight variations in initial body voltages (discussed later) and simplifications made in static noise analysis, such as linearization of gate capacitances of fanout transistors, diffusion capacitance of "off" transistors, and the modeling of aggressors as saturated-ramp voltage sources.

Static noise analysis propagates the worst case noise calculated on dynd to outd (see Fig. 10). The noise stability of this gate determines whether PacifIC flags a noise violation. A plot of the sensitivity of this propagated noise on outd is shown in Fig. 17 for Cases 1–3 and in Fig. 18 for Cases 4–6. In Cases 1, 4, and 5, outd is driven unstable by the propagated noise since the magnitude of the sensitivity is greater than one. SPICE simulations confirm instability, as indicated by the switching of the latch in Figs. 15(b) and 16(b).

[4]The y axis for static noise analysis and SPICE plots of outd are on different scales because we want to show the latch switching in SPICE and hence need to include the full swing.

[5]For SPICE simulations where the latch switches (Cases 1, 4, and 5) we consider the peak noise to be the value of the noise waveform at time $t_{\max}$, where $t_{\max}$ is the peak time for the cases where the latch does not switch (i.e., nonswitching Case 2/3 for switching Case 1, and nonswitching Case 6 for switching Case 4/5).

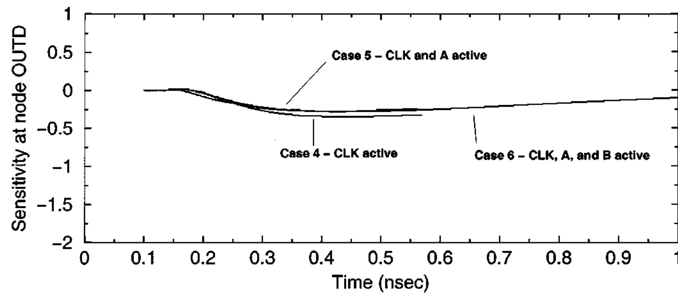

Fig. 20. The sensitivity, as determined by static noise analysis, of node outd with respect to the noise appearing on node dynd for Cases 4–6, when the coupling capacitance on net A has been reduced.

TABLE V
BODY VOLTAGES USED BY STATIC NOISE ANALYSIS AND SPICE FOR INITIALIZATION OF THE PROPAGATED NOISE SIMULATION

Transistor (→ target state)	Case	PacifIC target state voltage	SPICE target state voltage	PacifIC reference state voltage
M1 (→ state 5)	1	0.97 V	0.90 V	3.43 V
	2	0.66 V	0.70 V	2.80 V
	3	0.26 V	0.10 V	2.37 V
	4	0.97 V	0.90 V	3.43 V
	5	0.80 V	0.75 V	3.10 V
	6	0.26 V	0.11 V	2.37 V
M2 (→ state 1)	1	0.94 V	0.90 V	3.43 V
	2-5	0.77 V	0.60 V	2.80 V
	6	0.60 V	0.60 V	2.37 V
M7 (→ state 1)	1	0.70 V	0.65 V	2.55 V
	2-6	0.60 V	0.60 V	2.37 V
M9 (→ state 2)	1-5	3.01 V	3.00 V	1.45 V

C. Elimination of Failures

In order to eliminate the functional failures observed, one might consider reducing the coupling noise on A by more careful routing of this signal line or by placing the domino gate closer to the $A - \bar{A}$ driver. In Figs. 19 and 20, we show what happens for Cases 4–6 if we reduce the coupling noise on A by reducing C_c to 33 fF. As Fig. 19 shows, the propagated noise on dynd and outd is significantly reduced when compared to Fig. 14. The worst noise remains the same for Case 6, however, because charge-sharing noise is not affected by a reduced C_c. Fig. 20 shows that there is no instability at outd, with SPICE simulations (not shown) confirming no functional failures.

D. Effect of Body Voltage Variation

The small differences between PacifIC and SPICE (see Table IV) in the amount of propagated noise to node dynd are primarily influenced by slight differences in the initial condition body voltages (most significantly on transistor $M1$). Table V shows the initial condition body voltage values used by static-noise analysis and SPICE for transistors $M1$, $M2$, $M7$, and $M9$ when calculating the amount of propagated noise on net dynd.

PacifIC uses modified accessibility analysis, as described in Section II, to accurately estimate the initial condition body voltages. Table V lists both the target state body voltages and reference state body voltages that result from the analysis. In Case 1, there are no active net tags and the reference state value is initialized to V_4^{zero} (see Table I). Even though the circuit design explicitly includes transistor $M13$ to predischarge the internal node I [see Fig. 9(a)], this is not known until the clock is marked active in Cases 2 and 3. In these cases, transistor $M13$ discharges the internal node between transistors $M1$ and $M2$ every cycle. For Case 2, the reference state body voltage is discharged down to V_3^{forward} to satisfy the active-net constraints as described in Section II. The state-5 body voltage of Case 3 is lower than that of Case 2 because the active net tagging of A forces accessibility of state 1.

For Case 4, there is no predischarge device for node I; therefore, even with the clock active, the reference state voltage used remains V_4^{zero}, as in Case 1. Case 5 is similar to Case 4, but the fact that net A is under steady switching means that both states 2 and 4 are accessible for FET $M1$. State 2 accessibility limits the maximum body voltage possible to only about 0.80 V. This body voltage is not high enough to result in significant parasitic bipolar leakage, but the threshold voltage is still reduced enough to result in functional failure. Only when A, B, and CLK are marked active in Case 6 can the reference state voltage be brought down substantially to V_3^{forward}.

For SPICE, Table V shows the body voltages immediately after the $A = 0$, $B = 1$, $clk = 1$ condition is established at $t = 100\ \mu$s (allowing comparison with the initial condition target state body voltages used by static noise analysis). For example, in Cases 1 and 4, the body of transistor $M1$ charges easily to a very high bias, and at $t = 100\ \mu$s, $M1$ begins to draw bipolar leakage current. Our conservative upper bound in static noise analysis generally overestimates the target state body voltages in comparison with SPICE. The main reason for this discrepancy is the neglect of state 6 which is exerting a downward pressure on the body voltage which is not (in the interests of conservatism) considered in the modified accessibility analysis.

V. CONCLUSION

We have described extensions to transistor-level static noise analysis to handle the unique issues of PD-SOI technology: floating-body-induced threshold voltage variations and parasitic bipolar leakage currents. In particular, we have developed a model for estimating the allowable body voltage variation which takes into account modest knowledge of which nets have dependable regular-switching activity.

More work is required to include the effects of the dynamic state 6 in modified accessibility analysis. Future work could also include developing techniques by which nets would be explicitly forced active to control body voltage variation. This could be viewed as analogous to DRAM refresh. More work would be required to determine the necessary frequency and nature of this pattern.

REFERENCES

[1] C. T. Chuang, P.-F. Lu, and C. J. Anderson, "SOI for digital CMOS VLSI: Design considerations and advances," *Proc. IEEE*, vol. 86, pp. 689–720, 1998.

[2] M. Canada *et al.*, "A 580 MHz RISC microprocessor in SOI," in *Dig. Tech. Papers, Int. Solid-State Circuits Conf.*, 1999, pp. 430–431.

[3] D. H. Allen *et al.*, "A 0.20 μm 1.8 V SOI 550 MHz 64b PowerPC microprocessor with Cu interconnects," in *Dig. Tech. Papers, Int. Solid-State Circuits Conf.*, 1999, pp. 438–439.

[4] C. T. Chuang and R. Puri, "SOI digital CMOS VLSI—A design perspective," in *36th ACM/IEEE Design Automation Conf.*, 1999, pp. 709–714.

[5] P.-F. Lu *et al.*, "Floating-body effects in partially depleted SOI CMOS cicuits," *IEEE J. Solid-State Circuits*, vol. 32, pp. 1241–1253, Aug. 1997.
[6] C. T. Chuang, P. F. Lu, J. Ji, L. F. Wagner, S. Chu, and C. J. Anderson, "Dual-mode parasitic bipolar effect in dynamic CVSL XOR circuit with floating-body partially-depleted SOI devices," in *Int. Symp. VLSI Technol., Systems, and Applications*, 1997, pp. 288–292.
[7] K. L. Shepard, V. Narayanan, and R. Rose, "Harmony: Static noise analysis for deep-submicron digital integrated circuits," *IEEE Trans. Computer-Aided Design*, pp. 1132–1150, Aug. 1999.
[8] *BSIMPD Manual Version 2.2*, Univ. California, Berkeley, 2001.
[9] G. G. Shahidi *et al.*, "SOI for 1-volt CMOS technology and applictaion to a 512 kb SRAM with 3.5 ns access time," in *Proc. IEDM*, 1993, pp. 813–816.
[10] K. L. Shepard and D. Kim, "Body-voltage estimation in digital PD-SOI circuits and its application to static timing analysis," in *Proc. IEEE/ACM Int. Conf. Computer Aided-Design*, 1999, pp. 531–538.
[11] K. L. Shepard and D.-J. Kim, "Static noise analysis for digital integrated circuits in partially-depleted silicon-on-insulator technology," in *ACM/IEEE Design Automation Conf.*, 2000, pp. 239–242.
[12] Pacific data sheet, Cadence Design SystemsD.-J. Kim.. [Online]. Available: http://www.cadence.com/datasheets/cadmospacif.html.
[13] S. A. Parke, J. E. Moon, H. C. Wann, P. K. Ko, and C. Hu, "Design for suppression of gate-induced drain leakage in LDD MOSFET's using a quasitwo-dimensional analytical model," *IEEE Trans. Electron. Devices*, vol. 39, pp. 1697–1703, July 1992.
[14] K. L. Shepard and V. Narayanan, "Noise in deep submicron digital design," in *Proc. IEEE/ACM Int. Conf. Computer-Aided Design*, San Jose, CA, Nov. 1996, pp. 524–531.

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