A 100-fps Fluorescence Lifetime Imager in Standard 0.13-µm CMOS

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Abstract

A wide-field fluorescence lifetime imager capable of up to 100 frames per second (fps) is presented. The imager consists of a 64-by-64 array of low-noise single photon avalanche diodes (SPADs) in a standard 0.13-µm CMOS process, 4096 time-to-digital converters, and an application specific data path to enable continuous image acquisition at a total output data rate of 42 Gbps. These features combine to enable new lifetime-based diagnostic imaging.

Introduction

Fluorescence is used for a wide range of established and emerging biological and diagnostic imaging techniques. These techniques have traditionally relied on spectrally resolved intensity-based measurements. Recently, fluorescence lifetime imaging microscopy (FLIM) has emerged as a method for collecting additional information from fluorescent signals. In this modality, image contrast is based on the decay rate of a fluorophore's emission intensity following a pulsed excitation. This decay rate is closely linked to a fluorophore's chemical and physical microenvironment and can be used diagnostically[1,2]. The most accurate and wide-spread technique for acquiring FLIM images is time-correlated single-photon counting (TCSPC). Typical TCSPC systems consist of one measurement channel (single-photon detector and time-to-digital converter) and require pixel-by-pixel scanning with a laser to form an image, resulting in image acquisition times of tens of seconds and limiting the applications of FLIM to stationary samples.

This work builds on significant prior work in the development of CMOS-based SPADs as sensors[3–6]. Previous CMOS imagers based on SPADs have been unable to provide sustained high-speed TCSPC FLIM imaging due to the high data rates required[4,5]. Other approaches that allow approximate lifetimes to be extracted have been employed to reduce data rates and achieve demonstrated frame rates up to 50 fps for bursts of only 240 frames[6]. In this work, we present the first 64-by-64 array-based FLIM imager capable of supporting a data rate of 42 Gbps, allowing full lifetime waveform acquisition with an associated maximum frame rate of 100 fps. This is accomplished with the integration of low-noise SPADs[3], independent time-to-digital converters (TDCs), and a datapath that is optimized for TCSPC FLIM data compression. Such continuous high-frame-rate wide-field imaging enables many scientific applications in microscopy and clinical applications in endoscopy (where fast image acquisition is essential to prevent motion artifacts).

Fluorescence Lifetime Imager Design

Fig 1 shows a die photograph of the FLIM chip, a 9-mm-by-4-mm chip, fabricated in a standard IBM 0.13 µm process, with major functional blocks highlighted. A phase-locked loop (PLL) is used to generate a 1-GHz on-chip clock that is synchronized with a 20-MHz reference from a laser. The 64-by-64 imaging array is divided into four quadrants with a pixel pitch of 48 µm. Each pixel consists of a SPAD[3]; active reset, quench, and control circuits; and a peripheral time-to-digital converter (TDC). Fig 2 shows the SPAD control circuitry which generates the "stop" input to the TDC, shown in Fig 3. The TDCs of 128 pixels share a single delay-locked loop (DLL), resulting in 32 DLLs on the chip. Each DLL is accompanied by a 6-bit binary counter that is used for coarse-time measurements. The 16-phases of the DLL are encoded into 4 bits, resulting in 10-bit timing resolution (62.5 ps LSB with a 64 ns range) from the TDC.

In addition to the 10-bit timing information, each pixel generates a valid bit and requires 10-bit position information, which results in a generated data rate of over 1.5Tbps for continuous full-speed operation at a 20-MHz laser repetition rate. In order to prevent pile-up nonlinearities, however, TCSPC generally requires that the average hit rate for each pixel be around 1%[7]. Consequently, many laser repetitions result in no hits at a given pixel, allowing for significant data compression. A custom datapath eliminates these zeros as the data are moved from the TDC flip-flops to off-chip drivers as shown in Fig 4. This reduces the average data rate to approximately 16 Gbps. Each quadrant of the array has a dedicated bank of 21 low-voltage differential-signaling (LVDS) output buffers that can operate at up to 500 Mbps per channel. This provides up to 42 Gbps of bandwidth to accommodate data bursts. To form an image generally requires 2000 photon "hits" per pixel, which at 1% hit rate corresponds to 200,000 laser repetitions. At a 20-MHz laser repetition rate, 100 frames per second can be supported by the imager.

Measurement Results

The test board (Fig 5) is configured with one Xilinx XC6V130LXT FPGA per quadrant. The board is designed with a cabled PCIe interface for continuous high-speed data transfer to a PC. This interface is still under development, and current PC communication is performed over a 1 MHz serial interface using an Opal Kelly XEM6010-LX45, currently limiting imaging to a single quadrant at a time and restricting image acquisition speed.

We first characterized the transfer functions of the TDCs for recording the photon arrival times using the electrical calibration path in the pixel circuit and a SRS DG535 delay/pulse generator. Maximum DNL/INL are better than 3 LSB, limited by on-board jitter in the characterized delay path (which will not be present on-chip). Fig 6 shows the dark count rate (DCR) for each pixel in the bottom left quadrant of the array, averaging only 302 Hz at 1.25 V overvoltage. Fig 7 shows an image of a spot of 0.5 mM fluorescein dye in pH 7.4 PBS. Fig 7a shows an intensity image acquired by photon counting at each pixel. Fig 7b shows the corresponding lifetime image with lifetime values of 4-5ns[8]. These imagers are acquired with a 1-MHz repetition rate using a pulse-picked Fianium SC-450, allowing over 30,000 counts to be collected per pixel. A representative monoexponential decay curve from one of the pixels in Fig. 7b is shown inset. Table 1 summarizes the measured performance of the chip. Additional work continues to enable the PCIe interface and characterize the full 100-fps capabilities of the imager.

Acknowledgments

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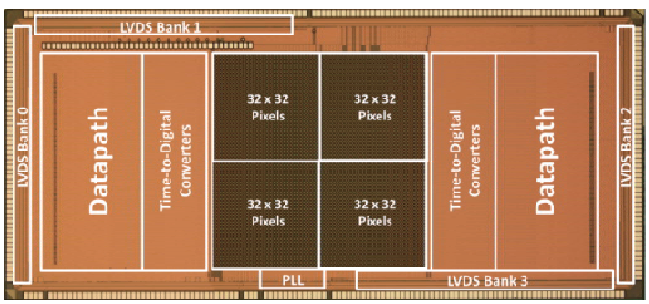

Fig 1: Die photograph and functional blocks of FLIM imaging IC.

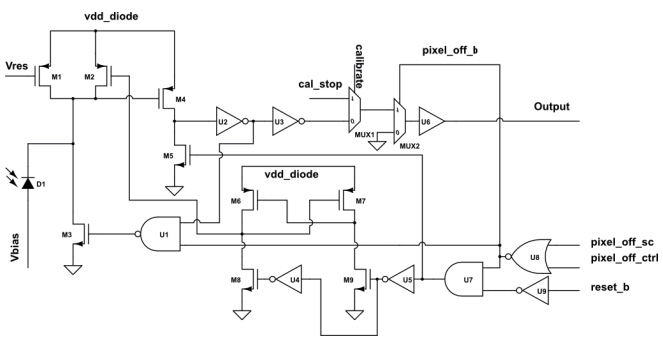

Fig 2: Pixel control, quench, and reset circuitry. Each pixel has an active quench (M1) and reset (M2) circuit accompanied by an output buffer that can select between the SPAD output and an electrical calibration signal. Each pixel can be disabled through the scan chain (pixel_off_sc) or through a global controller (pixel_off_ctrl). This controller can disable the pixel to limit the measurement window and reduce the likelihood of recording dark counts once the fluorescent signal has decayed. Transistors M1-M4 are thick oxide devices to allow for SPAD over voltages up to 3.3V.

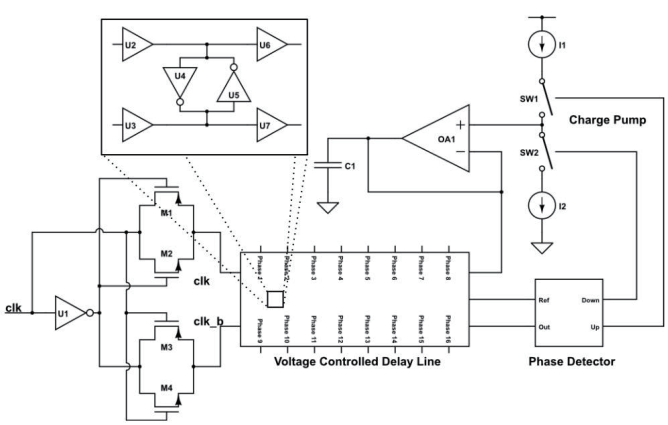

Fig 3: A differential voltage controlled delay line generates 16 phases from a globally distributed single-ended 1-GHz clock. These 16 phases along with a 6-bit coarse counter (not shown) are recorded into flip-flops that are asynchronously clocked by the pixel output signal.

Table 1: Performance characteristics of FLIM imager.

Pitch	48 µm
TDC Resolution/Range	62.5 ps / 64 ns
TDC DNL/INL Max.	< 3 LSB
Avg. DCR (V_{ov} = 1.25V)	302 Hz
PDP (V_{ov} = 1.25V) @ 425nm [3]	25.3%
System Power	14.5 mW/pixel

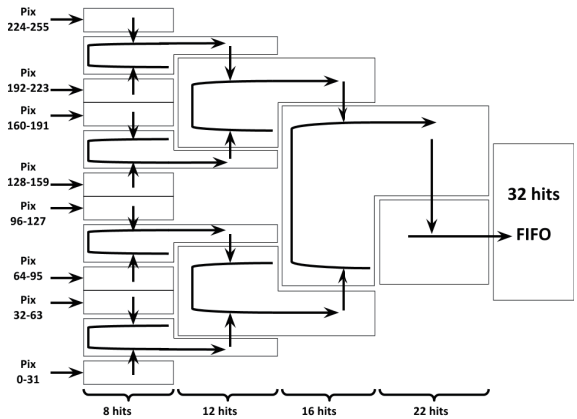

Fig 4: TDC data moves from left to right through a series of controlled shift registers. Each left-to-right shift stacks all non-zero data sequentially in the register. Registers are sized based on statistics of the photon arrival times such that an overflow event will occur in less than 1/1e9 measurements, on average.

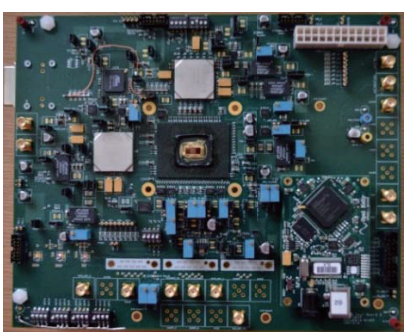

Fig 5: Photograph of test and characterization printed circuit board.

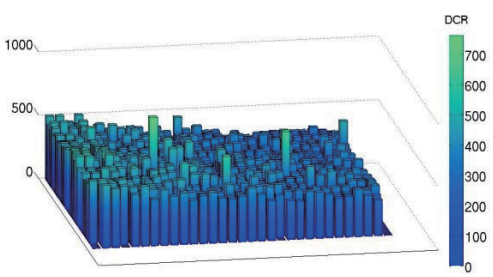

Fig 6: Dark count rate of bottom left quadrant of imager with V_{ov} = 1.25V.

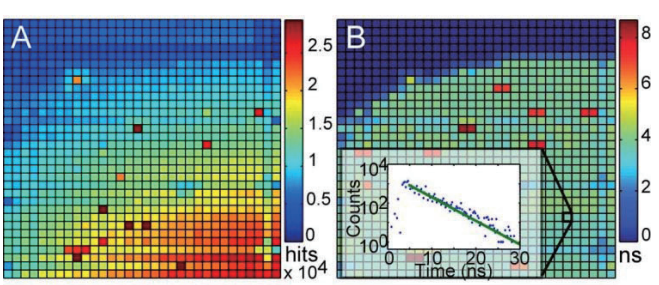

Fig 7: Images of a spot of fluorescein dye. (a) Intensity as measured by the total number of photon hits per pixel. (b) Lifetime of the fluorescence. (inset) representative decay curve.