23.1 A 2.5D Integrated Voltage Regulator Using Coupled-Magnetic-Core Inductors on Silicon Interposer Delivering 10.8A/mm²

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Energy consumption is a dominant constraint on the performance of modern microprocessors and systems-on-chip. Dynamic voltage and frequency scaling (DVFS) is a promising technique for performing “on-the-fly” energy-performance optimization in the presence of workload variability. Effective implementation of DVFS requires voltage regulators that can provide many independent power supplies and can transition power supply levels on nanosecond timescales, which is not possible with modern board-level voltage regulator modules (VRMs) [1]. Switched-inductor integrated voltage regulators (IVRs) can enable effective implementation of DVFS, eliminating the need for separate VRMs and reducing power distribution network (PDN) impedance requirements by performing dc-dc conversion close to the load while supporting high peak current densities [2-3]. The primary obstacle facing development of IVRs is integration of suitable power inductors. This work presents an early prototype switched-inductor IVR using 2.5D chip stacking for inductor integration.

The IVR employs 2.5D silicon interposer technology, thereby providing high thermal conductivity and minimizing losses from eddy currents, skin effect and domain wall motion as shown in Fig. 23.1.4. Efficiency versus switching frequency and load current for the IVR chip stack are shown in Figs. 23.1.5 and 23.1.6, respectively. Efficiency peaks at 74% with input voltage of 1.8V, conversion ratio of 0.61, switching frequency of 75MHz and load current of 3A. The FEOL current density is 10.8A/mm², which we define as load current divided by the FEOL area of the switches and the controller, likewise the silicon interposer current density is 0.94A/mm², which we define as load current divided by the total interposer area, 3.2mm². At peak efficiency, inductor DC and AC losses contribute approximately 26% and 48% of the total power loss, respectively, while switching and conduction of the bridge FETs contribute 25%. The peak current density occurs at the thermal limit of the IC with a load current of 5.4A and efficiency of 64%. Further improvement of the inductor structures, in particular lamination of the magnetic material to reduce eddy-current losses, will significantly improve the efficiency.

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References:
Figure 23.1.1: Diagram of 2.5D integrated voltage regulator (IVR) chip stack. IC with buck converter and load circuitry flips onto interposer with power inductors, which wirebonds to a ball grid array substrate.

Figure 23.1.2: Complete IVR system overview (top) and fast non-linear control loop (bottom).

Figure 23.1.3: Top view of four single-turn, coupled power inductors (left), cross-section of magnetic cores and windings (top right) and magnetization curves for the Ni-Fe core material (bottom right).

Figure 23.1.4: Inductance (L), coupling coefficient (K) and resistance (R) of coupled single-turn inductors.

Figure 23.1.5: IVR efficiency as a function of switching frequency.

Figure 23.1.6: IVR efficiency as a function of load current at 75MHz switching frequency.
Figure 23.1.7: Photo of IC (top left), silicon interposer (bottom left) and assembled chip stack (right).