All-around contact for carbon nanotube field-effect transistors made by ac dielectrophoresis

Zhi-Bin Zhang\textsuperscript{a}) and Shi-Li Zhang\textsuperscript{b})

\textit{Department of Microelectronics and Information Technology, Royal Institute of Technology, Electrum 229, SE-164 40 Kista, Sweden}

Eleanor E. B. Campbell

\textit{Department of Physics, Gothenburg University, SE-412 96 Göteborg, Sweden}

(Received 10 June 2005; accepted 7 November 2005; published 12 January 2006)

Carbon nanotube field-effect transistors (CNFETs) are fabricated by depositing one bundle of single-walled carbon nanotubes (SWNTs) per device between a pair of predefined Pd electrodes using ac dielectrophoresis. By repeating the process for the formation of the Pd electrodes after the bundle deposition, all-around Pd contacts are made to the SWNT bundles. After the formation of all-around contact, the CNFETs with only semiconducting SWNTs in the bundles retain a strong gate modulation with a high ratio of on to off current $I_{\text{on}}/I_{\text{off}} \geq 10^6$. For the CNFETs with at least one metallic SWNT in the bundles, their gate modulation disappears and carbon nanotube resistors (CNRs) are obtained. The on current $I_{\text{on}}$ of CNFETs is found to be sensitive to the process for the formation of all-around contact. In contrast, the two-probe resistance of CNRs is consistently reduced after the all-around contacts. The electrical measurements also indicate the presence of an interlayer residing at the SWNT/Pd contacts. © 2006 American Vacuum Society.

[DOI: 10.1116/1.2150226]

I. INTRODUCTION

The remarkable electrical properties of carbon nanotubes (CNTs) make them a promising building block in future nanoelectronics.\textsuperscript{1–4} One major challenge for the implementation of CNT-based electronic circuits is a controllable assembly of CNTs onto electrodes.\textsuperscript{5} Random deposition of CNTs on a substrate is impracticable for large-scale device fabrication. Growth of CNTs on patterned catalyst islands\textsuperscript{6} suffers from the high temperature (900 °C) during chemical-vapor deposition processing. This latter method is currently also challenged by its inability to only grow semiconducting CNTs through suppressing the growth of metallic tubes. Recently, ac dielectrophoresis has been developed to site selectively position individual metallic single-walled carbon nanotubes (m-SWNTs) or bundles between predefined electrode pairs.\textsuperscript{7–9} Through surface functionalization using sodium dodecyl sulfate (SDS), we have succeeded in depositing individual semiconducting SWNTs (s-SWNTs) onto electrode pairs by means of ac dielectrophoresis.\textsuperscript{10} We have attributed the successful fabrication of carbon nanotube field-effect transistors (CNFETs) to the formation of an electrical double layer around the s-SWNTs. The uniqueness of our method lies precisely in its good site selectivity and room-temperature processing.

Since the SWNTs deposited this way are contacted from the bottom by the electrodes, most likely bonded through a van der Waals force, a poor electrical contact may form. In the present work, we focus on the electrical contact between SWNTs and electrodes. Each of the devices studied consists of a bundle of SWNTs between an electrode pair. We have employed a method where the two ends of a bundle are subsequently coated with a second, top contact formed by repeating the process used for the base electrode pairs, i.e., standard photolithography and the lift-off technique. This process leads to the formation of an all-around contact geometry for the SWNT bundle. After the formation of all-around contact, the CNFETs with a bundle composed of pure s-SWNTs retain a strong gate modulation.

II. EXPERIMENT

Raw SWNT soot prepared by high-pressure conversion of CO(HiPCO) was ultrasonically suspended in a 1 wt % aqueous SDS solution. The suspension was then centrifuged twice at 16 000 g for 12 h. The upper supernatant was decanted for nanotube deposition. The devices were fabricated on heavily Sb-doped Si(100) wafers after a 150-nm-thick SiO\textsubscript{2} was thermally grown. Base electrode pairs were made of a 20-nm-thick Pd layer, using standard photolithography and the lift-off technique. The electrode pairs were 1 or 2 μm wide and separated by 1–3 μm.

During the nanotube deposition using ac dielectrophoresis, a drop of the SWNT-containing suspension, in 2 μl, was placed on the device area where an ac bias was applied to one electrode with the other electrode grounded and the substrate floating. The frequency was 10 MHz and the peak-to-peak voltage ($V_{\text{p-p}}$) was 5 V. After 1 min, the ac bias was turned off. The device was then briefly rinsed by deionized (DI) water (<5 s) and blown dried with N\textsubscript{2}. The devices were characterized by means of atomic force microscopy (AFM) in tapping mode and transport measurements on a HP 4156A precision semiconductor parameters analyzer. Most

\textsuperscript{a)Electronic mail: zhibin@imit.kth.se}

\textsuperscript{b)Electronic mail: shili@imit.kth.se}
frequently, several SWNT bundles 1–6 nm in diameter, according to AFM height profiling, were simultaneously aligned between an electrode pair using this technique. In this work, we only focus on devices with one bundle per device as shown schematically in Fig. 1. Altogether, we fabricated over 100 such devices among which about 15% behaved as $p$-type field-effect transistor with a high $I_{\text{on}}/I_{\text{off}}$ ratio $>10^6$. This low rate of success in producing transistors is a consequence of the use of mixed tubes: metallic and semiconducting.

Immediately after AFM and transport studies, the devices underwent a top contact fabrication step where the process for the base electrodes was repeated but with a fresh 30-nm-thick Pd layer. With this process step, the two ends of the SWNT bundle were covered by Pd forming an all-around contact geometry at the wafer level, [cf. Fig. 1(b)]. By properly adjusting the process parameters for photolithography, the distance between the top contacts could be varied with respect to the base electrodes. Shown in Fig. 2 is an AFM image of a typical device with the all-around contacts where the front edge of both top contacts extends inwards by about 0.1–0.3 µm from the base electrodes, thus narrowing down the distance between the electrodes. This configuration is referred to “symmetric contacts.” With this configuration, probable effects of the mechanical deformation of CNTs on electronic transport properties could be eliminated with the top contacts. Finally, the devices were annealed using rapid thermal processing (RTP) at 500 °C in Ar for 30 s. The whole process for the formation of all-around contact is not only compatible with standard Si technology but also of low thermal budget.

III. RESULTS AND DISCUSSION

A. Resistors with bundles having at least one $m$-SWNT

The majority (85%) of the devices showed no transistor action already after the fabrication because of the presence of metallic tubes in the starting material, and carbon nanotube resistors (CNRs) showing a good Ohmic behavior were obtained instead. Apparently, there was at least one $m$-SWNT present in each of the bundles and the $m$-SWNT was in direct contact with the base electrodes. After the formation of all-around contact, the two-probe resistance $R_{2t}$ was found to decrease by 10–100 times from 20 kΩ to 1 MΩ for all devices without exception. Smaller $R_{2t}$ were found for resistors with larger diameter bundles, as expected. In fact, the reduction of $R_{2t}$ already occurred when the top Pd electrodes were deposited and the RTP step induced a further reduction. The drastic reduction of $R_{2t}$ is ascribed to an increased contact area between the bundle and the Pd (Ref. 12) as well as an improved Pd-tube contact by the anneal. Several CNRs were comprised of one $m$-SWNT instead of a bundle, since the SWNT had a diameter around 1 nm according to AFM analysis. For these resistors, the $R_{2t}$ was above 1 MΩ even with the all-around contact. Pd has been reported to yield Ohmic contacts to $m$-SWNTs with a contact resistance ($R_c$) at 10–20 kΩ. Since transport in $m$-SWNTs is ballistic on a length scale of micrometer at low voltages, $R_{2t}$ should be mainly determined by $R_c$. Therefore, the high $R_{2t}$ in our devices indicates that the contacts are not intimate between the Pd and the SWNTs even after the all-around process. It is likely that an interlayer, possibly composed of residual SDS molecules, was present between the Pd and the SWNTs leading to a high $R_c$. Indeed, we have found that residual SDS molecules were still adsorbed on SWNTs after a brief DI water rinsing for about 5 s.
B. Conversion of CNFETs to CNRs with bundles having at least one \( m \)-SWNT

The \( I_{\text{on}}/I_{\text{off}} \) ratio for most CNFETs after the fabrication was greater than \( 10^6 \). After the formation of all-around contact, the capability of gate modulation for around 25% of the CNFETs was greatly reduced. Shown in Fig. 3 is an example where the \( I_{\text{on}}/I_{\text{off}} \) ratio has been reduced by five orders of magnitude. The device behaves almost like a resistor. In these degraded CNFETs, it is believed that there is at least one \( m \)-SWNT in the bundle. The \( m \)-SWNT is not in contact with the base electrodes, but becomes accessible by the top contacts. Once the \( m \)-SWNT is contacted, it predominates the transport through the bundle and greatly reduces the gate effect. Furthermore, the large \( I_{\text{on}}/I_{\text{off}} \) ratio as well as the low \( I_{\text{off}} \) at \( 10^{-13} \) A after the fabrication indicates that the \( m \)-SWNT was completely insulated from the base electrodes by the underlying \( s \)-SWNTs in the same bundle. This observation is in agreement with the large coupling resistance between SWNTs in a bundle.\(^{15} \)

C. CNFETs with bundles of only \( s \)-SWNTs

About 75% of the CNFETs retained their large \( I_{\text{on}}/I_{\text{off}} \) ratio (\( \geq 10^6 \)) after the formation of all-around contact. This indicates that the bundles are only composed of \( s \)-SWNTs. Figure 4 shows the \( I_{D}-V_{G} \) characteristics of such a CNFET with a \( \sim 3.5 \) nm diameter bundle. The contacts are symmetric as shown in Fig. 2. The \( I_{\text{on}} \) of this device has increased from 0.6 to 2.0 \( \mu \)A with an on-state resistance around 600 k\( \Omega \) after the formation of all-around contact. However, an increase in \( I_{\text{on}} \) after the formation of all-around contact was not always observed despite of the use of identical contact fabrication process. Unlike the resistors discussed above, the performance of CNFETs was apparently extremely sensitive to subtle variations whose nature and behavior are currently unknown. It should be noted that the CNRs and CNFETs appear in the same wafers, i.e., identical processes applied to both kinds of devices.

D. Symmetric versus asymmetric contacts

In Fig. 5(a) where the \( I_{D}-V_{D} \) characteristics for the same CNFET as in Fig. 4 are shown, \( I_{D} \) has not reached the saturation even at \( V_{D}=-2 \) V, which can be compared to a similar device with an intimate Pd-SWNT contact\(^{16} \) whose \( I_{D} \) started to saturate already at \(-1 \) V. This difference also suggests the existence of an interlayer at the contacts of our CNFET, in

![Fig. 3. Change of \( I_{D}-V_{G} \) characteristics for a CNFET with a bundle containing at least one \( m \)-SWNT before and after the formation of all-around contact.](image1)

![Fig. 4. Change of \( I_{D}-V_{G} \) characteristic for a CNFET with a bundle of pure \( s \)-SWNTs before and after the formation of all-around contact.](image2)

![Fig. 5. (a) Two sets of \( I_{D}-V_{D} \) characteristics for the CNFET with symmetric contacts obtained by exchanging the source and drain terminals. (b) \( I_{D}-V_{G} \) characteristics for the same device at different \( V_{D} \).](image3)

\(^{13} \) Zhang, Zhang, and Campbell: All-around contact for carbon nanotube field-effect transistors

\(^{15} \) J V S TB-M i c r o e l e c t r o n i c s a n d N a m o t e r Structures
agreement with the observation with the CNRs above. The interlayer inevitably imposes an energy barrier to the tunneling of carriers at both source and drain contacts.

Exchanging the source and drain terminals does not cause significant differences in the $I_D-V_D$ characteristics as seen in Fig. 5(a). This behavior is consistently found for a number of CNFETs. As the performance of our CNFETs has been found to be extremely sensitive to subtle variations at the contacts, it is difficult to conclude that the two contacts at the source and drain are identical. In light of the Schottky barrier model for the gate modulation of a CNFET, a slight difference in the two contacts can result in a substantially different current response when the source and drain terminals are exchanged, because of an exponential dependence of the tunneling current on the Schottky barrier height. A large difference in $I_D$ when exchanging the source and drain terminals has indeed been reported for Ti-contacted CNFETs. If the Schottky barrier for the Pd-tube contact is lower than the Ti-tube contact, the anticipated difference in $I_D$ upon exchanging the source and drain terminals would be much less pronounced for our devices with Pd contacts as compared to the CNFETs with Ti contacts. The absence of substantial increases of $I_{off}$ when decreasing $V_D$ (more negative) in the $I_D-V_G$ characteristics in Fig. 5(b) could also be accounted for by invoking a low Schottky barrier for the Pd-tube contact. Decreasing $V_D$ would reduce the Schottky barrier height and thus increase $I_{off}$ as has been observed in CNFETs with Ti contacts.

Whether the Schottky barrier model applies to our devices or not needs to be confirmed with further examples. We have therefore also intentionally made the contacts asymmetric as shown in the inset in Fig. 6(a), with one top contact shorter than its underlying base contact at one end while having the other end similar to that in Fig. 2. The $I_D-V_D$ characteristics in Fig. 6(a) resemble those in Fig. 5(a), in the sense that only a small difference in $I_D$ is found after exchanging the source and drain terminals. However, a much more pronounced influence of $V_D$ on $I_{off}$ is seen in Fig. 6(b), as compared to that in Fig. 5(b). This strong influence remained even when the source and drain terminals were exchanged. Whereas the behavior in Fig. 6(a) could still be interpreted as for Fig. 5 by assuming a low barrier height for the Pd-tube contact, it is a major effort to understand the observation in Fig. 6(b). The kink at the end where the top contact is shorter than its underlying base contact could modify the local band structure of the SWNT thereby introduce an additional energy barrier that would be modulated by the gate potential. The large influence of $V_D$ on $I_{off}$ in Fig. 6(b) could be accounted for if this kink-induced barrier would become a predominant factor for the carrier transport. But this assumption would also suggest a large difference in $I_D$ when exchanging the source and drain terminals, disagreeing with the observation in Fig. 6(a). It is unlikely that the kink-induced barrier would behave differently during the $I_D-V_D$ and $I_D-V_G$ measurements. Apparently, a consistent picture to explain the observations in Figs. 5 and 6, with symmetric and asymmetric contacts, respectively, is currently lacking and much desired. Whether or not tunneling through the interlayer at the SWNT/Pd interfaces could be dominating remains to be confirmed.

A valid comparison, in terms of contact integrity, between the contact schemes studied here, i.e., bottom and all-around, and the prevailing top contact geometry in the literature is at present very difficult. Our understanding of the metal-CNT contacts is premature and even a subtle difference in the materials involved and processes employed for the fabrication of test devices may lead to undesired effects that overshadow the sought physical picture(s).

**IV. CONCLUSIONS**

We have successfully fabricated CNFETs with single SWNT bundles using ac dielectrophoresis. Of the 100 plus devices fabricated in this work, about 15% are CNFETs showing a strong gate modulation with a high $I_{on}/I_{off}$ ratio $\geq 10^6$. The rest behave more like a resistor because of the $m$-SWNTs present in bundles being contacted by the base electrodes. The rate of success in fabricating CNFETs using the novel method presented here is expected to reach 100% if a CNT source containing only $s$-SWNTs is available. By repeating the process for the fabrication of the base electrodes using standard photolithography and the lift-off technique, all-around contacts are formed at the wafer scale.
About 3/4 of the CNFETs retain their large \( I_{on}/I_{off} \) ratio after the formation of all-around contact, while the remaining 1/4 have been converted to resistors as a result of the presence of at least one m-SWNT that is now being reached by the top contacts. Whereas the formation of all-around contact has significantly reduced the two-probe resistance of the resistors, the \( I_{on} \) of CNFETs is extremely sensitive to subtle variations at the contacts. The measured \( I-V \) characteristics also indicate the presence of an interlayer at the SWNT/Pd contacts.

**ACKNOWLEDGMENTS**

One of the authors (Z.-B. Z.) is grateful to Dr. X.-J. Liu for fruitful discussions. This work was partly financed by the Swedish Research Council (VR) (No. 621-2002-4099).

---