Statistical Timing in a Practical 65 nm Robust Design Flow

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The power of statistical formulas
Acknowledgements

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Caveat

- This presentation is mostly ASIC-focused, although microprocessor design issues will be mentioned (time permitting)
Outline

- Yield loss mechanisms and the tradeoffs involved
- **What is robust design?**
- **A timing closure methodology based on statistical timing**
- **Myths about statistical timing**
- **Interesting challenges**
  - early/late splits and CPPR
  - at-speed test
  - metrics for optimization
  - delay modeling for 45 nm
  - hierarchical statistical timing
Catastrophic vs. parametric yield loss

Diagram showing yield loss over time with different yield types: Defect Based, Lithography Based, and Parametric (design-based).

Source: NEC
Increasing and inevitable parametric variability

Litho-induced variability

Random dopant effects*

Oxide thickness

Interconnect CMP and RIE effects

*D. J. Frank et al, Symp. VLSI Tech., 1999
Normalized metal resistance data over 3 months

- **Wafer means change over time**
- **Values are “out-of-spec,” need to yield within WAC limit**

We would like to retain these wafers
Manufacturing for predictable performance

- Cp and Cpk (Process Capability Indices) measure manufacturing predictability
- Manufacturing typically (but not always) outperforms spec. limits
Normalized cumulative statistics

- Distributions are not Gaussian (but usually close)
Ring oscillator performance distribution

- Color coding is by wafer
- Hardware is faster/tighter than predictions
Normalized metal resistance across manufacturing lines

- Designs must yield at multiple fabs.
Normalized single-level capacitance distribution

- Variability is enormous!
Any performance left in worst-case design?
What do we do with all this variability?

As we know,
There are known knowns.
There are things we know we know.

We also know
There are known unknowns.
That is to say
We know there are some things
We do not know.

But there are also unknown unknowns,
The ones we don't know
We don't know.

Donald H. Rumsfeld

1Dept. of Defense news briefing, 2/12/02, linebreaks mine
Robust circuit design

\[ P(x, y) = \text{mean} \]

\[ + \frac{\partial p}{\partial x} \Delta x + \frac{\partial^2 p}{\partial x^2} \Delta x^2 + \cdots \]

\[ + \frac{\partial p}{\partial y} \Delta y + \frac{\partial^2 p}{\partial y^2} \Delta y^2 + \cdots \]

- Its the sensitivities, stupid!
Delay modeling

Can get across-parameter RSS relief

Can get space-dependent relief

Can get down-a-path RSS relief

Fast chip vs. slow chip

Chip means

Systematic ACV

Random ACV
Model-to-hardware correlation

- Early
- Late
- Fast chip
- Slow chip
- Mean RO delay

- RO delay
- Mean RO delay
Bounding distributions provide protection from various sins!
Statistical-timing-based flow

- Conduct statistical timing with correlations
  - predict timing slacks in “canonical” form parameterized by the sources of variation
- “Project” flop slacks to worst corner; if positive, we are safe
- Get “debits” and “credits”
  - mixed-mode projection
  - spatial
  - coupling noise
  - independently random
- Check sensitivities
  - alternative statement of Murphy’s law: “Variability exacerbates poor design!”
  - encourage “balanced” or “robust” design
- Check single-corner timing with all bells and whistles
- Optimization and fix-up
  - use incremental statistical timing
  - various diagnostics available
Myths about statistical timing

- “The main reason for statistical timing is within-die variations” ... “Variability is dominated by within-die variations” ... “The main frequency limiter is within-die variations”

- Random dopants are the only truly statistical phenomena
ACLV:12 product PSROs versus PSRO 1

(1) Systematic offsets  
(2) Scatter

Courtesy Anne Gattiker, IBM
Across-wafer variations

PSROs relative to reticle mean 05131SEA005.008

*Courtesy Anne Gattiker, IBM*
Interesting challenges: early/late splits and CPPR

Undue pessimism

Same buffer has different delays on early/late paths

late data
Interesting challenges: at-speed testing

From tester:
- RefClk
- StartTest
- Scan & Test Clocks
- Test Data

PLL → Clock control Logic → Clk

Chip Under Test

PLL Output

Clk

Scan Clock

Last Scan-Load Cycle
At-Speed Test
Scan Unload Cycles

[Courtesy Gary Grise]
Interesting challenges: at-speed testing

- Each point in the process space can have a unique critical path
- How to come up with a set of test vectors that tests for parametric variations in all parts of the process space?
- How to measure coverage thereof?
- How to test against workload-related defects?
- How to test against fatigue-related defects?
Interesting challenges: metrics for optimization

- **Slack is lacking**
  - different critical paths in different parts of the process space
  - slack is a distribution
  - slack does not give robustness information
  - relative ordering of paths
    - slack does not give correlation information

Other open problems

- Delay+power+noise variational modeling for 45 nm
- Robust optimization, fix-up
- Hierarchical robust design
Conclusions

- **Must protect against parametric variability**
  - high dimensionality, hence the need for statistical timing
  - hence the need for robust design
  - hence the need to check sensitivities
  - hence the need for statistical timing!

- **IBM has adopted a statistical-timing-based robust design flow for 65 nm ASICs**

- **Many open and interesting challenges remain**