Highly Sensitive Hall Magnetic Sensor Microsystem in CMOS Technology

Zoran B. Randjelovic, Maher Kayal, Radevoje Popovic, and Hubert Blanchard

Abstract—A highly sensitive magnetic sensor microsystem based on a Hall device is presented. This microsystem consists of a Hall device improved by an integrated magnetic concentrator and new circuit architecture for the signal processing. It provides an amplification of the sensor signal with a resolution better than $30 \mu V$ and a periodic offset cancellation while the output of the microsystem is available in continuous time. This microsystem features the overall magnetic gain of $420 V/T$.

Index Terms—CMOS Hall sensor, magnetic concentrators, microsystem, offset cancellation.

I. INTRODUCTION

IN MANY applications, a Hall element is used for contactless measurement such as linear and angular positions, electrical current and power, etc.

The Hall element fabricated by means of CMOS technology features mediocre characteristics [1]. It gives a weak output signal of the order of a few millivolts. This signal is often corrupted by sensor offset and noise. In addition, operational amplifiers (OPAMPs) made in CMOS technologies have a large offset that is subject to a temperature and aging drift. Therefore, the offset of OPAMPs must be periodically compensated for in continuous time.

In CMOS technology, the offset of the Hall element is often reduced by applying the spinning current method [15]–[17]. However, this method requires switching circuitry that is a source of switching noise. This paper deals with a new circuit architecture that can achieve the above requirements without using the spinning-current technique. It consists of an improved Hall device, an analog front-end with the dynamic offset cancellation, and a module for the automatic Hall device offset reduction.

The offset of the Hall element can be significantly reduced by applying the orthogonal coupling of two or four Hall elements [2]. Such a Hall device features an offset as low as $2 mT$, but it is still not enough to achieve a sufficient magnetic detectivity of the order of hundreds of microteslas. Therefore, we propose a further improvement of the Hall device by employing an integrated magnetic concentrator. This magnetic concentrator amplify the magnetic field, thus, improving the device’s signal-to-offset ratio.

Currently, several techniques are available for the offset cancellation of CMOS amplifiers [3]. Usually, the auto-zero methods need a passive components like a capacitor with analog switches or require a specific OPAMP architecture to achieve an offset compensation. The implementation presented in this paper can be used with a basic OA structure without requiring any special trimming process and no off-chip components. Therefore, the present design is very suitable for fully digital CMOS technology. In this paper, a mixed-mode design architecture reminiscent to that of [4] is presented. In addition, this microsystem does not need any external calibration, thanks to the self-adaptability to new operating conditions.

II. REDUCTION OF THE OFFSET OF A HALL EFFECT DEVICE

Any Hall element suffers from an offset. The main causes of the offset are: a process gradient over the chip, a mask-misalignment, and/or a mechanical stress imposed either in the fabrication process or packaging. The offset originating from the mask misalignment can be minimized by designing an appropriate and symmetrical layout of the sensor. A sensor geometry can also be optimized in terms of the offset [8]. The influence of the mechanical stress on the sensor offset can be reduced by orienting the sensor along crystallographic directions having the minimum value of the piezo-resistive coefficients [9]. In Fig. 1, the Hall effect sensors are rotated for 45 degrees in order to orient them along the $<110>$ crystallographic direction where...
The piezo-resistive coefficient take the minimum for an N-well Hall device [10].

The Hall effect sensor offset can be further reduced by using several sensors placed around a common center of symmetry [11]. An assembly of four Hall effect sensors situated around a common center of symmetry is shown in Fig. 1. This approach helps to reduce the sensor offset by a factor better than twenty, i.e., down to 2 mT.

The characteristics of the Hall element can be improved by coupling them with the integrated magnetic concentrator [12]. The principle of the operation of the integrated magnetic concentrator is illustrated in the left-hand side of Fig. 2. On the chip surface, a high-permeability ferromagnetic layer is deposited. In the middle of the chip, the ferromagnetic layer is etched and split into two pieces (see Fig. 2). Two ferromagnetic pieces are now divided by a very narrow air gap. Any external magnetic field parallel with the chip surface is captured by the magnetic concentrators. The magnetic flux passes through the magnetic concentrator. However, in the vicinity of the air gap, the magnetic flux splits into two parts. One part keeps flowing in the horizontal direction. The other part is the fringing magnetic field created around the air gap. The simulated magnetic field in the vicinity of the air gap is shown on the right-hand side of Fig. 2. The simulation result shows that the fringing magnetic field has a strong vertical component near the edges of the magnetic concentrator. Therefore, the magnetic concentrator will change the direction of the magnetic field from horizontal to vertical. This vertical component of the fringing magnetic field can be sensed by the Hall elements placed below the magnetic concentrator near the air gap.

Hence, the role of the integrated magnetic concentrator is two-fold: they change the direction of the magnetic field and they focus the magnetic flux. As a result, the Hall elements used to sense the vertical fringing magnetic field will see this magnetic field amplified. The amplification factor depends on several factors [12]: the width of the air gap, the shape of the magnetic concentrator, the position where the fringing magnetic field is measured, etc. In our case, the magnetic gain was about 5–5.6, whereas the saturation magnetic field of the concentrator is 20 mT.

In Fig. 1, two magnetic concentrators cover the sensors. The magnetic concentrators have an appropriate shape in order to focus the horizontal magnetic flux \( B \) toward the sensor area.

In Fig. 2, two magnetic concentrators cover the sensors. The magnetic concentrators have an appropriate shape in order to focus the horizontal magnetic flux \( B \) toward the sensor area. The Hall elements placed just below the edges of the magnetic concentrators near to the air gap (Fig. 1) can “see” the fringing magnetic field available in perpendicular direction. The sensors placed below each magnetic concentrator are grouped and connected in parallel. The inputs of the two groups of the sensors are also connected in parallel, and the outputs \( U_{1S} \) and \( U_{2S} \) are separated.

Since the resolution is dependent on both the signal-to-offset of the analog front-end ratio (SOAR) and the signal-to-offset of the sensor ratio (SOSR), the former must always be a bit better than the latter. Namely, there is no need to pay for better performance in terms of SOAR, while the SOSR cannot be further improved. The SOSR has been improved by using both the orthogonal coupling of the sensor and the magneto-concentrators. In accordance with the best SOSR we obtained, the current resolution of the magnetic microsystem is about 0.1 mT within the measurement range of ±20 mT. The measurement range is therefore limited by the saturation field of the magneto-concentrators.

### III. Microsystem Architecture

The top-level architecture of the microsystem is shown in Fig. 3. It consists of the sensor part, the analog front-end, and the module for the sensor offset cancellation. The whole system is driven by a digital control unit.
The sensor part encompasses an assembly of four symmetrical Hall elements mutually connected in such a way that their offsets cancel out. The assembly of the sensors can be represented by two identical sensors experiencing the same magnetic flux but in the opposite directions, as shown in Fig. 3. The outputs of the sensors are given by

\[ U_{1S} = U_{1SM} + U_{1Sof} \]
\[ U_{2S} = -U_{2SM} + U_{2Sof} \]

where \( U_{1SM} \) and \( U_{2SM} \) are sensor responses to a magnetic field and \( U_{1Sof} \) and \( U_{2Sof} \) are, respectively, the sensor offsets. As the sensors have a matched layout, the sensor offsets are almost identical and they partially cancel out. However, the sensor signals are summed as

\[ U_{LS} - U_{2S} = (U_{1SM} + U_{2SM}) + (U_{1Sof} - U_{2Sof}). \]

The analog front-end has two stages. The first stage is an auto-zeroed differential difference amplifier (DDA) [5] whose input offset voltage is better than 30 \( \mu \)V. The second stage is a buffer amplifier providing certain driving capabilities at the microsystem output. The analog front-end is repeated twice in order to provide continuous time output of the microsystem by employing the ping-pong technique [4]. The new microsystem architecture ensures a periodical amplifier offset cancellation and a continuous response at the output.

The output signal is

\[ U_{out} = A_{DDA} \cdot A_{BA}(U_{LS} - U_{2S}). \]

\( A_{DDA} \) and \( A_{BA} \) are the gains of the DDA and the buffer amplifier, respectively.

After substituting (3) into (4), the output signal is

\[ U_{LORE} = A_{DDA} \cdot A_{BA}(U_{1SM} + U_{2SM}) + A_{DDA} \cdot A_{BA}(U_{1Sof} - U_{2Sof}). \]

In (5), the first term is a desirable amplified output signal. The second term is an undesirable residual sensor offset, which is also amplified. It should be noticed that the useful parts of the sensor signals are summed, while the sensor offsets are subtracted. However, the residual sensor offset is not negligible and must be handled by using the module for the sensor offset cancellation.

The control unit drives the whole microsystem. It generates control signals needed for auto-zeroing the DDA amplifier and the functioning of the module dedicated to the sensor offset cancellation.

IV. ANALOG FRONT-END

The analog front-end electronics have to accomplish two goals: amplify an extremely weak input signal and provide enough driving current for a load at the output. Therefore, it is composed of a DDA and a buffer amplifier in Fig. 4.

The DDA has three input stages realized as separate differential pairs: M1–M2, M3–M4, and M5–M6. All of them are connected to the same active load, M7 and M8, so that there is a single common output at the node M. The first two DDA input stages (M1–M2 and M3–M4) are the inputs for the sensor signals, while the third (M5–M6) serves for defining the DDA closed-loop gain \( A_{DDA} \). The layout of the DDA input stages is carefully matched in order to prevent any asymmetry in amplifying the sensor signals. The differential pairs of the DDA input stages are made of P-MOS transistors operating in weak inversion in order to achieve a good tradeoff between \( g_m \) and power consumption.

An auto-zero technique for the DDA offset cancellation is presented in Section IV-A. This technique is an improved version of that one reported in [6].

The buffer amplifier, which is designed to drive a resistive load of less than 2 kΩ, is a symmetrical class AB amplifier.

A. Offset Cancellation Principle

Symbolic representation of a DDA is shown in Fig. 5. Three input differential pairs are depicted by the blocks denoted by \( g_{m1} \), \( g_{m2} \), and \( g_{m3} \), respectively. The \( g_{m1} \), \( g_{m2} \), and \( g_{m3} \) are the transconductances of the input transistors of the related differential pair, i.e., M1–M2, M3–M4, and M5–M6, respectively, in Fig. 4. The block denoted by \( \Sigma \) represents the common active loads M7 and M8. The output stage of the DDA is denoted by \( A_{R} \). This stage along with the compensation capacitor \( C_c \) acts as an integrator for \( I_{\text{eff}} \).

While the inputs of the differential pairs are tied to the same reference voltage, the offset current \( I_{\text{eff}} \) will arise at the node M shown in Fig. 5

\[ I_{\text{eff}} = g_{m1}U_{\text{dif}1} + g_{m2}U_{\text{dif}2} + g_{m3}U_{\text{dif}3} \]
where $U_{\text{off1}}$, $U_{\text{off2}}$, and $U_{\text{off3}}$ are the equivalent offset voltages referred to the input of a corresponding differential pair. The offset current will push the DDA output toward saturation.

Undesirable $I_{\text{off}}$, which is caused by the offset, can be cancelled out by injecting an external compensation current into the node M, as shown in Fig. 5. Since the $I_{\text{off}}$ may have arbitrary sign, the corresponding compensation current would be either sourced or sank. In order to provide both operations, two external current sources are employed: the constant current source $I_f$ and the programmable one $I_{\text{DAC}}$. The $I_{\text{DAC}}$ is the output current of a N-bits digital-to-analog converter (DAC). It ranges from 0 to $2I_f$. Therefore, the resolution of the DAC, i.e., the LSB of $I_{\text{DAC}}$, is

$$\Delta I_{\text{DAC}} = \frac{2I_f}{2^N}. \quad (7)$$

The $I_{\text{off}}$ taking values from the interval $-I_f$ to $I_f$ can only be canceled out. The residual error current is given by

$$I_{\text{err}} = I_{\text{off}} + I_f - I_{\text{DAC}}. \quad (8)$$

Therefore, $I_{\text{err}}$ can be controlled by $I_{\text{DAC}}$. The offset is completely canceled out only if $I_{\text{err}} = 0$. In reality, the error current $I_{\text{err}}$ can be reduced down to a resolution of the DAC, i.e., $\Delta I_{\text{DAC}}$. Therefore, the minimal value of the $I_{\text{err}}$ is always within the range $[-\Delta I_{\text{DAC}}/2, \Delta I_{\text{DAC}}/2]$.

Assuming that $g_{m1} \simeq g_{m2} \simeq g_{m3} \simeq g_m$ and $U_{\text{off1}} \simeq U_{\text{off2}} \simeq U_{\text{off3}} \simeq U_{\text{off}}, I_f$ becomes

$$I_f = 3g_m|U_{\text{off}}|_{\text{max}}. \quad (9)$$

Now, an offset cancellation algorithm can be constructed. The goal is to minimize $I_{\text{err}}$ by changing $I_{\text{DAC}}$ in (8). In turn, the DDA output voltage $U_{\text{out}}$ can be easily compared to the reference “0” voltage, while $I_{\text{err}} = 0$ yields $U_{\text{out}} = 0$.

Even for a very small $I_{\text{err}}$, the output voltage $U_{\text{out}}$ becomes large (the DDA operates in an open loop). Thus, $U_{\text{out}}$ is clamped to a supply voltage either $V_{DD}$ or $V_{SS}$, depending on the sign of $I_{\text{err}}$. This discussion clearly shows that the sign of $U_{\text{out}}$ should be regarded as the $U_{\text{out}}$ absolute value. Hence, during the execution of the offset cancellation algorithm, the alternative change of the sign of $U_{\text{out}}$ can be used to control $I_{\text{DAC}}$ so that $I_{\text{err}}$ is minimized. Here, a successive approximation algorithm [13] is chosen for determining the value of $I_{\text{DAC}}$.

During the offset compensation process, DDA operates in open-loop configuration. Therefore, the output voltage $U_{\text{out}}$ swings between positive and negative saturation voltage $\Delta U_{\text{sat}} = V^{+}\text{Sat} - V^{-}\text{Sat}$. The output voltage $U_{\text{out}}$ needs some time to establish a new value. This is a compensation decision time $\Delta t$. In accordance with (6) and (8), $\Delta t$ is

$$\Delta t = \frac{\Delta U_{\text{sat}}C_c}{|I_{\text{err}}|} = \frac{\Delta U_{\text{sat}}C_c}{(g_{m1}U_{\text{off1}} + g_{m2}U_{\text{off2}} + g_{m3}U_{\text{off3}}) + I_f - I_{\text{DAC}}}. \quad (10)$$

With an excellent matching of the DDA input stages, $\Delta t$ becomes

$$\Delta t = \frac{\Delta U_{\text{eff}}C_c}{3g_mU_{\text{off}} + I_f - I_{\text{DAC}}}. \quad (11)$$

The compensation decision time $\Delta t$ becomes infinite while $I_{\text{err}}$ tends to zero. Thus, it strongly limits the maximum clock frequency of the successive approximation algorithm.

B. Self-Adjusting Offset

In the preceding section, the offset cancellation method has been detailed. The implementation of this method is shown in Fig. 6.

The DDA output voltage $U_{\text{out}}$ is compared to the “0” reference voltage by using the buffer amplifier (BA), which is the second part of the analog front-end circuitry. Therefore, no additional comparator is needed. A successive approximation register (SAR) performs the successive approximation algorithm, whose measurement flow is shown in Fig. 7. In several successive steps, SAR finds an approximation of $I_{\text{off}}$ [see (6)], which is $I_f - I_{\text{DAC}}$. After performing the offset cancellation algorithm, the approximated value of $I_{\text{off}}$ as a digital word is stored in the register of the SAR. This digital word is converted to an analog current by employing a digital-to-analog converter (DAC). The DAC is implemented as an 8-bit M-2M MOS ladder [7], thus achieving a small silicon area.

C. Self-Adjustment of the Sensor Offset

A model of the Hall element offset is shown in Fig. 1. An asymmetry between the resistances in the Wheatstone bridge creates the sensor offset. Therefore, this offset is well correlated to the input resistance of the sensor. While the sensor is biased by a constant current source, the sensor offset voltage $U_{\text{off}}$ is directly proportional to the input sensor voltage $U_{\text{in}}$

$$U_{\text{off}} = KU_{\text{in}}. \quad (12)$$
This property of the Hall sensor can be used for the sensor offset cancellation [15]. The block scheme of the system for the sensor offset cancellation is shown in Fig. 8.

The output voltage of the above system is

\[ U_o = A(U_{SM} + U_{Soff}) - GU_{in}. \]  

(13)

The offset term can be eliminated if the following condition is satisfied:

\[ G = A \frac{U_{Soff}}{U_{in}}. \]  

(14)

Now, the constant of proportionality \( k \) in (13) becomes \( k = G/A \).

Fig. 9 shows the implementation of the principle presented in Fig. 8. This realization requires two assumptions: DDA has been already auto-zeroed and during a few ms after turning on the system and the entire microsystem is kept out of any magnetic field, i.e., \( U_{SM} \) in (13) is zero.

A R-2R ladder current DAC [7] is the most important for an automatic adjustment of the \( G \) in (14). The output current of the DAC is always a fraction of a reference current \( I_r \). This fraction \( m_1 \cdot I_r \) or \( m_2 \cdot I_r \) in Fig. 9 can be determined by the digital input of the DACs. Two DACs must be used in order to cancel out either positive or negative sensor offset. The part of the \( I_r \) injected into the node \( K \) is summed with the current \( U_{out}/R_1 \), which is the output voltage of DDA converted to a current

\[ I_{sm} = (m_1 - m_2) \cdot I_r + (U_{1Soff} - U_{2Soff}) \frac{A_{DDA}}{R_1} \]  

(15)

where \( A_{DDA} \) is the gain of DDA.

\( I_r \) is the sensor input voltage converted to a current

\[ I_r = \frac{U_{in}}{R}. \]  

(16)

The goal of the sensor offset self-adjustment algorithm is to find the coefficients \( m_1 \) and \( m_2 \) so that \( U_0 \) is zero, which is equivalent to \( I_{sm} = 0 \) in (15). One of the coefficients \( m_1 \) and \( m_2 \) is always zero. They can be found by employing a serial algorithm [13], as follows: \( m_1 \) and \( m_2 \) are implemented as a counters, the counter \( m_1 \) is counting down from its maximum to zero while the counter \( m_2 \) is reset to zero, then, the counter \( m_1 \) stays at the zero while the counter \( m_2 \) is counting up to its maximum. The algorithm is terminated when the comparator (comp) detects \( U_0 = 0 \), i.e., when it changes its state.

At the end of the self-adjustment algorithm, the gain \( G \) in (17) is found by replacing (16) in (15) as

\[ G = (m_2 - m_1) \frac{R_1}{R_2}. \]  

(17)

where either \( m_2 \) or \( m_1 \) is zero (\( m_1 \) and \( m_2 \) are the outputs of the corresponding counter). Therefore, both \( m_1 \) and \( m_2 \) range between 0 and \( 2^N - 1 \), where \( N \) is the number of the DAC bits.

In the current implementation, \( N = 6 \). Now, (17) becomes

\[ |G| = \frac{2^m - 1}{2^N - 1} \frac{R_1}{R}; \quad \exists m \in [0, 2^N - 1]. \]  

(18)

Once \( m_1 \) and \( m_2 \) are evaluated, the microsystem is ready for use. Then, the sensor offset is tracked and its instantaneous value is subtracted from the microsystem output \( U_0 \).

D. Continuous Time Operation

An auto-zero technique for the amplifier offset cancellation requires an interruption of the amplifier operation. During the
auto-zero phase, the inputs of the amplifier must be disconnected and tied to the reference voltage. During this time, the amplifier output is not available. In addition, the auto-zero procedure must be performed repeatedly in order to prevent a drift of the amplifier output voltage. The amplifier output voltage drifts are mostly due to the temperature drift of the amplifier offset. Hence, the auto-zero technique is often combined with some other techniques in order to provide a continuous time output of the amplifier. One of techniques referred to as a ping-pong technique [4] is presented in this section.

The basic idea behind the ping-pong technique is to double the part of the system that is subject of the auto-zero procedure. Therefore, the system contains two identical circuits: A and B (see Fig. 10). While circuit A is operating, circuit B is under calibration (auto-zeroing) and vice versa. At the end of every auto-zero cycle, the circuits A and B swap their roles. Thus, the output of the system is provided in continuous time. However, while circuits A and B swap, there is a short transition period in which the system output is not clearly defined.

The operation of the microsystem is driven by the control signals shown in Fig. 11.

Special care is taken in order to avoid a spike generation during the transition period. An intermediate phase is introduced between the auto-zero and the operation phase as shown in Fig. 12. Before swapping circuit A with B, the output of circuit A, which is currently active, is mirrored to the output of circuit B, which has just been calibrated. As the outputs of circuits A and B are made equal, there is no spike generated. However, a small ramp of output voltage occurs because circuits A and B do not have an equal residual offset after performing the auto-zero procedure.

E. Control Unit

The functionality of the design architecture, which is shown in Fig. 11, is provided by closing or opening corresponding signal paths. All signal paths are routed by employing CMOS switches also shown in Fig. 10. The switches are driven by five different control signals denoted by $\phi_1$ through $\phi_5$. Phases of the control signals are shown in Fig. 11.

The control unit drives circuits A and B of the microsystem throughout four different states: continuous time operation (currently A in Fig. 10), auto-zero (currently B in Fig. 10), follower, after auto-zeroing of B, the output voltage of A is mirrored to the output of B, see Fig. 12, swapping the roles of A and B.

While one of the circuits, A or B, is in the auto-zero state, the control units perform the successive approximation algorithm. At the end of the algorithm, a converted value of the corresponding DDA offset is stored in a register of the control unit (SAR in Fig. 3). This value is repeatedly evaluated every eight periods of the clock (see Fig. 11).

The control signals are generated in the digital part of the architecture. This part also includes a low-frequency oscillator (clock) with $f_c = 8$ kHz. This frequency is then divided down to 1 Hz, which is the operating frequency of the microsystem. Accuracy of the clock frequency is not important. Both applied the offset cancellation and the ping-pong methods are insensitive to the clock frequency variation.
V. EXPERIMENTAL RESULTS

The whole microsystem is fully integrated by means of 0.8-μm CMOS digital, 5-V technology. The chip is shown in Fig. 13.

Table I shows several of the most important parameters of the microsystem. In this table, the worst-case values of both the output referred offset and the residual input offset are given. The measured value of the residual input referred offset of the microsystem is lower than 30 μV.

In Table II, the microsystem magnetic characteristics are given.

The presented circuit is able to achieve an SNR of 65 dB. Since the signal-to-offset ratio yields 57.3 dB, the offset is still the limiting factor.

The residual offset has also been measured over a wide temperature range: –10 °C to 80 °C. The variation of the residual offset was around 3 μV. All these measured results confirm the ability of the electronic interface to amplify a very weak sensor signal down to a few millivolts.

During the DDA offset cancellation phase (see Fig. 3), the successive approximation algorithm needs some time for decision making. This time, Δt is given by (10) and (11). In case there is no offset cancellation, i.e., \( I_f = I_{DAC} \) in (11), Δt takes the minimal value. Assuming that \( U_{off,max} \) of DDA is 5 mV and using all needed data from Table I, one obtains \( \Delta t_{\text{min}} = 100 \mu s \), which corresponds to the maximal clock frequency of \( f_{\text{clk,max}} = 10 \text{ kHz} \). However, (10) shows that \( \Delta t \) tends to infinity while the error current \( I_{err} \) becomes very small. Therefore, \( f_{\text{clk,max}} \) is an upper limit and a clock frequency should be as low as possible in order to achieve better performances.

In present implementation, a clock of \( \sim 1 \text{ Hz} \) is chosen. The clock frequency is well below \( f_{\text{clk,max}} \) in order to obtain the lowest residual offset of the DDA. Therefore, the decision time \( \Delta t \) is very long. This long time can be reduced by disconnecting the DDA compensation capacitor \( C_C \) (see Fig. 5) during the auto-zero phase.

After performing the offset cancellation algorithm, there is still some residual offset of a corresponding DDA. This residual offset is amplified along with the signal while DDA operates. Furthermore, after every offset cancellation cycle the residual offset is not the same. The maximum value of the residual offset is limited by the number of bits used for the offset cancellation procedure, but its real value can range between zero and that maximum. Therefore, at the output, the residual offset appears amplified, and its peak-to-peak value may vary for 7 mV, in accordance with the data given in Table I.

The ping-pong technique provides a continuous time output of the microsystem. The analog front-end circuitry of the microsystem is doubled so that one circuitry is under use, while the other one is under calibration, as shown in Fig. 10. However, when these two circuitries swap their roles, there is a ramp at the microsystem output. The ramp occurs due to a difference in residual offsets of DDAs, as well as a difference in the gain of circuits A and B in Fig. 12. These gains differ due to mismatches of the layout, a process gradient, imposed stress, etc. Therefore, the microsystem output voltage may ramp for less than 14 mV while the swap of circuits A and B takes place.

VI. CONCLUSION

The new microsystem architecture for a Hall magnetic sensor microsystem has been presented. The microsystem is able to measure a weak magnetic field within the range of ±6 mT with a resolution better than 0.1 mT. The microsystem is very robust and it can operate within a wide temperature range from –10 °C to 80 °C with an error of ±10 μT. The microsystem encompasses a Hall device and interface electronics.

The Hall device is a novel structure composed of four orthogonally coupled Hall elements and a magnetic concentrator. This
magnetic concentrator amplifies the magnetic signal by a factor of 5 up to 5.6. Therefore, the signal-to-offset and the signal-to-noise ratios are improved by the same factor, and, thanks to the magnetic concentrator, the Hall elements can be orthogonally coupled in a new manner, resulting in a signal twice as large, while the sensor offsets mutually cancel out (see [3]).

The detection of a very low magnetic field, typically 100 μT, is required for applications such as Bank note magnetic properties mapping, long-distance position detection, or low current sensing. In such cases, the limiting factors are the equivalent magnetic noise (which is the noise over sensitivity ratio) and equivalent magnetic offset (offset over sensitivity ratio). Adding flux concentrators on Hall sensors increases the sensitivity without any degradation of noise and offset. It pushes down the limits for low field measurements. However, the saturation of flux concentrators does limit the dynamic range of the Hall sensor microsystem. This is why such sensors will be used in field detection applications or low-current sensing for low-cost sensor microsystem. This is why such sensors will be used in

The presented interface electronics is a mixed-mode circuitry. The digital part of the electronics is independent of technology. In addition, there is no longer any need for precision analog components such as capacitors. The applied auto-zero offset cancellation method is suitable for a fully digital CMOS technology.

The ping-pong technique is used to provide a continuous time output. At any moment, one part of the system is under calibration while its counterpart is operating and vise versa. Therefore, the microsystem continuously self-adjusts to new operating conditions.

The accuracy of the implemented offset cancellation method is 30 μV. Therefore, the residual offset referred to the output may range up to 7 mV. Since the continuous time output is provided by employing the ping-pong technique, after swapping sequences (see Fig. 12), a ramp of around 14 mV, in the worst case, may appear at the output. This undesired output voltage swing is periodic and arises every nine clock periods.

**REFERENCES**


Radevoje S. Popovic was born in Yugoslavia (Serbia) in 1945. He received the Dipl. Ing. degree in applied physics from the University of Beograd, Yugoslavia, in 1969 and the M.Sc. and Dr.Sc. degrees in electronics from the University of Nis, Yugoslavia, in 1974 and 1978, respectively.

From 1969 to 1981, he was with Elektronska Industrija Corporation, Nis, Yugoslavia, where he worked on research and development of semiconductor devices, and later became head of the company’s CMOS department. From 1982 to 1993, he worked for Landis & Gyr Corporation, Central R&D, Zug, Switzerland, in the field of semiconductor sensors, interface electronic, and microsystems. There, he was responsible for research in semiconductor device physics (1983–1985), and for microtechnology R&D (1986–1990), and was appointed vice president (Central R&D) in 1991. In 1994, he joined the Swiss Federal Institute of Technology in Lausanne (EPFL), Switzerland, as Professor for microtechnology systems. His current research interests include sensors for magnetic, optical and mechanical signals, sensor microsystems, physics of submicron devices, and noise phenomena.

Hubert Blanchard was born in Switzerland in 1972. He received the Ph.D. degree in microengineering from the Swiss Federal Institute of Technology in Lausanne (EPFL), Switzerland, in 1999 for his work on the fabrication of high aspect ratio submicrometer feature size employing electron beam lithography, conducted at King’s College London.

In 1995, he joined the Institute of Microsystems at EPFL, where he worked on Hall sensors for low magnetic field measurements and on current sensors. After receiving the Ph.D. degree, he joined the R&D department of LEM Holding, world leader in the market of isolated current measurement. His current research and development interests include magnetic sensor microsystems and new technologies for the realization of current sensors.