Making Sense Out of Variability Measurements

Borivoje Nikolić
University of California, Berkeley
bora@eecs.berkeley.edu
Outline

- What kind of variability matters?
- Test structures for measuring variability in logic
- Analysis of variability measurements in 90nm CMOS
Temporal vs. Spatial Variability

- **Nature of process variability**
  - Within-die (WID), Die-to-die (D2D), Wafer-to-wafer (W2W)
  - Systematic vs. random

- **Spatial variability/correlation**
  - Device parameters (CD, $t_{ox}$, …)
  - Supply voltage, temperature

- **Temporal variability/correlation**
  - Within-node scaling, Electromigration, Hot-electron effect, NBTI, self-heating, temperature, SOI history effect, supply voltage, crosstalk [Bernstein, IBM J. R&D, July/Sept 2006]
## Systematic and Random Device Variations

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Random</th>
<th>Systematic</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel Dopant Concentration Nch</td>
<td>Affects $\Delta V_{th}$ [1]</td>
<td>Non-uniformity in the process of dopant implantation, dosage, diffusion</td>
</tr>
<tr>
<td>Gate Oxide Thickness Tox</td>
<td>Si/$\text{SiO}_2$ &amp; $\text{SiO}_2$/Poly-Si interface roughness[2]</td>
<td>Non uniformity in the process of oxide growth</td>
</tr>
<tr>
<td>Gate Length L</td>
<td>Line edge roughness (LER)[3]</td>
<td>Lithography: Proximity effects, RET, OPC, PSM</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Resist development, etching, etc</td>
</tr>
</tbody>
</table>

Systematic, lithography-induced variation dominates

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What to Measure?

Present design methodology is pessimistic

Variations

- Systematic Layout Dependent
- Die to Die (D2D)
- WID
- Spatial Correlation

3σ Total Variations

Foundry

Within Die (WID)

Circuit Designer

Correlated

Worst Scenario

Chip

Correlation

Die to Die (D2D)

WID

Spatial Correlation
Chip Yield Depends on Inter-Path Correlation

- Yield = Pr (max delay of K paths < clock period)
- K = 1 gives highest yield

Correlated paths reduce impact of variation

Bowman et al, JSSC, Feb 2002
Chip Yield Depends on Inter-Gate Correlation

- Yield = \( Pr(\text{sum of } n \text{ delays} < \text{clock period}) \)
- \( \rho = 0 \) gives highest yield through increased averaging

Non-correlated gates in a path reduce impact of variation
Impact of Variation on Performance Gain

Decrease in frequency due to variation offsets gain due to scaling

Overall gain in performance decreases with scaling

Variations diminish scaling benefits

Bowman et al, JSSC, Feb 2002.

$3\sigma_{L\text{WID+D2D}} = 20\% * L$

$\sigma_{L\text{WID}}^2 = 50\% * \sigma_{L\text{WID+D2D}}^2$
Step-and-Scan Lithography
**Lithography: Proximity Effects**

- **Gate CD is a function of its neighborhood**
  - Isolated line
  - Dense lines

- **Test structures:**
  - Poly line resistance
  - I-V characteristics of individual devices
  - Logic structures (ring oscillators)
Lithography: Density Effects

- Denser features: More accurate line width and less variation.
- Dense lines are wider than isolated lines.

Measurement structure: Poly lines with varying density
Lithography: Optics

- Defocus
- Lens aberrations:
  - Spherical aberrations
  - Astigmatism
  - Coma

- Spherical aberrations - affect the reticle-level features
  - Stepper dependent
- Coma affects individual features
  - Chip-location dependent
Lens Aberrations – Coma Effect

- Coma effect: optical aberration due to lens imperfection.
- Causes mirrored structures to display non equivalent properties
- Systematic shift between the 2 layouts

Image of a circular dot shows a tail

prints differently from

Measurement structure: Non-symmetric poly lines
Step and Scan Lithography

- **Slit direction:**
  - Lens aberration in the slit
  - CD’s more correlated

- **Scan direction:**
  - Dosage, scan speed and other fluctuations
  - CD’s less correlated

Measurement structure: Poly lines with varying orientation
Lithography: Flare

- Light scattering and reflections
- More stray light under dark features in the mask
  - Local flare depends on the density of chrome in the mask

Measurement structure: Uniform poly lines; varying spatial density
Gate Length (CD) Measurements

Exhaustive ELM poly-CD measurements (280/field):

Combine voltage drop measurements with sheet resistance measurements from neighboring Van der Pauw structures to get CD.

J. Cain and C. Spanos, SPIE'03.
Decomposition of Spatial CD Variation

\[
\text{Average Wafer} = \text{Scaled Mask Errors} + \text{Across-Field Variation}
\]

\[
\text{Across-Wafer Variation} + \text{Die-to-Die Variation} + \text{“Random” Variation}
\]

Friedberg and Spanos, SPIE’05
RO Arrays: 90nm CMOS Test-Chip

- Layout effects: Density, symmetry, gate stacking, metal coverage

12 layout configurations

L.T. Pang, VLSI’06
RO Arrays: 90nm CMOS Test-Chip

16 columns, 1mm

Tile Array

10 rows, 1mm

ADC

90nm CMOS test-chip die photo

L.T.Pang, VLSI'06

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RO Arrays: Leakage Current ($I_{\text{LEAK}}$)

- NMOS subthreshold leakage

L.T. Pang, VLSI'06
RO Arrays: Single Slope ADC

- Thick oxide, 2.5V transistors
- Folded-cascode amplifier

\[
\frac{\Delta t_{\text{ref}} - \Delta t_s}{\Delta t_s} \sim \frac{I_s}{I_{\text{ref}}}
\]
RO Arrays: Frequency (F)

- RO enable and mux output select signals
- On-chip frequency divider

Results: Poly Density - Single Gates

- Max $\Delta F$ between layouts $\sim 10\%$
- Within-die $3\sigma/\mu \sim 3\%$, weak dependency on density ($<1\%$)
Results: Poly Density- Stacked Gates

- Weaker effects, max $\Delta F$ between layouts $\sim 3\%$
- Within-die $3\sigma/\mu \sim 3\%$, no dependency on stacking
Results: Poly Density - Leakage Current

- Single gates: low poly density → faster and leakier
- Denser layout → smaller variation ($\sigma/\mu$)

99% Confidence Intervals

 Counts:
- 36 chips
- Fastest
- Slowest

Log($I_{leak}$)
Coma Effect – Lens Aberrations

- Measurable coma effect (~1%)
Variation of mean F: $3\sigma/\mu$ die-to-die ~ 15%

Radial pattern: faster and leakier at wafer center
Results: Spatial Correlation

Dotted lines = 99% confidence bounds

- $3\sigma/\mu$ within-die variation ~ 4%
- $\rho$ depends on gate orientation and direction of spacing
- ROs with rotated gates have lower variation
Results: Step and Scan Photolithography

- Slit direction more correlated
Results: D2D Correlation

Scatter Plot for Mean of 36 chips

Strong correlation for die to die variation

Strong die-to-die correlation
Conclusions: What to Do?

- Consider proximity effects
- Incorporate systematic vs. random; correlation
- D2D > 15%. On-chip compensation circuits
- L2L > 10%. Regular layouts
- WID < 4%. Exploit spatial correlation in different directions