Design of High-Speed Serial-Links in CMOS
(Task ID: 930.001)

SRC Research Review

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Design of High-Speed Serial-Links in CMOS

- Technical Thrust
  - Circuit Design
- Students
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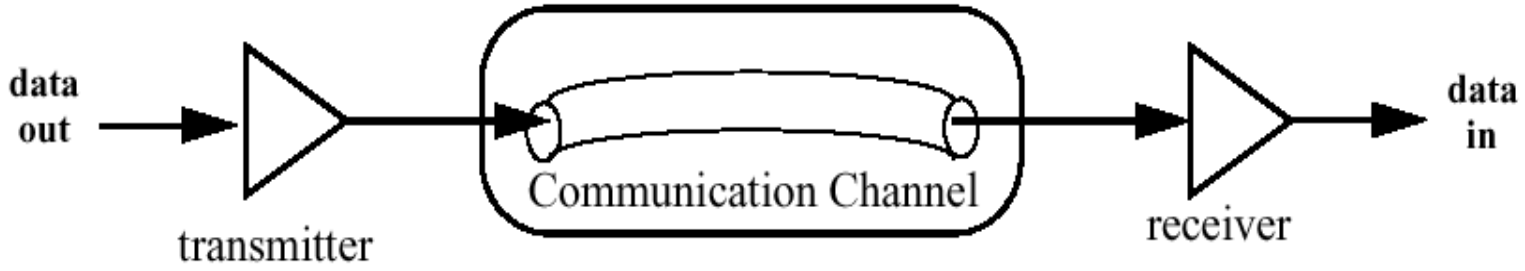
Accomplishments for 2003

- Developed adaptive/synchronization techniques for frequency channelized receivers.
- Designed a serial-link prototype based on frequency channelization.
  - Currently in fabrication.

Outline of Talk

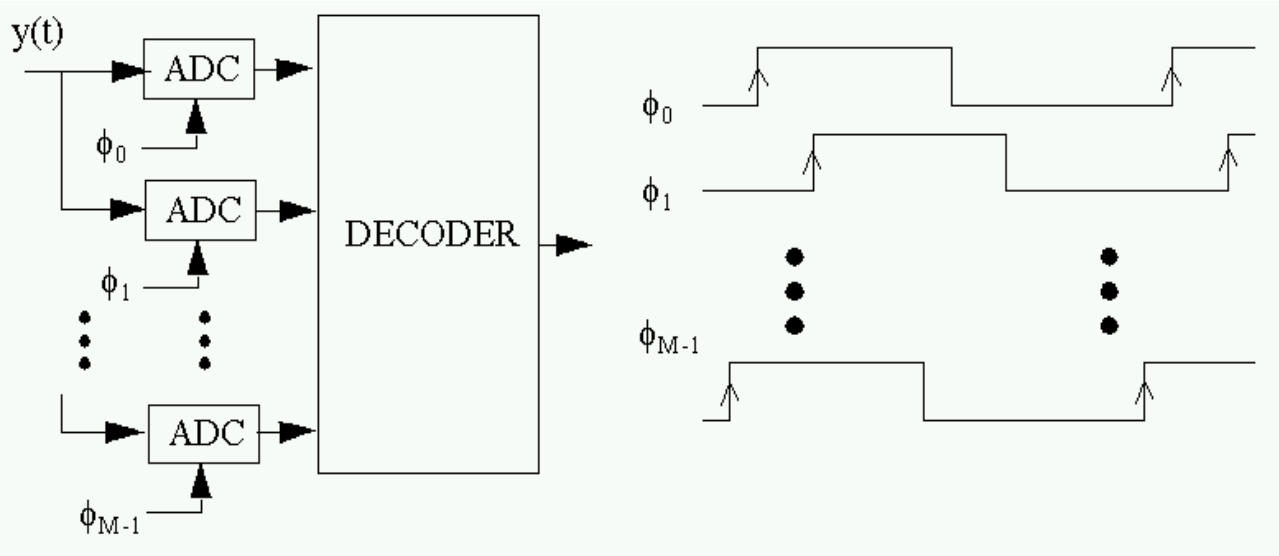
- Adaptive frequency channelized receiver.
- Frequency channelized receiver implementation.
- Research plans for next year.

Background in Signaling



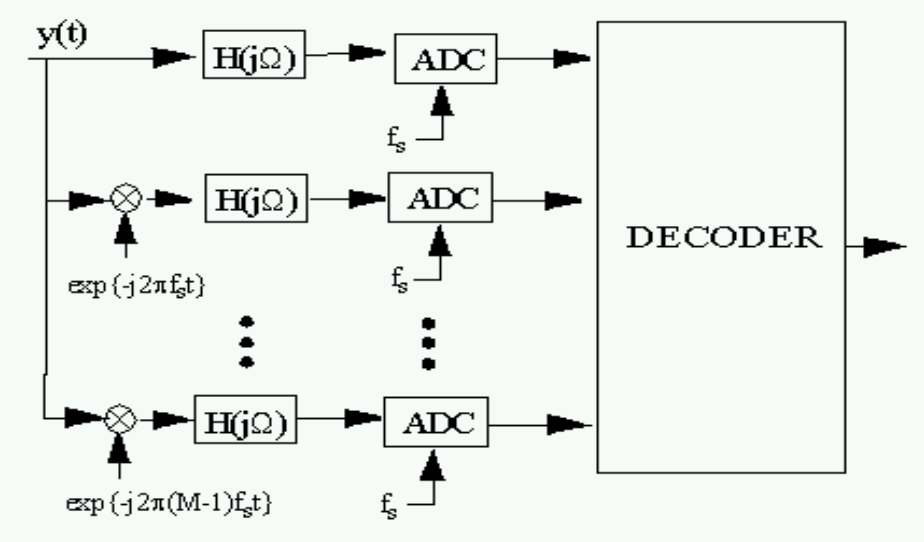
- Transistor mismatches.
- On-chip noise.
- Inter-symbol interference.
  - Wire losses and package parasitics.
  - Finite receiver/transmitter bandwidth.

Existing Architecture – Time-Interleaved Receiver



- Sample at approx. Nyquist rate; 2-4 bit ADC's (flash).
- ADC sees the full bandwidth of the input signal.
  - Sample/hold circuitry difficult to design.
  - Sensitive to sampling jitter and sample-time offsets.
- Large input capacitance.

Frequency Channelized Receiver

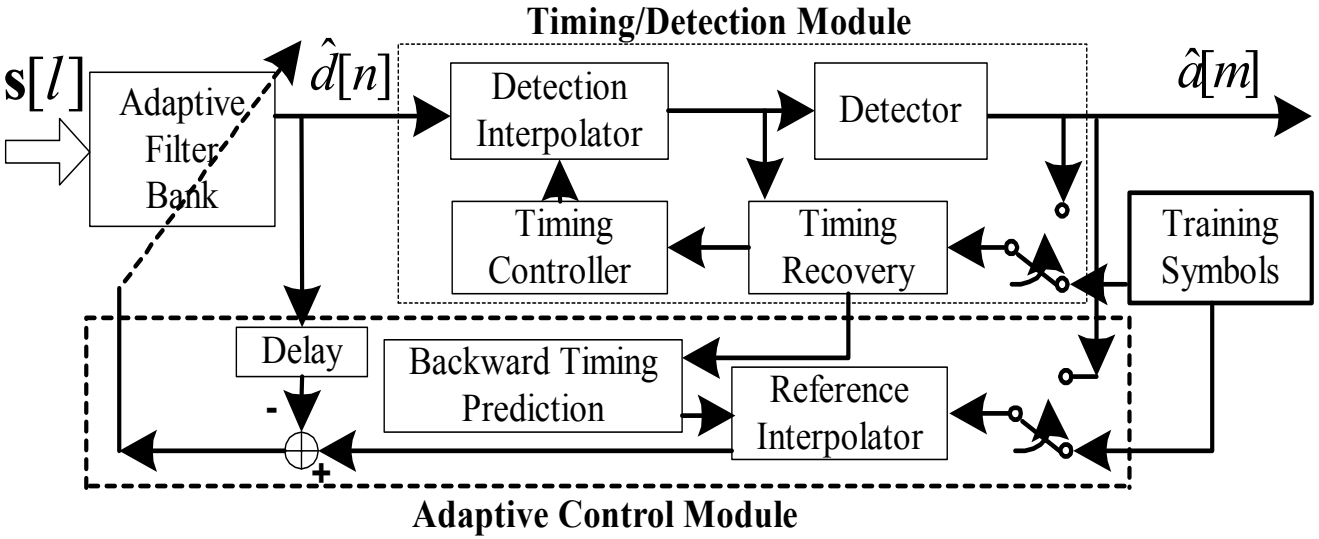


- Achieves the same effective sampling frequency as time-interleaved receiver using the same number of ADCs.
- ADC input bandwidth reduced.
  - Sample/hold circuitry relaxed.
  - More robust to sampling jitter even with mixer phase noise present.
- Reduced input bandwidth.

Adaptive Frequency Channelized Receiver Overview

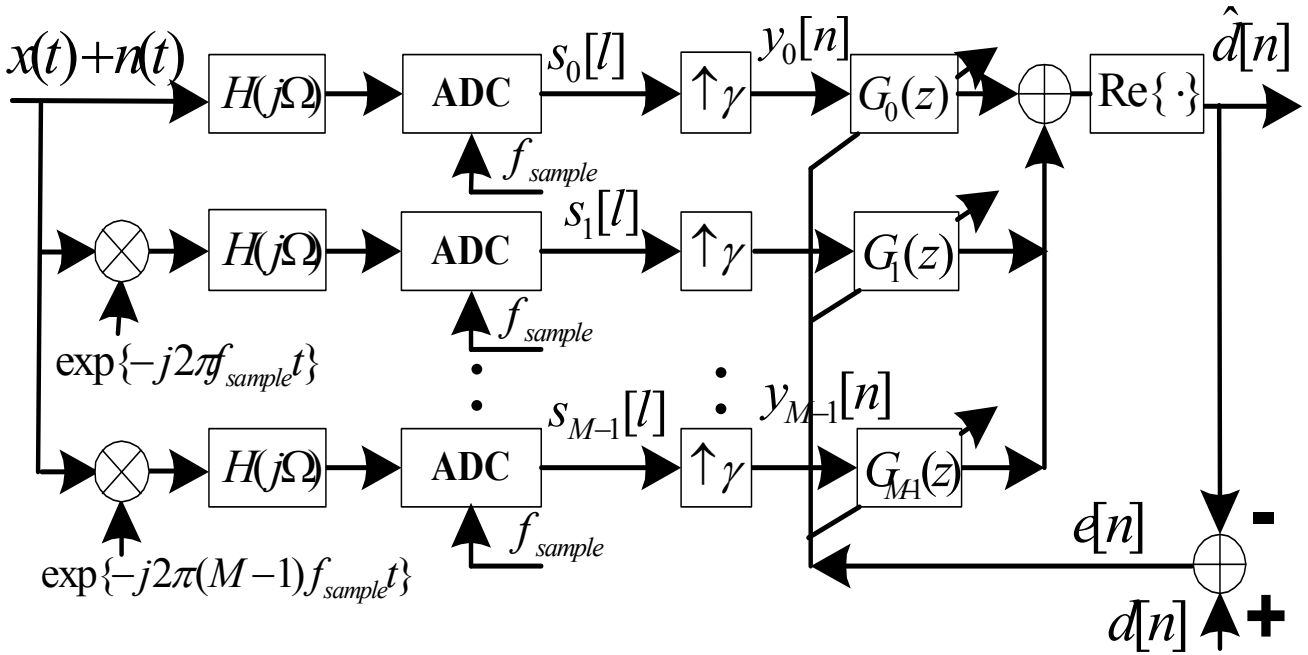
- Adaptive synthesis filter bank.
  - Equalize distortion caused by the propagation channel and reconstruct the channelized signal for detection.
  - Analog analysis filter bank not accurately known at design time.
  - Error signal based on the detected symbol.
- Digital interpolators.
  - ADC sampling frequency generally not an integer multiple of the symbol frequency.
  - Interpolation must occur after synthesis filter bank.

Overall Receiver Structure



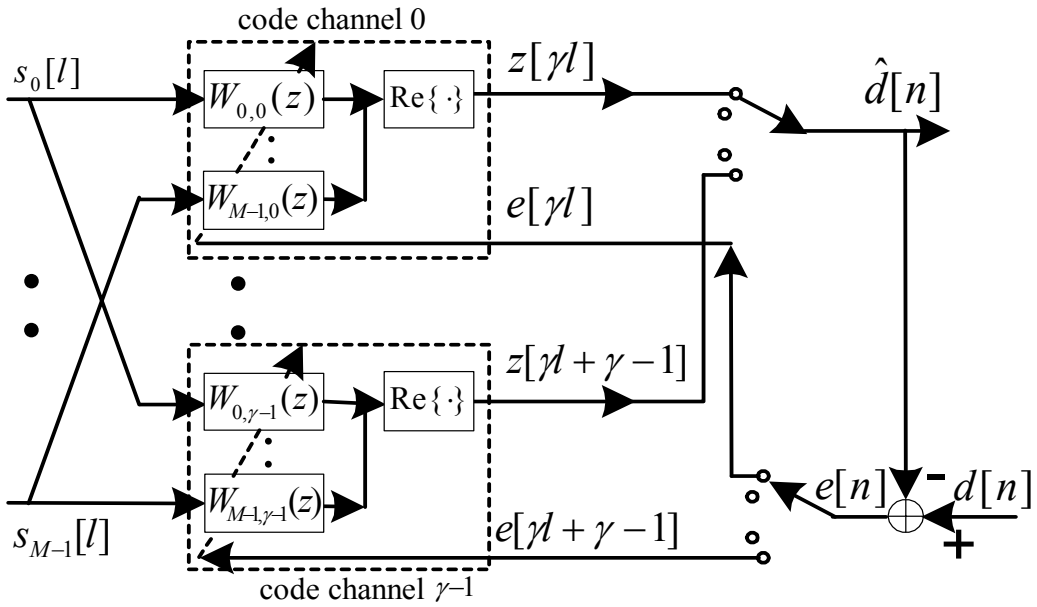
- Timing/detection module extracts timing information and detects transmitted symbol.
- Adaptive control module generates error signal used to update the adaptive synthesis filter bank.

Adaptive Filter Bank (1)



- Effective sampling frequency $f_{eff} = \gamma \cdot f_{sampl}$, where $\gamma = 2M - 1$.
- Re{} applied since transmitted signal is a baseband real signal.

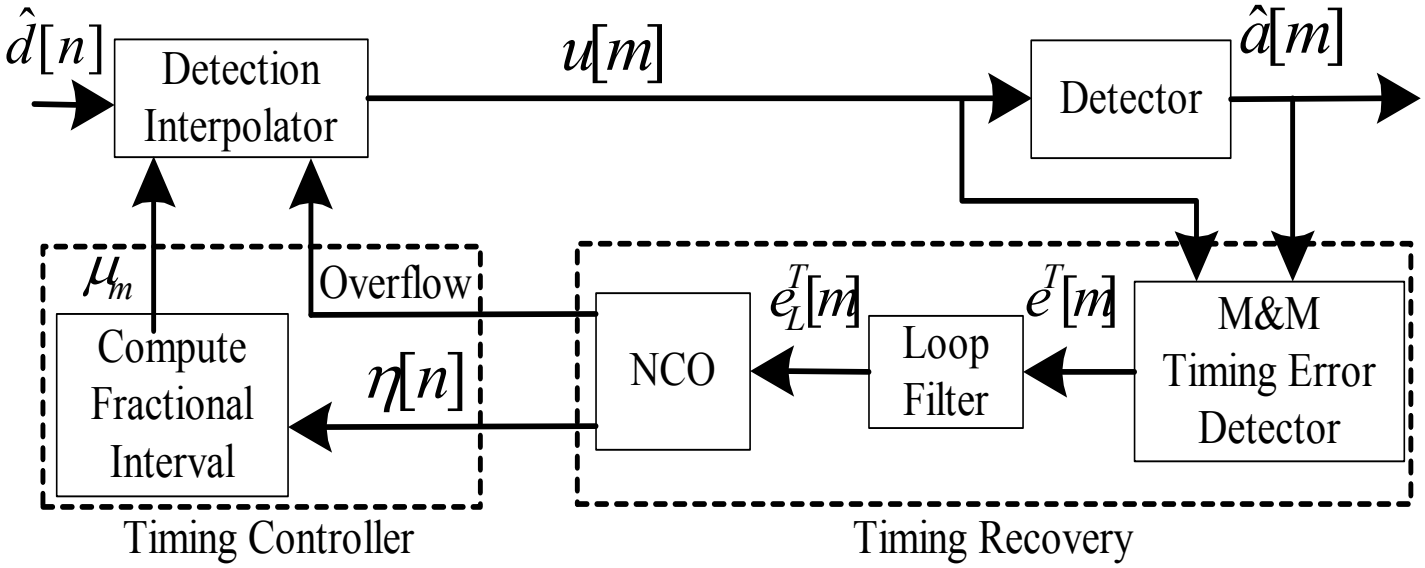
Adaptive Filter Bank (2)



- Synthesis filter bank is LPTV system with period γ.
- Each code channel estimates one of γ consecutive samples.
- LMS adapts each code channel independently:

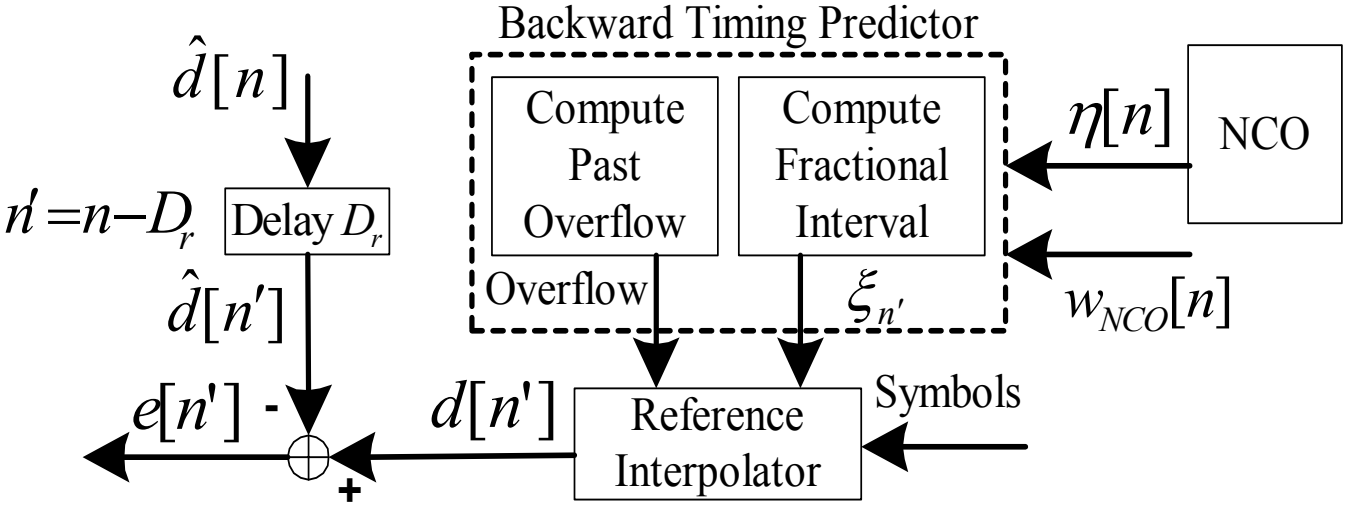
$$\mathbf{w}_i[l+1] = \mathbf{w}_i[l] + \varepsilon \mathbf{s}[l] e[\gamma l + i]$$

Timing/Detection Module



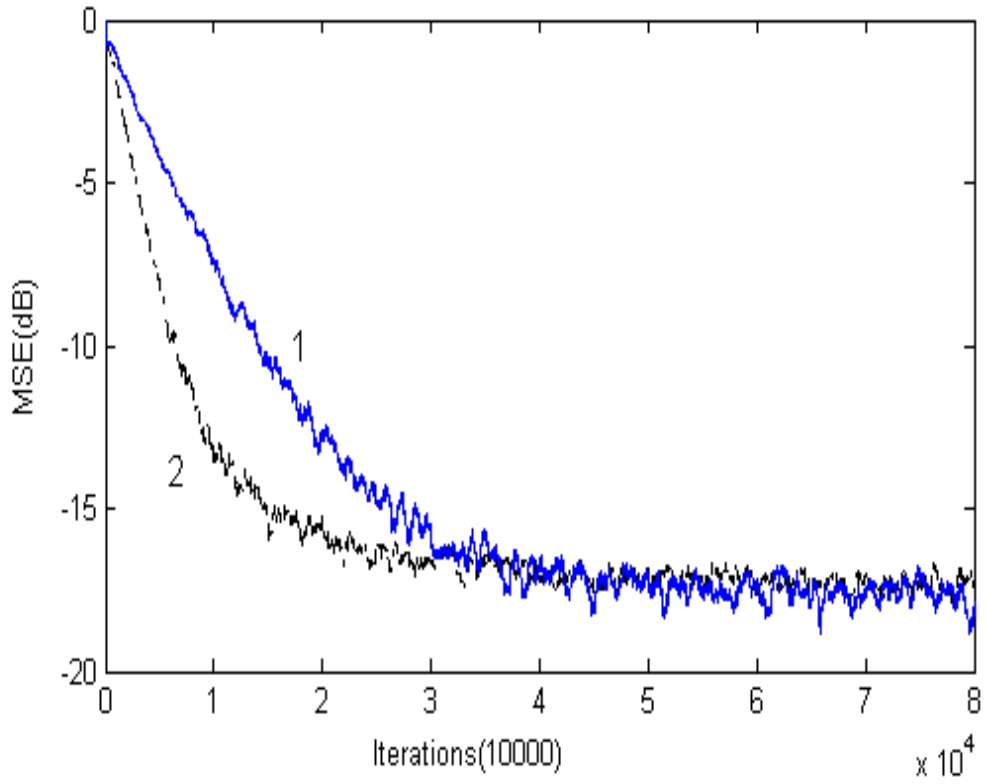
- Detection interpolator resamples to symbol rate.
- Timing recovery determines timing error that controls interpolator.

Adaptive Control Module

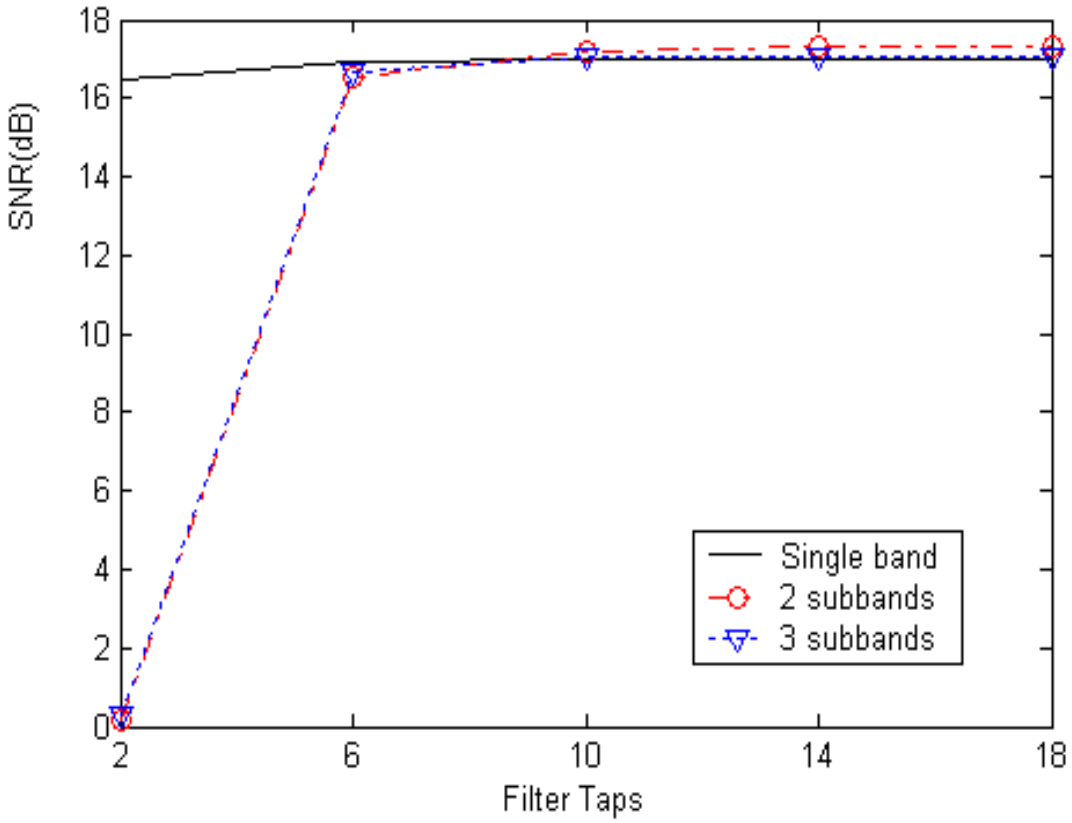


- Backward timing predictor calculates timing information of delayed filter bank output based on current NCO state.
  - Delayed for used in DD mode.
- Reference interpolator generates desired reference signal.

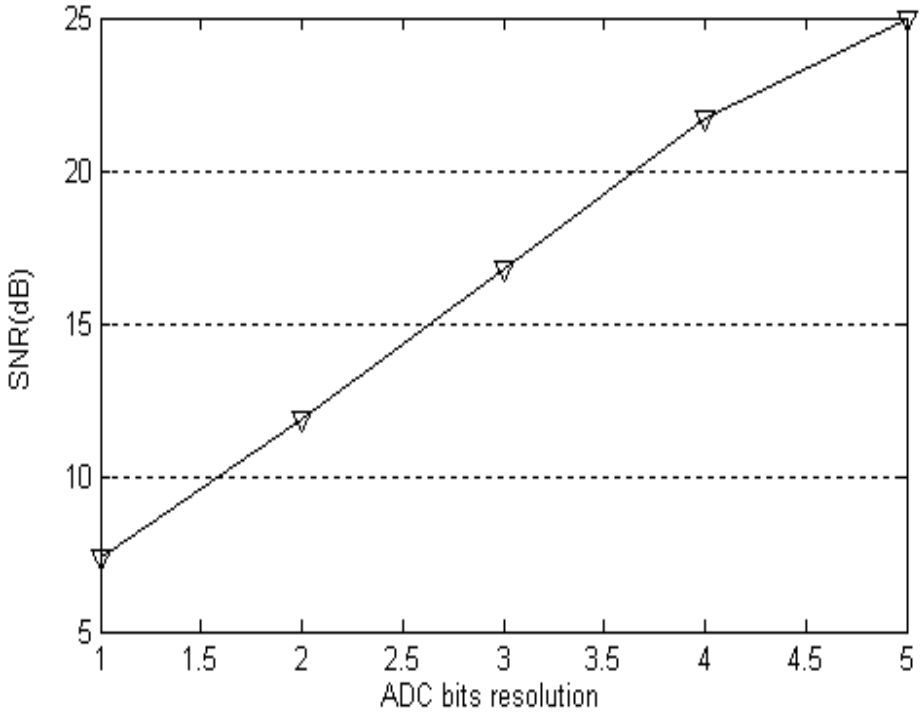
Simulation Results – Convergence Performance



Simulation Results – Effect of Filter Taps



Simulation Results – Effect of ADC Bits



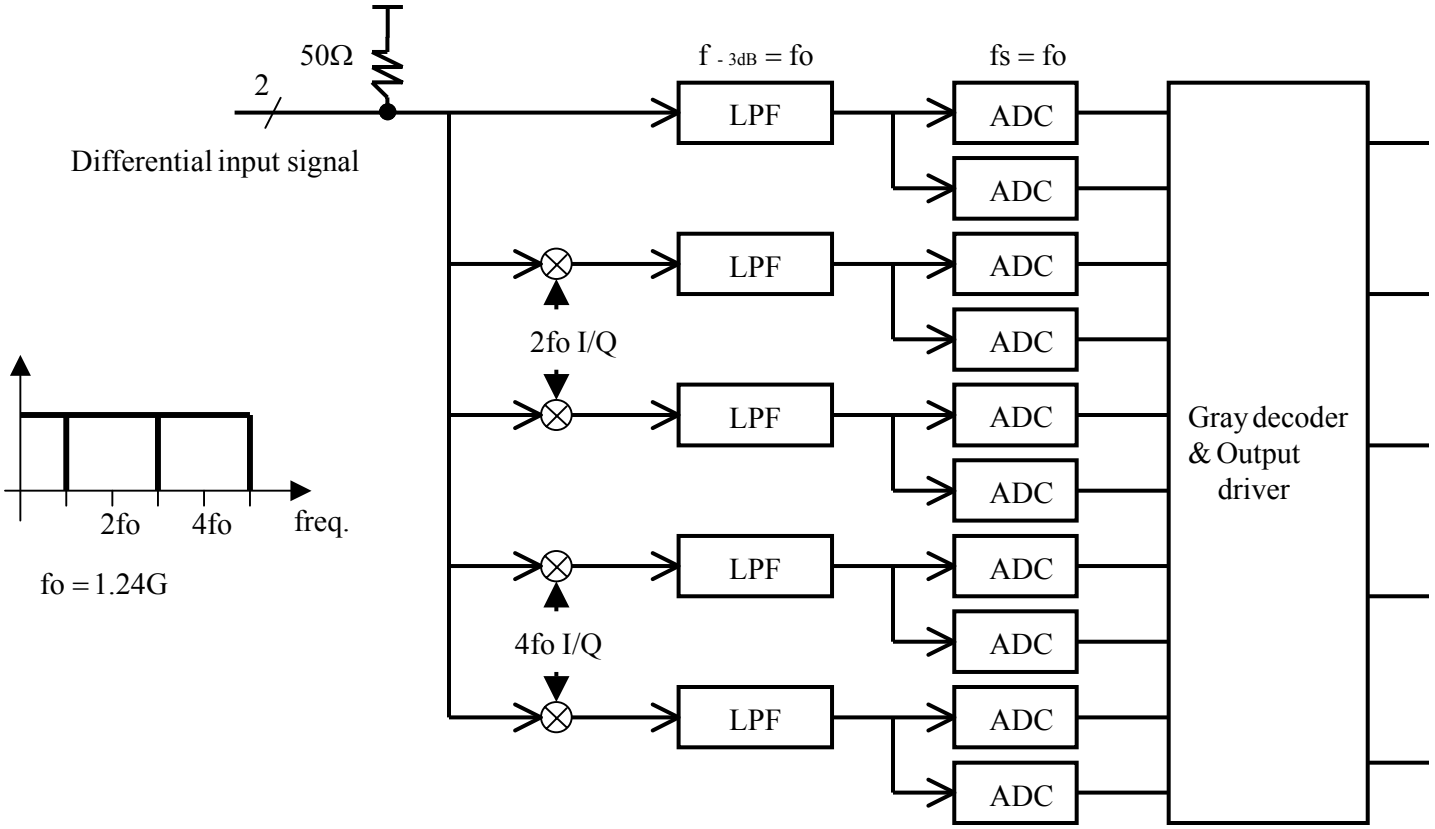
Summary of Adaptive Frequency Channelized Receiver Work

- Based on frequency channelized signals, an adaptive synchronization/detection scheme is described.
- Performance of proposed receiver is similar to that of a single channel receiver.
  - Convergence time is slightly longer.

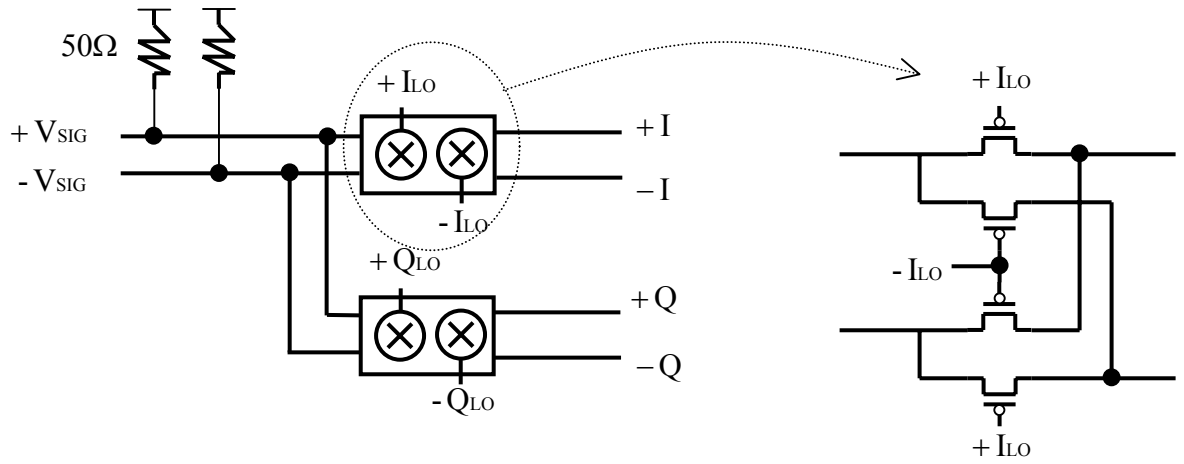
Implementation of Frequency Channelized Receiver

- A frequency channelized receiver excluding the digital back-end has been implemented in 0.25um CMOS.
- Symbol rate of 10Gsymbols/sec.
- Three frequency subbands and 10 3-bit ADC's each operating at 1.24Gsamples/sec.
- Currently in fabrication.

System Architecture

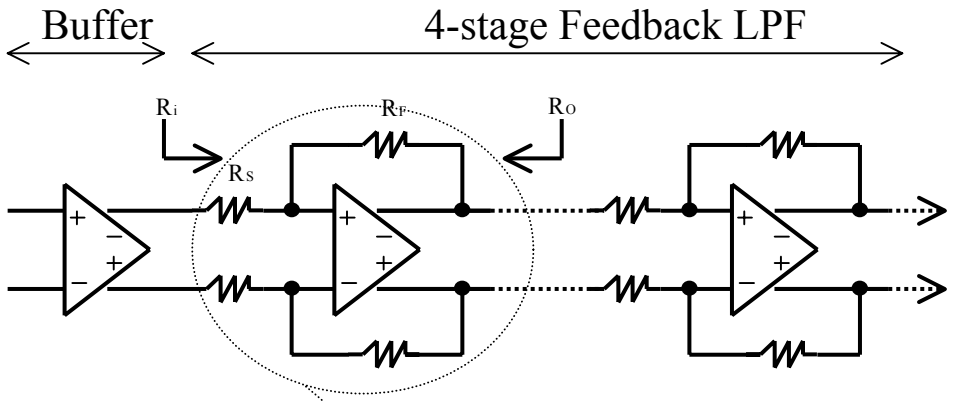


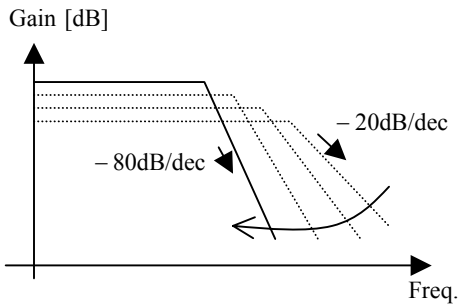
Quad-Phase Mixing

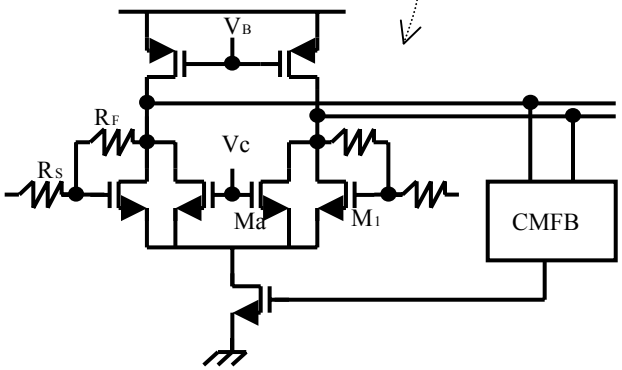


- Conventional passive double balanced mixer.
- 50 ohm matching allows wide input bandwidth: ~6.5GHz.

Low Pass Filtering



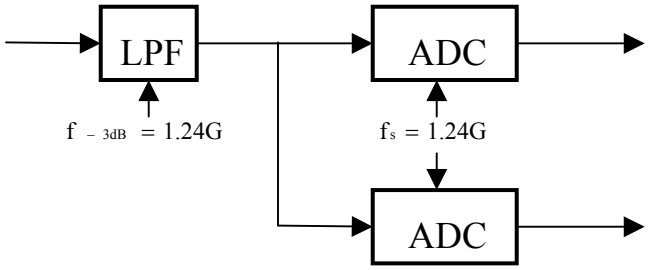




- Vc adjusts gm of transistor M1 to control gain without affecting bandwidth.
- Achieves 20dB gain with 1.4GHz 3-dB bandwidth.

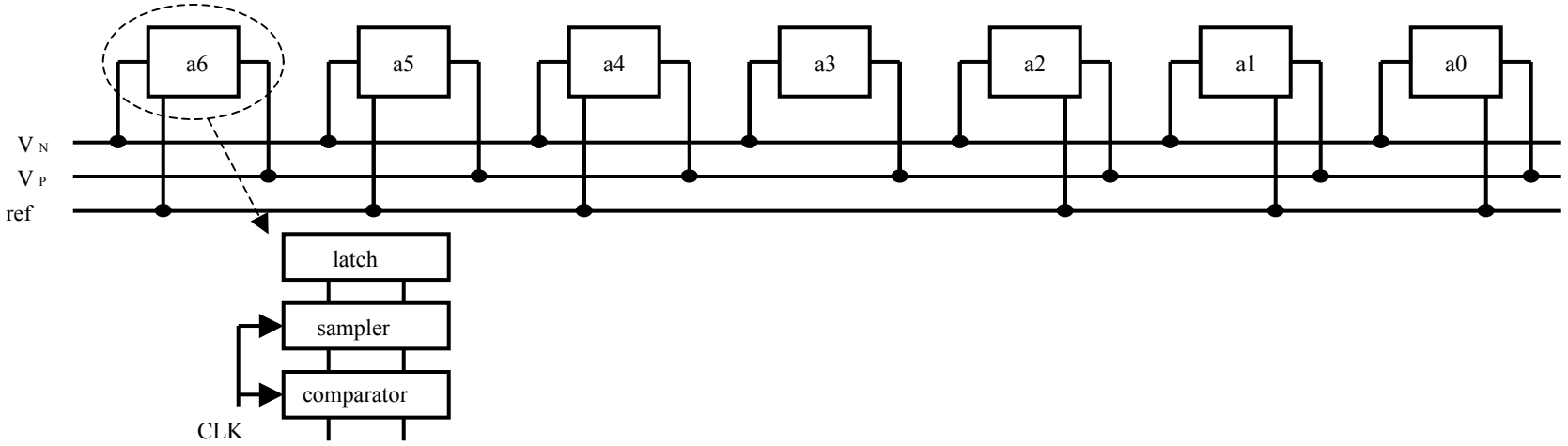
ADC Architecture

• 2 Time-interleaved 3-bit ADC

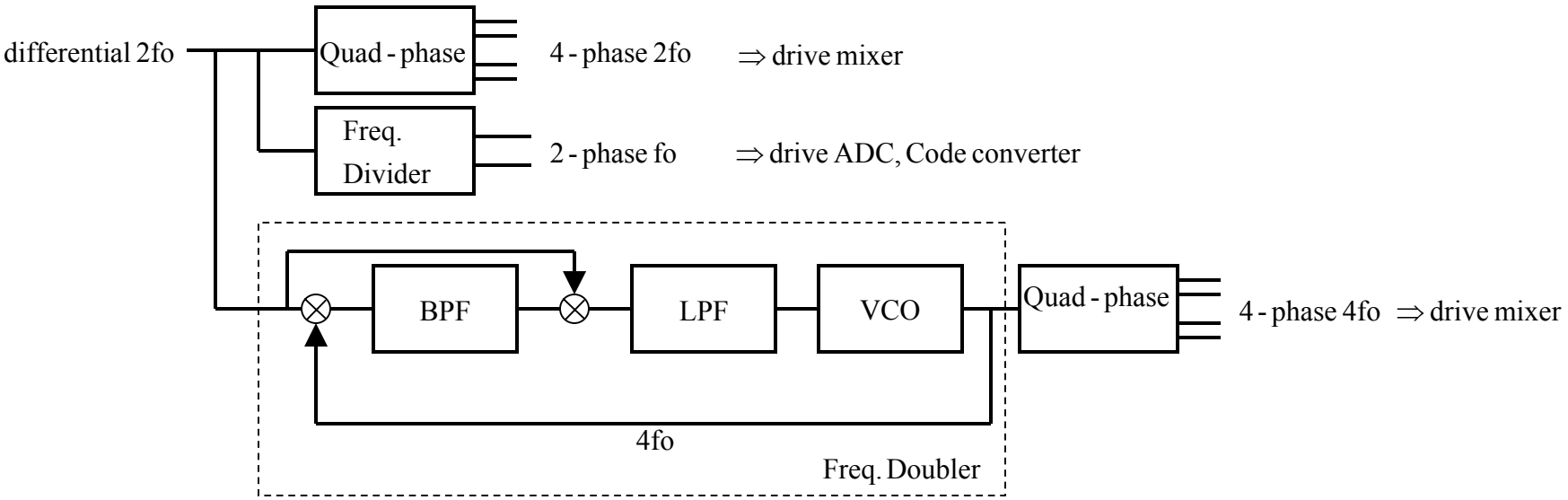


• Each 3-bit ADC samples at 1.24Gsps.
• Effective sampling rate/channel is 2.48Gsps.
• No offset scheme necessary.

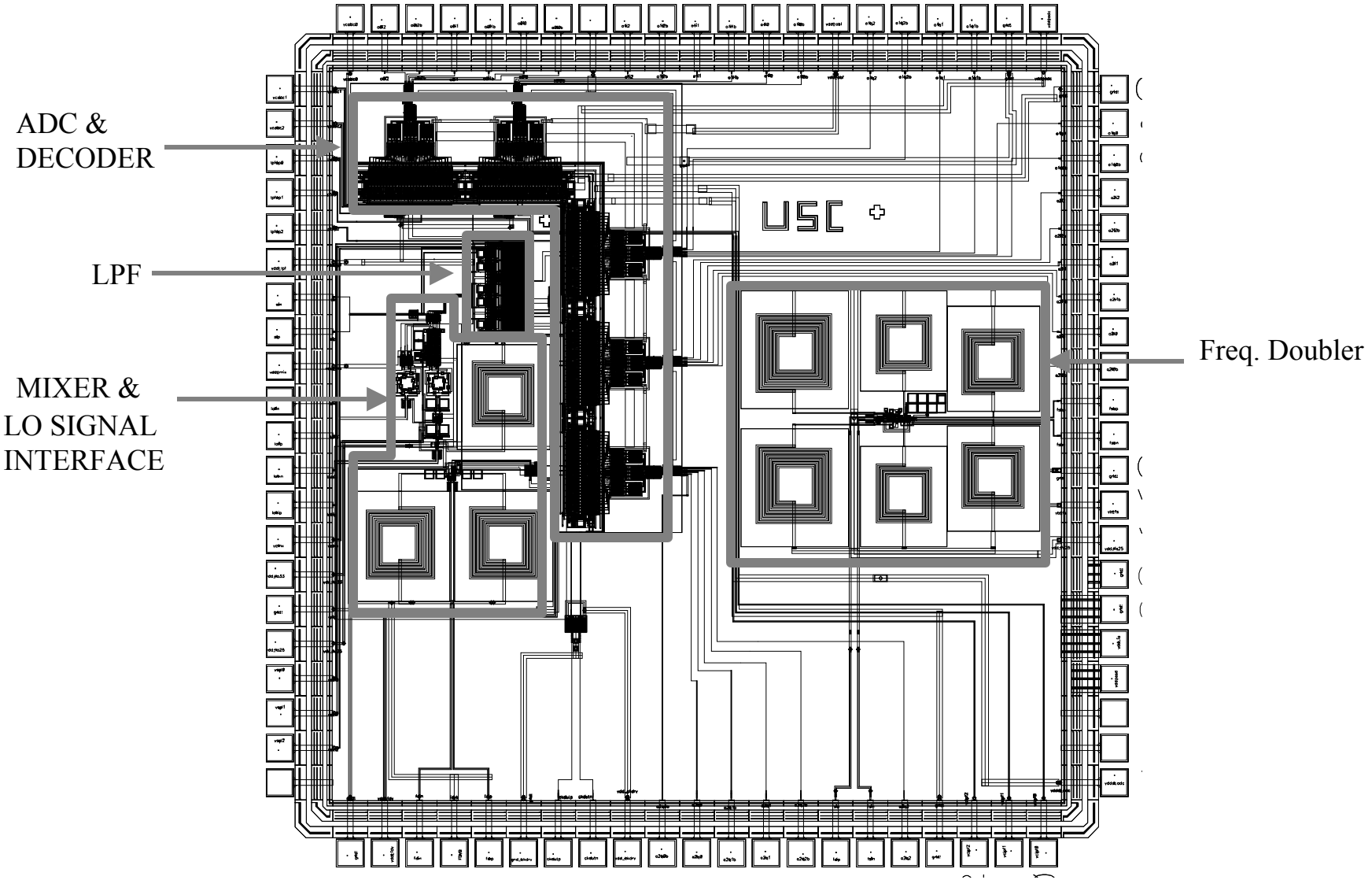
• ADC architecture



Local Oscillator Frequency Generation



Chip Layout



Plans for Next Year

- Fabricate and test design prototype to verify main concepts.
- Develop/analyze more sophisticated adaptive reception algorithms based on maximum-likelihood sequence estimation (MLSE).
  - Faster convergence speed and higher performance.
- Design transmitter/receiver to support higher rates.
  - Multi-level signaling.
  - OFDM based communication systems.