Low Voltage PLL Design Tolerant to Noise and Process Variations

SRC ICSS Program Review
September 9, 2003

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Anticipated Result: Development of low voltage design techniques that can be used for the design of noise tolerant PLLs and frequency synthesizers. Self-calibration methods will be developed to tune out process/temperature and voltage variations yielding a robust design.
Task Deliverables

- New noise tolerant design techniques for low voltage PLLs in digital processes (Jun-30-2004)
- Verification of low voltage noise tolerant design techniques using fabricated test structures (Mar-1-2005)
- Digital control techniques for blocks within the PLL (Mar-31-2005)
- Verification of self-calibration and digital control techniques using fabricated test structures (Dec-1-2005)
- Design of a 1.2 volt PLL for a 5GHz wireless LAN application in a 0.1-um CMOS process (Mar-31-2006)
Executive Summary

• Accomplishments during the past year
  ✓ Project start date Apr-1-2003
  ✓ Initial study of power supply noise sensitivity on ring oscillators
Executive Summary

• Future direction
  ✓ Develop noise tolerant low voltage design techniques for PLLs utilizing ring and LC based oscillators
  ✓ Develop effective digital programmability for self-calibration
Executive Summary

• Technology transfer & industrial interactions
  ✓ Interactions with National Semiconductor

• Publications
  ✓ None

• Patentable inventions, patent applications
  ✓ None
Outline

• PLL Design Issues
• Ring-oscillator based VCOs
• Supply noise analysis
• Future work
Phase-Locked Loop Design Issues

- Low Noise
- Tuning Range
- Inductor Design
- Jitter/Phase Noise
- High Speed
- Supply Noise
- Substrate Noise

Diagram showing the components of a Phase-Locked Loop (PLL) including:
- Phase Detector
- Loop Filter
- VCO
- Frequency Divider
PLL Building Blocks

• Voltage controlled oscillator
  ✓ Wide tuning range and low jitter/phase noise
• Charge-pump based loop filter
• Frequency divider
• Phase detector
Phase Noise/Jitter vs. Tuning Range

- LC oscillators tend to be low noise, narrow tuning range
- Ring oscillators tend to be high noise, wide tuning range
Source of Ring Oscillator Phase Noise

- **Intrinsic Noise**
  - Thermal
  - Flicker
- **Environmental Noise**
  - Power Supply
  - Substrate
Ring Oscillator Topologies

**Maneatis Delay Cell**

**Lee/Kim Delay Cell**

<table>
<thead>
<tr>
<th></th>
<th>Maneatis</th>
<th>Lee/Kim</th>
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<tbody>
<tr>
<td>Intrinsic Noise</td>
<td>Poor</td>
<td>Good</td>
</tr>
<tr>
<td>Power Supply Noise</td>
<td>Good</td>
<td>Poor</td>
</tr>
<tr>
<td>Tuning Range</td>
<td>Wide</td>
<td>Narrow</td>
</tr>
</tbody>
</table>

Which has better overall phase noise performance?
Lee/Kim Cell Operation

- No tail current source $\rightarrow$ rail-to-rail swing
- Positive feedback through cross coupling $\rightarrow$ fast switching
- No mechanism to reduce power supply noise coupling to output
Conversion of CM Noise to DM Noise

- Power supply noise causes CM noise at the output
- Resistor mismatch converts CM noise to DM noise
- Non-linear loads cause resistor mismatch

Need a practical, linear load
Maneatis Symmetric Load

- First order approximation to linear resistor I-V curve
- Only symmetric up to $V_{CTRL} \rightarrow$ limited output swing
Resistor Matching Symmetric Load

- Differential output swings equal and opposite amounts and sees the same slope $\rightarrow$ matched resistance
- Assumes the output swings around $V_{CTRL}/2$
Improving Noise of Maneatis

If output CM level is not $V_{CTRL}/2$, resistance matching is poor.
More *Linear* Load

- $-V_{RES}^2$ term of $M_2$ cancelled by $+V_{RES}^2$ term of $M_1$
- Approximate current equation: $I_{RES} = k'W/LV_{RES}$
- Valid for $0 \leq V_{RES} \leq V_{CTRL}$
More Linear Load I-V Curves

$I_{RES}$ vs. $V_{RES}$

- Linear
- Symmetric

Resistance vs. $V_{RES}$

- Symmetric
- Linear

Fairly linear even above $V_{CTRL}$ → No need to limit swing

More Linear Load I-V Curves
Implementation of Linear Load

- A source follower is used to implement the voltage drop
Power Supply Noise Generation

- Works for either $V_{DD}$ or ground noise
- Noise variance = $\frac{kT R_0}{C R_1}$
- Able to sweep noise variance by sweeping $R_0$
Initial Simulation Environment

1.8-V 0.18 µm CMOS, \( f_{\text{osc}} = 3.3 \text{GHz} \), \( \Delta f = 1 \text{MHz} \)

(1/f noise not included in the model)

Figure of Merit (FOM) defined:

\[
FOM(\Delta \omega) = 20 \log(f_0) - L(\Delta \omega) - 10 \log(P)
\]

• Lee/Kim has better intrinsic noise rejection since the FOM is higher for small amounts of $V_{DD}$ noise

• Maneatis has better $V_{DD}$ rejection since the corner where $V_{DD}$ noise starts degrading FOM is higher
Ground Noise Sensitivity

- Both oscillators are less sensitive to ground noise
- Unlike $V_{DD}$ case, there is a point at which the superior ground rejection of Maneatis outweighs the superior intrinsic noise rejection of Lee/Kim
Noise on Both $V_{DD}$ and Ground-Fixed

- Set ground variance at a fixed level ($10^{-2}$) and sweep $V_{DD}$
- Overall FOM follows ground only FOM when $V_{DD}$ noise is small and $V_{DD}$ FOM when $V_{DD}$ noise is large
Linear Load Power Supply Sensitivity

- Better intrinsic noise rejection than Maneatis
- Similar $V_{DD}$ noise rejection
- Worse ground noise rejection
Dual Tail Current Latch Delay Cell

- The best power supply rejection achieved due to the tail current source (like the Maneatis oscillator)
- The best intrinsic noise rejection due to the positive feedback (like the Lee/Kim oscillator)
- This cell combines the two positive features
Latch Power Supply Sensitivity

- Best intrinsic noise rejection
- Similar $V_{DD}$ noise rejection compared to Maneatis
- Worse ground noise rejection
Which Oscillator is Best?

*Depends on the amount of $V_{DD}$ and ground noise!*

- A series of plots show trends
  1. Fixed amount of ground noise
  2. Plot $V_{DD}$ noise variance vs. FOM as before
  3. Increase ground noise and repeat
Ground noise variance = $10^{-8}$ V²

![Figure of Merit](image-url)
Ground noise variance = \(10^{-6} \, V^2\)

![Graph showing the relationship between Mean-Squared Power Supply Noise (V^2 on Log Scale) and Figure of Merit for different noise sources. The graph compares Lee/Kim Latch and Maneatis Latch noise levels.](image)

- **Lee/Kim Latch**: Blue triangles
- **Maneatis Latch**: Green squares
- **Gnd noise**: Black circles
- **Latch**: Cyan stars
- **Linear**: Gray dashed line

Figure 10.2: Mean-Squared Power Supply Noise (V^2 on Log Scale) vs. Figure of Merit for different noise sources.
Ground noise variance = $10^{-4} \, V^2$
Ground noise variance = $10^{-2} \text{ V}^2$

![Diagram showing Mean-Squared Power Supply Noise vs. Gnd noise variance, with curves for Lee/Kim, Maneatis, and Latch.]
Conclusions From Plots

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<thead>
<tr>
<th>$V_{DD}$ Noise</th>
<th>Ground Noise</th>
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<tr>
<td></td>
<td>Small</td>
</tr>
<tr>
<td>Small</td>
<td>Latch</td>
</tr>
<tr>
<td>Medium</td>
<td>Latch</td>
</tr>
<tr>
<td>Large</td>
<td>Latch</td>
</tr>
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- Latch type (Latch, Lee/Kim) are usually better than source coupled pair (Maneatis, Linear)
- Linear load oscillator never has the highest FOM overall, but it does often outperform the Maneatis
  ✓ Viable alternative to Maneatis as proposed
Next Steps

- Explore 0.1\(\mu\)m predictive models from Berkeley
- Power supply noise sensitivity analysis of various ring \textit{and} LC based oscillators
- Develop noise tolerant low voltage design techniques for oscillators and PLLs using ring \textit{and} LC based oscillators
- Develop effective digital programmability for self-calibration
- Start interaction with Industry Liaisons to align practical future direction