Charge-injection-induced dynamic screening and origin of hysteresis in field-modulated transport in single-wall carbon nanotubes

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Gate modulated transport in semiconducting single-wall carbon nanotubes shows significant hysteresis in their transfer characteristics. The origin of this hysteresis is generally attributed to the screening of the gate voltage due to the movement of mobile charges/ions in the inherent presence of a trapping/detrapping mechanism in the adjacent dielectric, as in conventional silicon metal-oxide-semiconductor field-effect transistors. However, recent works have conjectured that the screening charges may originate from the nanotube itself. From an extensive study of the temperature dependence of the hysteresis behavior in nanotube field-effect transistors the authors experimentally establish this alternative mechanism, in which the screening charges are injected from the nanotube itself into the surroundingdielectric. Any detailed trapping/detrapping mechanism does not appear to play a significant role, and all experimental results can be simply explained in terms of a capacitive charging of the surrounding dielectric due to the charge injection. © 2006 American Institute of Physics. [DOI: 10.1063/1.2362586]

The ability to modulate the electronic conductance of semiconducting single-wall carbon nanotubes (s-SWCNTs) with a gate voltage has led to enormous advances in understanding their fundamental transport properties. This also makes them a possible candidate for future nano-scale electronics. Field-effect transistors (FETs) based on s-SWCNTs typically show a p-type unipolar behavior. As a result, for gate voltages below a threshold \( V_G < V_{th} \), a nanotube channel is conducting, and many nanotube transport properties are experimentally obtained in this region. Accurate estimations of nanotube properties are, however, hampered by the presence of a hysteresis in the transfer characteristics between the forward and reverse sweeps of the gate potential. The amount of hysteresis is dependent on a number of experimental parameters, like the time delay before a sweep is started from one end (hold time \( \tau \)), range \( \pm V_G \) and rate (\( dV_G/dt \)) of the gate voltage sweep, and temperature \( T \). Although annealing and surface passivation help to reduce or eliminate the hysteresis, no method exists to control it to desired degrees in a reproducible fashion, due to a lack of understanding of its underlying origin. A majority of experiments are done with the nanotube lying on a Si/SiO\(_2\) substrate, and hence, in an analogy with Si-based FET structures, hysteresis in carbon nanotube FETs was believed to occur as a result of a slow relaxation of mobile charges/ions in the presence of traps residing in the gate architecture under the influence of a gate bias. This relaxation was believed to modify the gate potential, with relaxation times comparable to the experimental time scales.

However, suspended SWCNT devices, independent from the influence of surface/interface charges on the dielectric layer, still show hysteresis behavior, which can be almost completely eliminated by placing the device in vacuum. From this, the dominant mechanism for hysteresis in SWCNT devices has been attributed to a process of trapping/detrapping of mobile charges in a layer of water molecules surrounding the nanotube and the SiO\(_2\) surface, which can be expected to generate enough trapping sites to give rise to the hysteresis. Alternately, it has been recently proposed that the charges responsible for the hysteresis may be injected from the nanotube itself into traps in the surrounding dielectric and the time scale depending on the injection mechanism as well as the capture cross section of traps. It has also been suggested that the trap energies would give rise to an acti-
vated temperature dependence of the hysteresis. However, there are no direct experimental evidences so far, establishing these mechanisms.

In this letter, we present an extensive study of hysteresis in gated, three-terminal s-SWCNT devices. These measurements provide conclusive experimental evidence that a dynamic screening arising out of a charge injection from the nanotubes into the surrounding dielectric indeed causes the hysteresis. From the temperature dependence of hysteresis, \( (20–300 \text{ K}) \), we find that the magnitude of hysteresis does not reflect any activated process of the trap energies. Rather, it depends only on the number of charges available for the nanotube channel conductance.

A number of devices were characterized for hysteresis, and the details of a representative device is here. They show a low room-temperature saturation conductance \( G_{\text{sat}} \) of less then \( 0.01 \text{e}^2/\hbar \), due to a high contact resistance of \( 1–10 \text{ M}\Omega \) [Fig. 1(b)]. \( G_{\text{sat}} \) decreases monotonically with \( T \) [Fig. 2(b)] down to \( T \sim 100 \text{ K} \). Below 100 K, \( G_{\text{sat}} \) gradually saturates, according to the thermal- and tunneling-injection regimes\(^{10}\) in SWCNT FETs.

The nanotube devices were typically 1 \( \mu \text{m} \) long, grown by chemical vapor deposition, and contacted to Ti/Au electrodes fabricated by electron beam lithography, with the 100 nm oxide separated Si substrate as a back gate\(^\text{11}\) [Fig. 1(a)]. Typically no current flows through the device for \( V_G > V_{\text{th}} \) (off-state). The transfer characteristics were measured under a vacuum pressure \(<10^{-6} \text{ Torr} \) by keeping the drain voltage \( V_{\text{DS}} \) at fixed values of \( 10–50 \text{ mV} \) and sweeping the \( V_G \) between \( \pm20 \text{ V} \). For \( V_G < V_{\text{th}} \), the device switches to its on-state and current starts to flow. At large \(-ve \) gate voltages, the current through the device increases until it reaches a saturation value. In most cases, a small drain current was also observed at positive gate voltages because a small number of charge carriers can access the conduction band, either due to a favorable band alignment at the nanotube-contact interface\(^\text{12}\), or due to a doping of the nanotube with \( n \)-type carriers by water molecules\(^\text{13}\). Figure 1(b) shows the transfer characteristics in a typical device at room temperature. Large hysteresis was observed with a hysteresis gap \( \Delta V_H \sim 20–30 \text{ V} \) for \( V_G^{\text{max}}=20 \text{ V} \). \( \Delta V_H \) is the difference in \( V_{\text{th}} \) for forward and reverse sweeps. At 295 \( K \), \( \Delta V_H \) decreases linearly with decreasing \( V_G^{\text{max}} \) [Fig. 1(c)], indicating that the accumulation of charges responsible for the screening is proportional to the \( V_G^{\text{max}} \). The positions of the threshold voltage (as indicated with arrows) for the forward \( (V_{\text{th}}^f) \) and reverse \( (V_{\text{th}}^r) \) sweeps and \( \Delta V_H \) depends on the intrinsic time scale involved in the building up of the net screening. In order to quantify this, the devices were held at \( V_G^{\text{max}} \) for varying times \( \tau \) before performing the sweep. \( V_{\text{th}}^f \) was found to shift towards more negative values for increasing \( \tau \) [Fig. 1(d)], due to an increased amount of initial buildup of charge screening \( V_G \). The screening saturates for larger values of \( \tau \), with very little change for \( \tau > 5 \text{ s} \). Therefore, a hold time of 5 s was used as standard for subsequent measurements. When \( V_G \) is swept from \(-ve \) to \(+ve \) values, \( V_{\text{th}}^r \) shifts towards more negative gate voltages, and when \( V_G \) is swept from \(+ve \) to \(-ve \) values, \( V_{\text{th}}^f \) shifts towards more positive gate voltages.

As the temperature is decreased from 295 K, \( V_{\text{th}}^f \) shifts to higher values of \( V_G \), while \( V_{\text{th}}^r \) shifts to lower values of \( V_G \) [Fig. 2(a)]. \( \Delta V_H \) narrows down and begins to show signs of saturation at the lowest temperatures. The devices show small but significant hysteresis even at 20 K. For a \( \pm20 \text{ V} \) sweep, \( \Delta V_H \) decreases to \( \sim2–5 \text{ V} \) at 20 K. The variation of \( \Delta V_H \) at different \( V_G^{\text{max}} \) [Fig. 1(c)] and \( dV_G/d\tau \) at 20 K shows trends similar to those at room temperature, with proportionately smaller values, indicating a similar mechanism behind this hysteresis at all temperatures. The average of \( V_{\text{th}}^f \) and \( V_{\text{th}}^r \) changes very slowly with temperature and at 20 K, where hysteresis effects are minimum, the average \( V_{\text{th}} \) generally falls in the range of \(-3.0 \text{ to } -5.0 \text{ V} \).

An Arrhenius plot of \( V_{\text{th}}^f \) or \( V_{\text{th}}^r \) (not shown) reveals that over the entire temperature range, there is no single activated process. This is also the case for \( \Delta V_H \) (Fig. 3). This is unexpected if the hysteresis was caused by trapping/detrapping of mobile charge carriers already present in the dielectric. The slope of the Arrhenius plot should be indicative of the activation energy of any traps. The slope decreases as temperature is lowered and even at the steepest part (at high temperature), activation energies of \( 5–10 \text{ meV} \) is derived from the slope, which is an order of magnitude lower than typical diffusion activation energies of common mobile ions\(^\text{14}\), such as \( \text{Na}^+ \) \((\sim120 \text{ meV})\) and \( \text{Li}^+ \) \((\sim100 \text{ meV})\) or the trapping/detrapping energy of electrons\(^\text{15}\) \((120–170 \text{ meV})\) in defect sites of \( \text{SiO}_2 \) dielectric in traditional Si FETs. These are the first clear indications that mobility and trapping of ions

![FIG. 1. (Color online) AFM image of a single SWCNT device contacted by Ti/Au electrodes in its schematic three-terminal FET configuration.](https://example.com/figure1.png)

![FIG. 2. (Color online) Variation of \( V_{\text{th}}^f \), \( V_{\text{th}}^r \), and \( \Delta V_H \) as a function of \( T \) for a SWCNT FET.](https://example.com/figure2.png)
or electrons in the underlying dielectric do not dictate the hysteresis in SWCNT FETs. In addition, any ionic movements in water monolayers or in the oxide substrate should freeze out at low temperatures, thereby removing hysteresis altogether. Therefore, we explore the alternate mechanism, where the charges that cause hysteresis are reversibly injected into the surrounding dielectric from the nanotube itself.

In the case of such charge injection governing hysteresis, the magnitude and variation of the hysteresis gap should be related to the amount of charge being injected from the nanotube into the surrounding dielectric. This in turn is expected to be proportional to the number of carriers present in the nanotube conduction channel. In order to estimate the carrier density \( n \) in the nanotube, we invoke the drift–diffusion model\(^9\) for carrier transport through the s-SWCNT, which gives \( G^\text{on}=ne\mu L \). Here, \( e \) is the electronic charge, and \( \mu \) is the carrier mobility, and the channel charge density \( ne \approx C_G(V_G-V_\text{th})/L \).\(^8\)\(^,\)\(^10\) Therefore, \( n \) is proportional to the ratio \( G^\text{on}/\mu \). \( \mu \) can be estimated from the slope\(^8\) \( (dI_D/dV_G) = \mu V_D/C_G/L^2 \) of the linear part of the transfer characteristics. Figure 2(b) shows the variation of slope with temperature, which follows trends similar to previous reports.\(^7\)

Figure 3 also shows the variation of the ratio \( G^\text{on}/\text{slope} \) with \( T \), which is indicative of the variation of \( n \) with \( T \), along with the variation of \( \Delta V_H \) with \( T \). It is immediately evident that the temperature dependence of the hysteresis gap is strikingly similar to that of the number of carriers over the entire range of temperatures. The ratio of on-state conductance to the hysteresis gap (inset of Fig. 3) shows exceptional insensitivity to temperature over the entire range. This provides conclusive experimental evidence that the screening that leads to hysteresis occurs from charges that are injected into the surrounding dielectric from the nanotube itself, and not from any mobile charges/ions already present in the gate oxide. Although the charge transport mechanism along the nanotube channel changes dramatically between the classical and quantum regimes, the hysteresis depends simply on the carrier charge density of the nanotube over the entire range of temperatures.

In conclusion, we have presented a systematic investigation of the origin of hysteresis in gate-modulated transport in s-SWCNTs. From a temperature dependence of the on-state conductance, carrier mobility and the hysteresis gap, we have established that the hysteresis is caused by charges injected directly from the nanotube into the surrounding dielectric, leading to a dynamic screening of the gate voltage.

This interpretation is built up on the facts that (a) hysteresis exists in nanotube FETs at temperatures as low as 20 K, where the diffusion of mobile ions in the dielectric is unexpected, and (b) the temperature dependence of hysteresis does not reflect any trapping/detrapping mechanism. In contrast, (c) it is solely dependent on the number of charges present in the nanotube over a large range of temperatures, spanning both classical and quantum transport regimes. The secondary dielectric (water monolayers) serves the dual purpose of lowering the threshold for charge injection, as well as providing a medium for capacitive accumulation and distribution of injected charges. The leaky dielectric around the nanotubes can also be any other condensed gas or vapors, or passivation layers such as oxides or polymers. The amount of hysteresis depends on how much the dielectric layer lowers the threshold energy for charge injection, and whether it allows charges to accumulate within itself. Knowledge of these properties would help in controlling or completely eliminating the hysteresis seen in nanotube devices. In a related work, we have shown how the capacitive charging of the surrounding dielectric can be modeled as a charging/discharging of a series RC circuit, which can be used to estimate accurate device properties in the presence of hysteresis using a single “time-decay” experiment.\(^18\)

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**Figure 3.** (Color online) Variation of the ratio \( G^\text{on}/\text{slope} \) (①) and \( \Delta V_H \) (②) with \( T \), plotted as an Arrhenius plot, for a SWCNT FET. The inset shows the ratio \( (G^\text{on}/\text{slope})/\Delta V_H \).