Statistical Modeling of Device Mismatch for Analog MOS Integrated Circuits

Christopher Michael and Mohammed Ismail, *Senior Member, IEEE*

Abstract—**A generalized parameter-level statistical MOS model, called SMOS, capable of generating statistically significant model decks from intra- and inter-die parameters statistics is described. Calculated model decks preserve the inherent correlations between model parameters while accounting for the dependence of parameter variance on device separation distance and device area. Using a Monte Carlo approach to parameter sampling, circuit output means and standard deviations can be simulated. Incorporated in a CAD environment, these modeling algorithms will provide the analog circuit designer with a method to determine the effect of both circuit layout and device sizing on circuit output variance. This will ultimately lead to computer-aided optimization of both circuit and layout design of analog integrated circuits. Test chips have been fabricated from two different fabrication processes to extract statistical information required by the model. Experimental and simulation results for two analog subcircuits are compared to verify the statistical modeling algorithms.**

I. Introduction

ADVANCES in microelectronics fabrication coupled with the desire to create faster, more complex analog CMOS circuits have pushed the feature size of many analog processes to the 1–2-μm range. Because variances in parameters such as channel length, channel width, threshold voltage, and substrate doping do not scale with dimension, device mismatch increases as device feature size is reduced. It is expected that the performance variations caused by this mismatch in short-channel CMOS circuits will be crucial and may, ultimately, introduce a limitation for device scaling in analog circuits.

In order to simulate short-channel analog CMOS circuits with a high degree of reliability, a parameter-level statistical model which accounts for intra-die variances and correlations in model parameters is needed. Second moment simulation based on a model of this type will be useful in determining the sensitivity to scaling of existing circuits as well as predicting performance variations in new designs. Likewise, fabrication processes can be compared according to performance and reliability by simulating the same circuit using statistical data from different processes. With this tool, an analog circuit designer can estimate the yield of a circuit based on a performance specification without fabrication of the device.

Despite its importance to circuit operation, relatively few papers have been presented on the subject of MOS transistor mismatch. Shyu *et al.* [1] examined the dependence of the standard deviation of current sources on device size. Lakshmikumar *et al.* [2] advanced this work by separating the area dependence of transistor mismatch into two separate components: the standard deviations of the current factor and the threshold voltage. Pelgrom *et al.* [3] further parameterized mismatch by including a term for the standard deviation of the substrate factor. Additionally, the effect of device spacing on transistor matching was investigated. While these studies successfully determined the primary causes of device mismatch, the resultant equations for drain current mismatch are not compatible with present circuit simulators.

Previous publications in the area of statistical modeling and simulation [4]–[10] have focused on methods to solve the problem of correlated parameters. Some investigations [4]–[6] attempted to describe the total device variance in terms of a few independent physically meaningful parameters. While this approach is sufficient for large-geometry devices, the inclusion of second-order effects is necessary in the statistical modeling of short-channel devices, especially in analog circuits where model accuracy is crucial. Other investigations [8]–[10] have used principal component analysis, a more standardized statistical technique to account for parameter correlation. Using this technique, these studies have accomplished the goal of producing a CAD-compatible algorithm to calculate correlated model parameters, including second-order effects. However, these studies depend on either die-level statistics or a combination of die-level and matched statistics [8], [11] to calculate model decks. In either case, the dependence of parameter standard deviations on device area and circuit layout is not included in the parameter calculations. The resultant simulations are generally overly pessimistic, with no information concerning the effect of device area and spacing on the circuit output variances.

This paper will present a unified method to accurately calculate statistically relevant device model decks. Section II presents both the statistical model and the algorithms used to calculate model decks. A comparison of experimental data to simulations performed using the new

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C. Michael was with the Department of Electrical Engineering, Ohio State University, Columbus, OH 43210. He is now with National Semiconductor Corporation, Santa Clara, CA 95052.

M. Ismail is with the Solid-State Microelectronics Laboratory, Department of Electrical Engineering, Ohio State University, Columbus, OH 43210.

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statistical model will be provided in Section III. In Section IV, potential and applications of the statistical model will be explored.

II. Statistical MOS Model

Two major obstacles to achieving second moment simulation are the correlation between model parameters inherent in device models and the variance of these model parameters across the die. Neglecting width and length sensitivity terms, the standard SPICE short-channel model BSIM [12], [13] contains 17 primary electrical parameters, most of which are correlated. In addition, the variance of each parameter across the die must also be considered. These parameter variances will, in general, be dependent on both transistor size and the distance between transistors. Therefore, in an analog circuit containing ten transistors, there will be 170 nonindependent parameters that need to be calculated in such a way as to preserve the correlations and variances inherent to that process.

A. Parameter Variance Model

MOS transistor mismatch can be defined as the variation in drain current for identically designed devices under similar bias conditions. Mismatch is caused by variations in processing steps such as ion implantation, oxide growth, and lithography. A basic assumption in this paper is that these processing variations are independent and normally distributed. As a result, the approximation of normally distributed model parameters is reasonable and will be used throughout this paper.

The first step in the development of a statistical model which comprehends device sizes and spacings is to determine the form for the variance of a single model parameter. The dependence of parameter variance on device area WL and separation distance D must be accounted for in this basic model. In addition, this model must be compatible with the algorithms, described in the following three subsections, used to preserve parameter P by the relation found by Pelgrom *et al.* [3]:

$$\sigma^2(P) = \frac{a_P}{WL} + s_P^2 D^2 \tag{1}$$

where a_P and s_p are process-dependent constants relating the parameter variance to the device area and separation distance, respectively.

The device area term in the parameter variance model was derived by Pelgrom *et al.* assuming a random white-noise mismatch-causing source. The separation distance term emanates from fabrication variations such as the deviation of polysilicon linewidth across a wafer [14], [15]. These variations tend to occur in a radial pattern across the wafer. Therefore, the effect of fabrication variations on the matching of a transistor pair will be dependent on the orientation of the pair relative to the wafer center. Since the two terms in the parameter variance model are independent and are assumed to be normally distributed, they can be accounted for separately when computing transistor models.

To verify the form of the parameter variance model, a test chip was fabricated using a MOSIS 2-μm n-well process. This chip contains n-channel test transistors with three device sizes ($W/\mathrm{L} = 3/2, 20/2, 20/4$ $\mu\mathrm{m}/\mu\mathrm{m}$) at three separation distances ($D = 50, 100, 150$ μm). Separation of the area and distance dependencies of the parameter variance model was performed by measuring the difference in parameter values for devices separated by varying distances. Each transistor pair is oriented in the same direction on the chip, and the mismatch between transistor parameters is always referenced to the same side of the chip. Therefore, process variations characterized by radial patterns should have the same effect on each transistor pair.

Results of these measurements for the flat-band voltage are shown in Fig. 1. The large devices were chosen for Fig. 1, since the relative effect of the separation distance term of the parameter variance model is larger than for small-area devices. The variation about the mean parameter difference is due to a white-noise mismatch process described by the device area dependence in the parameter variance model. Ideally, this standard deviation would be constant, independent of separation distance. In Fig. 1, the parameter-mismatch standard deviations are not equal due to the small number of measurements. The drift in the mean value of parameter difference as the devices are separated by longer distances is due to fabrication variations described by the separation distance dependence of the parameter variance model. This measurement technique, which will be described in more detail in Section III, constitutes a new method to separate the two dependencies in the parameter variance model. Assuming a perfectly radial mismatch causing source, the mean value of the parameter difference will be changed as the transistor pair is rotated, resulting in a uniformly distributed mismatch component. However, in this research, we have assumed that this rotation will result in a normally distributed mismatch term. Since there is no prior knowledge of the orientation of the transistor pairs on the test chip relative to the wafer center, the measured drift in mean parameter difference values was assigned to be the separation distance term in the parameter variance model.

To illustrate the area dependence of the parameter variance, the standard deviation of the flat-band voltage (*VFB*) and the saturation region mobility (*MUS*) are plotted against $1/\sqrt{WL}$ in Fig. 2. In these plots, only the area dependence of the parameter variance is considered. Both plots exhibit the linear dependencies indicated by the parameter variance model. Each of the 16 BSIM parameters extracted from the test transistors showed good fit to the area-dependent term of the parameter variance model.

The relative effect of device separation distance on the parameter standard deviation can be seen in Fig. 3. For small-area devices, the separation distance has little effect on the parameter variance. Thus, in analog circuits containing small-area transistors, an increase in transistor size

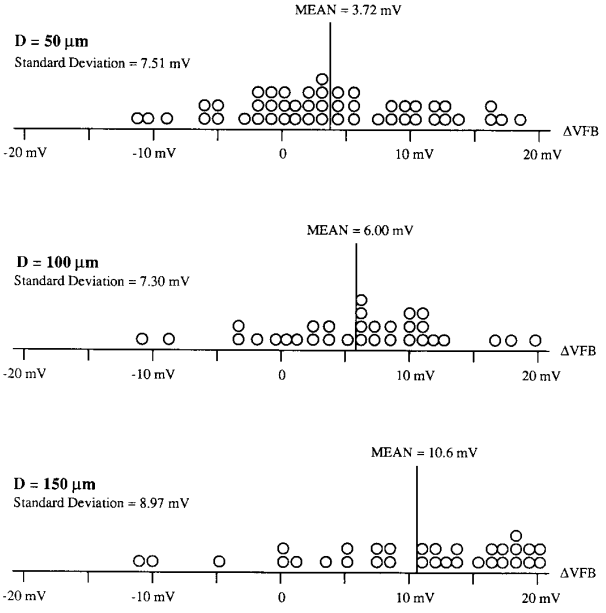

Fig. 1. Mismatch in flat-band voltage in $W/L = 20/4\text{-}\mu m/\mu m$ devices at three different device separation distances.

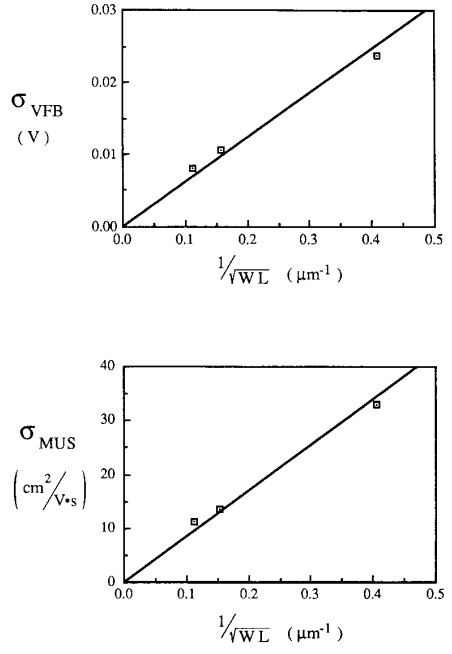

Fig. 2. Area dependence of the mismatch standard deviation of two BSIM model parameters: the flat-band voltage (*VFB*) and the saturation region mobility (*MUS*).

is necessary in order to significantly improve transistor matching. However, for large-area transistors, matching can be substantially improved by placing the transistors in close proximity.

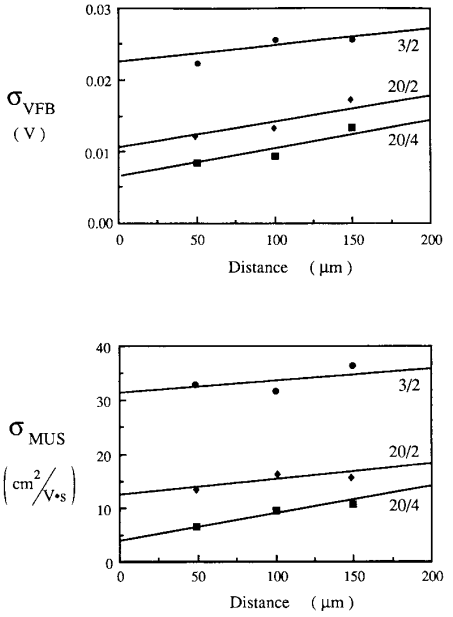

Fig. 3. Device separation distance dependence of the mismatch standard deviation of two BSIM model parameters: the flat-band voltage (*VFB*) and the saturation region mobility (*MUS*).

B. σ-Space Analysis

Calculation of parameters which preserve variances dependent on device separation distances is a new approach to statistical modeling. Previous modeling approaches lumped parameter variances into various categories, such as matched, wafer level, or wafer to wafer. This approach may be valid for circuits when a high degree of accuracy is unnecessary; however, in analog circuits, small inaccuracies such as these can cause fairly large errors in simulation results.

In a multiple-transistor circuit, preservation of spacing-dependent standard deviations of every transistor can be achieved through σ-space analysis (σSA) [16]. In this analysis technique, the spacing-dependent portion of the device mismatch is modeled by a series of linear equations. Neglecting the parameter mean and area-dependent variance, the following set of linear equations must be solved:

$$\begin{aligned} P_1 &= 0 \\ P_2 &= A_{22}R_2 \\ P_3 &= A_{32}R_2 + A_{33}R_3 \\ &\vdots \\ P_M &= \sum_{I=2}^{M} A_{MI}R_I \end{aligned} \tag{2}$$

where P_M is the general model parameter P in transistor M, R_I are independent unit normal random numbers, and A_{MN} are the random number coefficients which must be

computed. Each parameter will have a unique set of random number coefficients based on its statistics.

The effect of each random number coefficient for a given model parameter can be explained in terms of an N-dimensional σ space. This space is considered a σ space since the distance between any two points in this space represents a standard deviation. In this regard, this space representation is analogous to euclidean uncertainty space [17], in which covariances can be represented by norms of vectors in a linear space. Transistors are placed at points in this space in such a manner as to preserve spacing-dependent variances between each transistor pair in the circuit.

An example of a σ space for a given parameter P in a three-transistor circuit is shown in Fig. 4. The unit vectors corresponding to the coordinates in a σ space are a series of independent random numbers with $\mu = 0$ and $\sigma = 1$. The random numbers R_I in (2) meet these criteria and, therefore, are used as the unit vectors in σ space in Fig. 4.

Parameters are placed in the σ space according to the values of σ_{MN}, the standard deviation between P_M and P_N, where the subscript of P denotes the transistor number. At this point, device size is not considered; therefore, σ_{MN} can be represented by

$$\sigma_{MN} = s_P D_{MN} \tag{3}$$

where s_P is a process-dependent fitting constant. Transistor 1 is the reference transistor; therefore, P_1 is placed at the origin. P_2 is placed a distance $|\sigma_{12}|$ from the origin on the R_2 axis. P_3 is located at the intersection of two arcs: an arc drawn from P_1 with a radius of $|\sigma_{13}|$, and an arc drawn from P_2 with a radius of $|\sigma_{23}|$.

Random number coefficients correspond to the axis coordinates in this space. A_{22}, the coefficient along the R_2 axis for parameter P_2, is equal to σ_{12}. Likewise, A_{32} and A_{33} are the R_2 and R_3 coordinate values for parameter P_3, respectively. Expressions for A_{32} and A_{33} are given by

$$A_{32} = \frac{A_{22}^2 + \sigma_{13}^2 - \sigma_{23}^2}{2A_{22}}$$

$$A_{33} = \sqrt{\sigma_{13}^2 - A_{32}^2}. \tag{4}$$

After further derivation, a closed form for the random number coefficients A_{MN} can be determined and is given by

$$M > N: \quad A_{MN} = \frac{\left[\sum_{i=2}^{N} A_{Ni}^2\right] + \sigma_{1M}^2 - \sigma_{NM}^2 - 2\left[\sum_{j=2}^{N-1} A_{Mj}A_{Nj}\right]}{2A_{NN}}$$

$$M = N: \quad A_{MM} = \sqrt{\sigma_{1M}^2 - \left[\sum_{i=2}^{M-1} A_{Mi}^2\right]}. \tag{5}$$

An important feature of σSA and the resultant determination of the random number coefficients A_{MN} is that the techniques presented in this section are statistical in nature and, therefore, are model independent. In this paper, σSA will be used to preserve the spacing dependence of the standard deviation of BSIM SPICE parameters; however, this analysis technique is equally valid for any parameterized device model. A second method to preserve the spacing dependence of the parameter mismatch, based on the coordinates of the transistors relative to an arbitrary origin, has also been developed [18], [19].

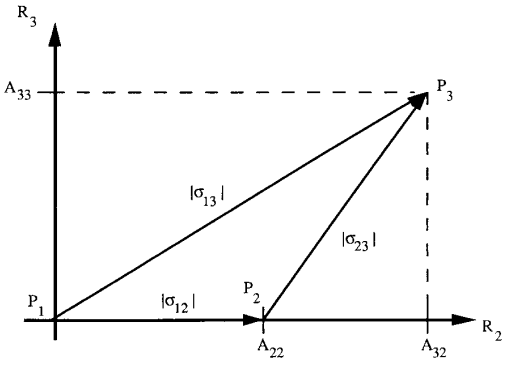

Fig. 4. σ-space representation for parameter P in a three-transistor circuit.

C. Principal Component Analysis

Using σSA, the spacing dependence of each model parameter can be preserved. This is sufficient to calculate one parameter for a multiple-transistor circuit. However, in a multiple-parameter device model, the correlations between model parameters must also be preserved during the calculation of model decks. In order to preserve these parameter correlations, the relationships between parameters, or the dependence structure, must be examined. As mentioned in the introduction, one method to account for this dependence structure is based on the determination of a reduced set of independent critical parameters. However, due to the model accuracy needed to simulate analog circuits, especially for circuits employing small devices, algorithms based on the assumption of a reduced number of model parameters will not yield accurate results. The method employed in this study to account for parameter correlations during the calculation of model decks is called the principal component analysis (PCA) [20]–[22]. In PCA, a transformation of the parameter correlation matrix yields a series of linear equations relating the normalized model parameters to independent unit normal random variables. While the dependencies between model parameters may not be linear, a linear approximation is valid

	VFB	K1	K2	ETA	MUZ	U0	U1	X2MZ	X2E	X3E	X2U0	X2U1	MUS	X2MS	X3MS	X3U1
VFB	1															
K1	-0.9011	1														
K2	-0.5842	0.8837	1													
ETA	0.6711	-0.5869	-0.3320	1												
MUZ	0.2467	-0.0884	0.1693	0.3231	1											
U0	0.1067	0.0818	0.2384	0.3741	0.0820	1										
U1	-0.0947	0.0616	0.0144	-0.5006	0.2662	-0.7585	1									
X2MZ	0.3439	0.0349	0.4308	0.2981	0.5489	0.2738	0.0341	1								
X2E	-0.6952	0.6302	0.5064	-0.5707	0.0564	-0.0387	0.1997	-0.0682	1							
X3E	-0.4724	0.4775	0.2534	-0.7929	-0.2066	-0.2299	0.4158	-0.2819	0.3888	1						
X2U0	0.5420	-0.1535	0.2446	0.5016	0.3753	0.3774	-0.1931	0.8829	-0.4423	-0.4071	1					
X2U1	-0.6622	0.5532	0.3977	-0.5608	-0.0896	-0.0028	0.1151	-0.1326	0.9381	0.3619	-0.4918	1				
MUS	-0.1043	0.1943	0.2657	-0.3937	0.6175	-0.3548	0.8254	0.3074	0.3395	0.3799	0.0100	0.2170	1			
X2MS	-0.1972	0.4388	0.6506	-0.2029	0.3847	0.1716	0.1744	0.7059	0.6161	0.0701	0.3675	0.5758	0.4540	1		
X3MS	-0.2520	0.2637	0.2201	-0.6225	0.2768	-0.4774	0.8827	0.0919	0.3890	0.5151	-0.1911	0.3160	0.9049	0.3568	1	
X3U1	-0.1921	0.1822	0.1022	-0.6432	0.1095	-0.6492	0.9377	0.0022	0.2718	0.5482	-0.2246	0.2109	0.8101	0.2187	0.9417	1

Fig. 5. Correlation matrix of BSIM SPICE model parameters for n-channel MOS transistors. Matrix is symmetrical.

due to the small range over which parameter values vary (analogous to a small-signal approximation in analog circuit analysis). PCA is applicable to the simulation of analog circuits, since no statistical information is lost due to parameter reduction assumptions. Additionally, PCA is a generalized statistical technique and is, therefore, valid for any model structure.

For the 2-μm n-well test chip, BSIM SPICE parameters were extracted from four chips, each containing 192 n-channel MOSFET's. Before finding parameter correlations, the extracted parameters were normalized. Normalization, necessary due to units considerations, is achieved as follows:

$$P' = \frac{P - \mu_P}{\sigma_P} \tag{6}$$

where μ_P and σ_P are the population mean and standard deviation of parameter P, respectively, and P' is the resultant normalized value for P. After normalization, parameter correlations can be determined from

$$\rho_{PQ} = \frac{1}{\mathrm{N}} \sum_{i=1}^{N} P' Q_i' \tag{7}$$

where ρ_{PQ} is the correlation between parameters P and Q. The correlation matrix for the n-channel BSIM model as calculated from n-well test chip is presented in Fig. 5.

Principal components can be related to the normalized parameters by determining the eigenvalues and eigenvectors of the correlation matrix and using the following equation:

$$\boldsymbol{C} = \boldsymbol{\Lambda}^{-1/2} \boldsymbol{U}^{-1} \boldsymbol{P}' \tag{8}$$

where $\boldsymbol{C}$ is the principal component vector, $\boldsymbol{\Lambda}$ is the diagonal matrix containing the eigenvalues of the parameter correlation matrix, $\boldsymbol{U}$ is the corresponding eigenvector matrix, and $\boldsymbol{P}'$ is the normalized parameter vector. Each principal component C_i is an independent normal random variable with zero mean and unit variance.

An added benefit of PCA is its ability to account for the variance of a device with many parameters by relatively few principal components. During PCA, the first principal axis, characterized by C_1, is rotated in the normalized parameter space to align with the largest variance. Further axis rotations are performed in a similar manner. Thus, the first few components will account for the majority of the total device variance. For the correlation matrix shown in Fig. 5, the first six principal components, accounting for 96% of the total device variance, were retained.

Values for the normalized parameters can be calculated from the inverse of (8):

$$\boldsymbol{P}' = \boldsymbol{U} \boldsymbol{\Lambda}^{1/2} \boldsymbol{C} \tag{9}$$

where the values for $\boldsymbol{U}$ and $\boldsymbol{\Lambda}$ have been previously determined. An example of the linear principal component equations is given in (10) for three important BSIM model parameters: the flat-band voltage (*VFB*), the linear region mobility (*MUZ*), and the saturation region mobility (*MUS*):

$$\begin{aligned} VFB' &= 0.6977C_1 + 0.4067C_2 - 0.4594C_3 \\ &\quad + 0.0891C_4 - 0.2610C_5 + 0.1880C_6 \\ MUZ' &= -0.0527C_1 + 0.7673C_2 - 0.0904C_3 \\ &\quad + 0.3323C_4 + 0.4880C_5 + 0.1246C_6 \\ MUS' &= 0.6923C_1 + 0.5491C_2 - 0.3715C_3 \\ &\quad + 0.0937C_4 + 0.1828C_5 + 0.1525C_6. \end{aligned} \tag{10}$$

Values for C_I can be randomly and independently generated from a unit normal distribution ($\mu = 0$, $\sigma = 1$). Thus, for each transistor, six random variables are needed to calculate the 17 normalized parameters in the BSIM model. Through this method, values for the normalized parameters can be calculated quickly and easily. Repeated generation of the $\boldsymbol{C}$ vector constitutes a Monte Carlo approach to sampling the multidimensional parameter space. If only a simple global variance is considered, these values can be denormalized by inverting (6). The resultant parameter values can be entered into a simulator to determine one output point. Repetition of this procedure will produce a variance for each circuit output. In this paper, denormalization is more complicated, as the parameter variances are dependent on both the device area and the separation distances between devices. However, the sampled normalized parameters will be invaluable in the calculation of model decks, since they are normally distributed random variables which preserve the correlations between model parameters.

D. Model Integration

A combination of the models and algorithms examined in this section is necessary in order to calculate statistically relevant model decks. Through σSA, the device spacing dependence of the parameter standard deviation model is preserved. However, to fully realize the parameter variance model given by (1), a device area dependence must be included in the final model for parameter standard deviation. Likewise, the results of PCA must be integrated into this model in order to preserve the parameter correlations inherent to the model. To calculate complete model decks, a model for the parameter means must also be included. An additional factor, the inter-die parameter variance, should be inserted into the model to account for wafer-level or wafer-to-wafer parameter variance. While this component will not contribute to device mismatch, it will have an effect on circuit performance.

As previously noted, the result of entering random numbers for C_N in the PCA-generated linear equations, shown in (10), is a group of unit normal numbers that preserve the correlation between model parameters. If these normalized numbers are used in place of the unit normal random numbers in the σSA, the result is a statistical model that preserves both the parameter correlations and the spacing dependency of the parameter variance. For example, the value for VFB' in (10) can be used as R_2 in the σ_{VFB} equations similar to (2). Similarly, the value for MUZ' in (10) can replace R_2 in the σ_{MUZ} equation. Thus, the generation of six unit normal random numbers, $C_1 \cdots C_6$, is capable of computing one model deck for one transistor. Each successive model deck is calculated by generating a new C_I vector and calculating a new set of normalized parameters.

Statistical MOS (SMOS), a statistical model for a general parameter P of transistor M in an N-transistor circuit, is given by

$$P_M = \mu(P_M) + \sqrt{\frac{a_P}{2W_M L_M}}\, R_P(M) + \sum_{I=2}^{M} A_{MI} R_P(N + I) \tag{11}$$

where $\mu(P_M)$ is the mean parameter value and R_P are the correlated unit normal random numbers generated through PCA. While the statistical parameter model of (11) does not preserve parameter correlations exactly, the error introduced by incorporating PCA into the statistical model is negligible. For a typical circuit layout, calculated parameter correlations deviate from their desired values by less than 1%.

The model for the parameter means is based on the inverse geometry dependence [12], [23] of SPICE parameters. This model is generated by a least-squares fit to the $1/L$ and $1/W$ factors. The resultant equation for the mean parameter values is provided by

$$\mu(P_M) = \mu_{0P} + \frac{\mu_{LP}}{L_M} + \frac{\mu_{WP}}{W_M} + \sigma_{\text{inter}} R_P(N + 1) \tag{12}$$

where L_M and W_M are, respectively, the length and width of transistor M, and μ_{0P}, μ_{LP}, and μ_{WP} are fitting constants. The σ_{inter} term represents the inter-die parameter variances, which can be modeled as a deviation in parameter mean for each transistor in a circuit. In subsequent circuit simulations, the inter-die parameter variance terms are neglected. A complete set of fitting constants for the n-well test chip is provided in Table I.

III. Experimental and Simulation

This section contains a comparison between simulated circuit variance using the statistical model described in Section II and experimental circuit variance determined from two test chips. Since a large number of any given circuit is necessary to confidently determine an actual variance, and since a limited amount of chip area is available, two-transistor subcircuits are employed to test the algorithms.

A. Test Chip Description

To test the statistical model presented in this paper, two chip designs were fabricated from two different processes. A total of four chips from each design were obtained. Each of these chips contains sufficient test transistors to determine both the parameter correlations and spacing-dependent parameter variances needed to characterize the statistical model. In addition, each chip design includes numerous repetitions of a simple subcircuit whose actual output variance can be compared to a simulated variance.

Chip 1, fabricated using a MOSIS 2-μm p-well process, contains a total of 192 test transistors and 96 two-transistor grounded resistor circuits. The goal of this first chip is to test the algorithm which models the separation distance dependence of the parameter standard deviation. As such, only two device sizes, $W/L = 20/2$ and $20/4$ μm/μm, were fabricated. To test the distance depen-

TABLE I
COMPLETE SET OF MODEL FITTING CONSTANTS FOR 2-μm N-WELL PROCESS. UNITS COLUMN REFERS TO THE μ_0 TERMS. OTHER FITTING CONSTANTS HAVE UNITS AS DESCRIBED IN THE FINAL ROW.

	μ_0	μ_L	μ_W	$\sqrt{a_p}$	s_P	Units
VFB	−0.7923	0.1596	−0.2149	0.0623	7.33E-5	V
*K*1	1.0631	−0.3540	0.6939	0.0714	4.53E-5	$V^{0.5}$
*K*2	0.1297	0.1116	0.0565	0.0178	7.00E-6	none
ETA	−0.0290	0.0993	−0.0321	5.41E-3	4.38E-6	none
MUZ	611.9	437.9	−107.5	27.9	0.0399	$cm^2/V \cdot s$
*U*0	0.0478	0.0764	−0.0632	6.25E-3	5.13E-6	V^{-1}
*U*1	0.2972	0.7812	−0.0720	0.0714	4.67E-5	$\mu m/V$
X2MZ	−3.063	−1.052	104.5	4.545	1.93E-3	$cm^2/V^2 \cdot s$
X2E	−5.04E-3	0.0269	−0.0172	8.89E-4	6.67E-7	V^{-1}
X3E	3.93E-3	−5.43E-3	2.54E-4	1.09E-3	4.30E-7	V^{-1}
*X2U*0	5.06E-4	−6.93E-3	0.0395	1.78E-3	1.07E-6	V^{-2}
*X2U*1	−0.1009	0.2365	−0.1449	0.0267	6.20E-6	$\mu m/V^2$
MUS	763.5	1160	−145.8	87.0	0.0645	$cm^2/V \cdot s$
X2MS	−64.43	159.5	61.69	14.1	9.33E-4	$cm^2/V^2 \cdot s$
X3MS	30.30	239.8	−26.61	19.5	0.0131	$cm^2/V^2 \cdot s$
*X3U*1	0.1502	0	−3.38E-3	0.0194	1.47E-5	$\mu m/V^2$
T_{OX}	0.0400	0	0	0	0	μm
PHI	0.7500	0	0	0	0	V
V_{DD}	5	0	0	0	0	V
	unit	unit · μm	unit · μm	unit · μm	unit/μm	

dence of the algorithm, $M1$ and $M2$ in the grounded resistor circuit [24], shown in Fig. 6, were separated by three different distances: 50, 100, and 150 μm. To save chip area, the $M1$ transistors in the resistor circuits are also used as test transistors to determine parameter correlations and variances.

From the input node in Fig. 6, the two transistor circuit fabricated on chip 1 acts as a grounded resistor with an equivalent resistance given by

$$R = \frac{V_{IN}}{I_{IN}} = \frac{1}{\mu C_{OX} \frac{W}{L} (V_C - V_{TH})}. \quad (13)$$

The resistor circuit assumes identically sized MOSFET's operating in the saturation region with a control voltage of V_C. To achieve a linear resistance, this circuit depends on perfectly matched devices to cancel the nonlinearities inherent to the MOSFET. Thus, this circuit is a good candidate to determine the effect of device mismatch on circuit variance.

Chip 2, fabricated using a MOSIS 2-μm n-well process, also contains 192 test transistors and 96 two-transistor subcircuits. However, the subcircuit in this case is a simple current mirror shown in Fig. 7. The contents and layout of one transistor group on the second test chip are shown in Figs. 8 and 9, respectively. A total of 16 transistor groups are contained on the chip. As shown in Fig. 8, three device sizes, W/L = 3/2, 20/2, and 20/4 $\mu m/\mu m$, were included in this chip. Unlike the first test chip, the goal of chip 2 was to test the entire statistical model, including the area dependence of the parameter variance. Similar to the grounded resistors included in chip 1, $M1$ and $M2$ of the current mirrors were separated by three distances: 50, 100, and 150 μm as shown in Fig.

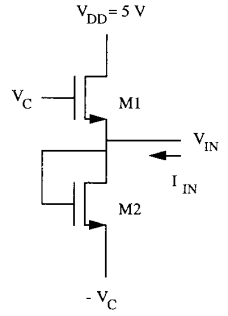

Fig. 6. Test circuit 1: two-transistor voltage-controlled all-MOS grounded resistor.

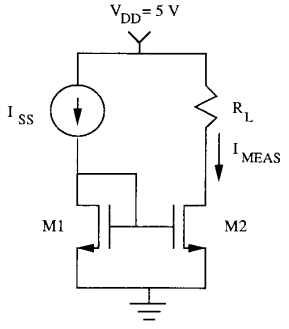

Fig. 7. Test circuit 2: current mirror.

9. BSIM SPICE models were extracted from both of the current mirror transistors to determine the needed statistical data to characterize the statistical model. The off-chip load resistor was chosen to force the reference and mirrored currents to be equal. The same load resistor was then used for each measurement.

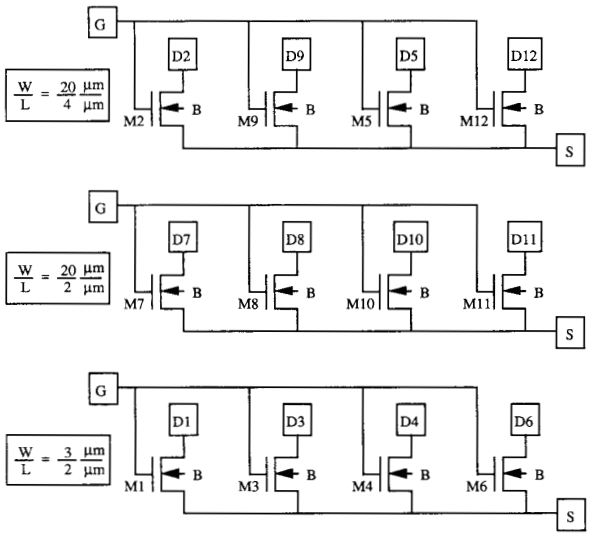

Fig. 8. Contents of one transistor group on the second test chip.

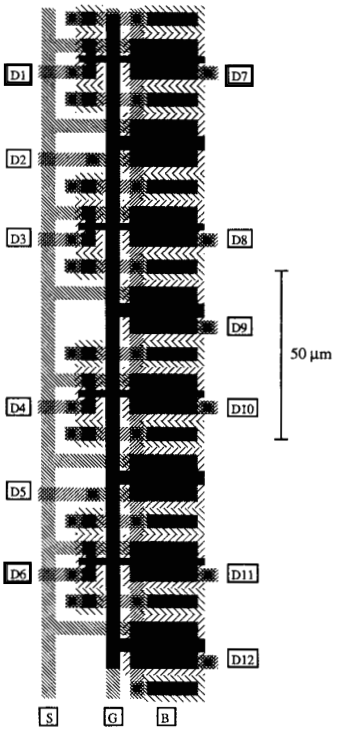

Fig. 9. Layout of one transistor group on the second test chip.

The test structure consists of a column of test transistors, as shown in Figs. 9 and 10, for each device size examined. For each device size on the test chip, a total of 16 of these test columns are present, with each column oriented in the same direction. When calculating the mismatch of a given model parameter, a reference direction for the parameter difference is maintained. As an example, for a given transistor pair in Fig. 10, the parameter mismatch is always calculated by subtracting the parameter value for the transistor which is physically lower in the figure from the parameter value for the physically higher transistor. Thus, the process variations characterized by wafer-level gradients should affect each transistor pair separated by a certain distance in a similar fashion.

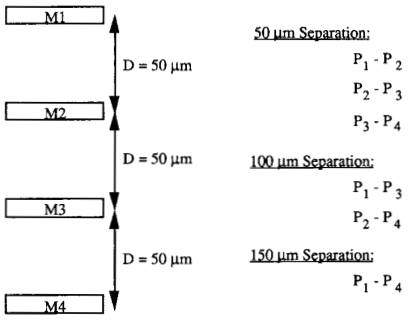

Fig. 10. Four-transistor column with available mismatch data.

The advantage of maintaining a consistent direction of device separation during mismatch calculations is that the statistical model fitting constants can be determined independently. The disadvantage of this scheme is that the parameter mismatch is measured in only one direction. Therefore, transistor columns similar to that shown in Fig. 10 should be oriented in at least two directions. However, s_P can be approximated from these test chips by assuming that the measured parameter mismatch ΔP is equal to the standard deviation of ΔP, $\sigma(\Delta P)$. Hence

$$\Delta P = s_P D \tag{14}$$

where D is the separation distance between the transistor pair.

B. Parameter Extraction

A BSIM parameter extractor, based on Berkeley's extractor [25], was written specifically for this project. The extractor operates on an IBM PC or compatible computer and controls an HP4145B parameter analyzer. For this research, the primary issue for the BSIM parameter extractor is the repeatability of the extractions. That is, if model parameters are repeatedly extracted from the same device, the parameters values should be consistent. To determine the repeatability of the parameter extractor, 16 BSIM parameters were extracted 25 times from the same device. Results of this experiment are presented in Table II, where the parameter sensitivity is defined as the standard deviation of the extracted parameters. The repeatability of parameter extraction is slightly dependent on the device size; however, the parameter sensitivities for the device sizes investigated in this research were on the same order of magnitude. Most importantly, as long as the measured parameter-mismatch standard deviations are significantly larger than the parameter sensitivities listed in Table II, the values determined for the statistical fitting constants are trustworthy.

TABLE II
REPEATABILITY OF EXTRACTED PARAMETERS FOR A $W/L = 20/2\text{-}\mu m/\mu m$ DEVICE

Parameter	Parameter Sensitivity	Units
VFB	0.82E-3	V
K1	0.73E-3	$V^{0.5}$
K2	0.19E-3	none
ETA	0.16E-3	none
MUZ	1.1	$cm^2/V \cdot s$
U0	0.071E-3	V^{-1}
U1	1.0E-3	$\mu m/V$
X2MZ	0.068	$cm^2/V^2 \cdot s$
X2E	0	V^{-1}
X3E	0.078E-3	V^{-1}
X2U0	0.049E-3	V^{-2}
X2U1	0.31E-3	$\mu m/V^2$
MUS	1.2	$cm^2/V \cdot s$
X2MS	0.30	$cm^2/V^2 \cdot s$
X3MS	0.625	$cm^2/V^2 \cdot s$
X3U1	0.68E-3	$\mu m/V^2$

C. Simulation

A flowchart of the simulation procedure, including experimental and computational requirements for the actual model deck calculations, is presented in Fig. 11. The "Statistical Parameter Analysis" block constitutes the process characterization work which is necessary to determine the fitting constants in the statistical parameter models. This work must be performed only once for a given fabrication process. From the parameter correlation matrix, PCA will produce a series of linear equations relating the normalized parameters to a small number of independent random numbers. These linear equations must also be calculated only once for a given process. Given a circuit description that includes device sizes and spacings, the random number coefficients A_{MN} can be calculated from (5). If a circuit layout has not been completed, a nominal value can be entered for each separation distance. Calculation of the random number coefficients must be performed only once for each circuit layout. Therefore, after the first model deck is calculated, only a few random numbers must be generated to calculate each successive model deck.

D. Results

To test the modeling algorithms described in Section II, SPICE model decks were calculated for both the resistor and the current mirror circuits for different device sizes and spacing using the statistical model. A total of 50 simulations were performed on each circuit at each condition.

A comparison between simulated and actual means and standard deviations for the grounded resistor circuit with device sizes of 20/2 and 20/4 $\mu m/\mu m$ is provided in Table III. The simulated and actual mean resistances at each control voltage show excellent agreement. This agreement is expected since the statistical data base from which the simulation is derived is based, in part, on parameter extractions of the transistors in the actual resistor circuits. The agreement between simulated and actual

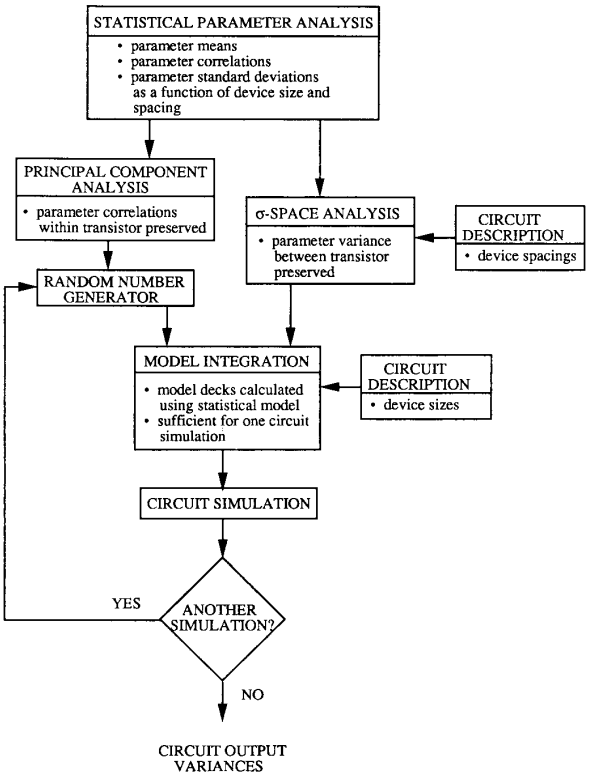

Fig. 11. Simulation flowchart.

mean resistances is, therefore, an indication that the BSIM parameter extraction program is accurate. In general, the simulated and actual mean resistances will not be equal due to inter-die process variations. However, inclusion of the inter-die parameter variance term in (12) should account for these variations. The trend of increasing circuit output standard deviation as separation distance between devices is increased is clearly shown in both the simulation and experimental data. Simulation results using the die-level parameter standard deviations, the standard deviation of a parameter over an entire die, are presented to compare the new statistical model with previous models. Simulations using die-level standard deviations tend to be overly pessimistic for small circuits and yield no information concerning the effect of circuit layout on output variance.

Similar to the density histogram of flat-band voltage mismatch presented in Fig. 1, the distribution of current mismatch for the current mirrors of the second test chip is plotted in Fig. 12. Once again, the reference MOSFET in the mirror is always kept toward one side of the wafer. Through this measurement technique, the two mismatch causing effects can be separated. The variation about the mean current difference is due to the random area dependence of the statistical parameter model. The nonzero mean current difference is caused by the nonrandom separation distance dependence of the parameter

TABLE III
MEASURED AND SIMULATED VALUES FOR RESISTANCE MEAN AND STANDARD DEVIATION AT THREE DIFFERENT CONTROL VOLTAGES FOR W/L = 20/2- AND 20/4-μm/μm DEVICES. ALL RESISTANCE VALUES ARE IN OHMS.

		W/L = 20/2 μ/μm		W/L = 20/4 μm/μm	
Statistic	Bias	Measured	Simulated	Measured	Simulated
Mean	V_C = 2 V	905	910	2137	2141
	V_C = 3 V	726	720	1398	1405
	V_C = 4 V	688	692	1200	1207
D = 50-μm Standard Deviation	V_C = 2 V	8.8	9.0	8.5	7.5
	V_C = 3 V	7.6	8.0	6.4	5.5
	V_C = 4 V	6.2	6.6	5.5	4.5
D = 100-μm Standard Deviation	V_C = 2 V	11.6	12.3	10.2	9.8
	V_C = 3 V	8.7	9.9	8.0	6.9
	V_C = 4 V	7.4	7.6	6.2	5.4
D = 150-μm Standard Deviation	V_C = 2 V	12.4	12.7	10.9	10.5
	V_C = 3 V	10.8	10.4	9.6	8.8
	V_C = 4 V	8.5	7.8	7.9	6.8
Die-Level Standard Deviation	V_C = 2 V	16.3	16.9	15.4	15.0
	V_C = 3 V	10.4	11.1	11.3	9.9
	V_C = 4 V	8.7	9.0	8.0	7.1

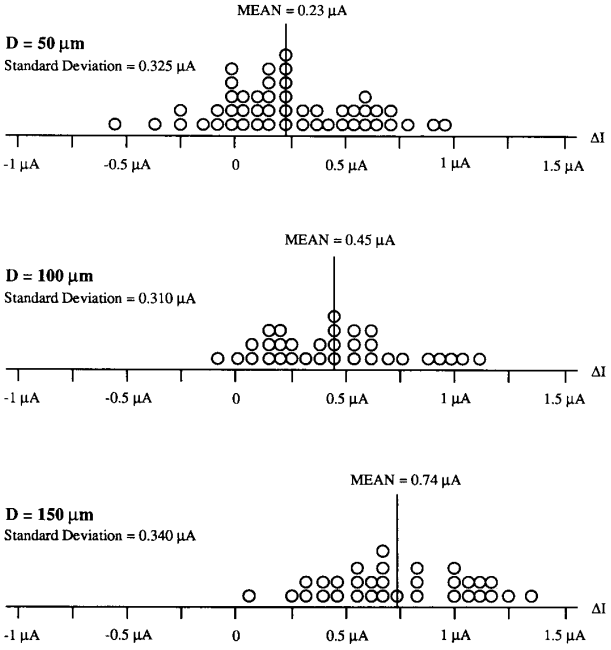

Fig. 12. Mismatch in mirrored current for W/L = 20/4-μm/μm devices at three different device separation distances. Reference current is 50 μA.

variance model. Table IV includes simulated and experimental standard deviations for the current mirrors fabricated on chip 2. As shown in this table, the SMOS model is capable of preserving the device area, circuit layout, and bias dependencies of transistor mismatch when incorporated in a circuit simulator.

The measured and simulated values for the standard deviation of mirrored current show good agreement. As expected, the relative effect of the separation distance between devices on the standard deviation increases as devices size increases. The dependence of device area on the standard deviation is also evident, although the difference in bias conditions due to the different W/L ratios distorts the $1/\sqrt{WL}$ dependence.

Statistical simulation results, shown in Figs. 13 and 14, for the current mirror circuit with constant current bias illustrate the dependencies of device area, separation distance, and bias on the current mismatch variance. Each simulation point on these graphs corresponds to 1000 Monte Carlo simulations using a CAD implementation of the SMOS model [19], [26]. Fig. 13 shows the importance of circuit layout and device size on circuit performance variance. Fig. 14 investigates the effect of bias, with the result that small $V_{GS} - V_T$ values (small I_{SS}) cause greater relative mismatch. Of course, the design of the bias point may be constrained by circuit performance requirements. It is important, however, for analog designers to be aware of the relative effect of transistor bias, as well as the device size and placement, on the reliability of circuit performance.

IV. DISCUSSION

Accounting for the effects of transistor separation distance and device size in the statistical model allows the simulation of circuits based on circuit layout and critical dimension. A byproduct of statistical modeling based on intra-die statistics is the possibility of optimizing the circuit layout or the device sizes. With a simulation tool based on this statistical model, accurate simulations of analog circuits can be performed in which the circuit performance is correlated to input parameter spread. This will

TABLE IV
MEASURED AND SIMULATED VALUES FOR MEAN AND STANDARD DEVIATION OF MIRRORED CURRENT FOR TWO DIFFERENT REFERENCE CURRENTS. ALL CURRENT VALUES ARE IN MICROAMPERES

		W/L = 3/2 μm/μm		W/L = 20/2 μm/μm		W/L = 20/4 μm/μm	
Statistic	Bias	Measured	Simulated	Measured	Simulated	Measured	Simulated
Mean	50 μA	50.05	49.98	49.90	50.05	50.15	49.94
	100 μA	100.13	99.86	99.92	100.02	99.88	99.92
D = 50-μm Standard Deviation	50 μA	0.815	0.828	0.642	0.647	0.407	0.390
	100 μA	1.462	1.477	1.080	0.990	0.519	0.667
D = 100-μm Standard Deviation	50 μA	0.824	0.843	0.708	0.843	0.577	0.537
	100 μA	1.476	1.538	1.196	1.252	0.850	0.848
D = 150-μm Standard Deviation	50 μA	0.857	0.845	0.857	1.180	0.808	0.752
	100 μA	1.552	1.596	1.427	1.711	1.141	1.140

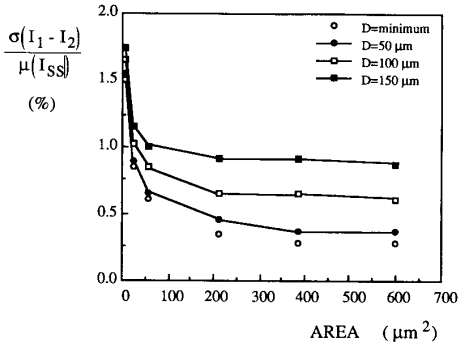

Fig. 13. Simulated device area and separation distance dependence of current mirror circuit. All simulations performed at I_{SS} = 50 μA and W/L = 1.5.

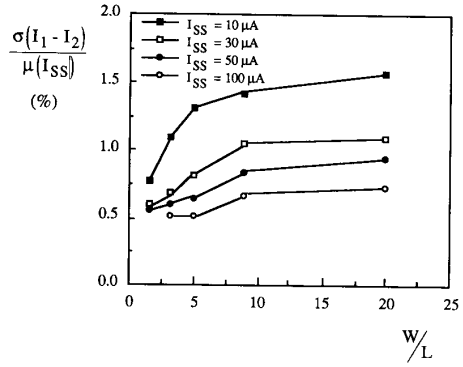

Fig. 14. Simulated bias dependence of current mirror circuit. All simulations performed for device areas of 80 μm^2 and at minimum separation distances.

enable the circuit designer to determine which transistors in the circuit contribute most to the output variance. Thus, the minimum device size for which the circuit will meet specifications or the circuit layout which minimizes mismatch-induced variance can be determined. A more detailed explanation of circuit optimization methods as well as the CAD aspects of this research will be explored in a later paper [26].

An important feature of the primary algorithms used to model device mismatch in this study, σSA and PCA, is that both algorithms are statistical in nature and, therefore, independent of model or technology. The BSIM SPICE model was chosen in this study due to its ability to accurately model short-channel transistors; however, any parameterized device model could have been used. Similarly, this study focused on the dc parameters in the BSIM model, but the model deck calculation procedures are equally valid for any model parameters including parasitic capacitances. Since model parameters are extracted from both the linear and saturation regions, the statistical model is valid for transistors operating in either region.

When formulating this or any statistical model, a large and accurate data base is necessary to characterize the process. In a production environment, an adequate data base can be amassed through extraction of model parameters from simple test structures, consisting of n- and p-channel transistors spaced at different intervals. Our statistical data base was extracted from two test chips fabricated through MOSIS. Since area was limited on these chips, the statistical data needed to model and simulate MOS transistors were gathered for n-channel devices only. Inclusion of p-channel devices into the statistical model is a simple extension of the modeling scheme presented in this paper. The mismatch, or intra-die, components of the statistical model can be assumed independent for n- and p-channel MOSFET's. For the inter-die variations, correlations between n-channel and p-channel model parameters can be determined and entered into an expanded correlation matrix. Thus, through PCA, parameter correlations for each device type on the die can be preserved.

V. CONCLUSION

As device feature sizes in analog circuits are reduced to the micrometer or submicrometer range, the effect of device mismatch on circuit performance and reliability

will be magnified. Statistical methods are required to simulate mismatch induced variance; therefore, an accurate statistical device model is required. This paper describes the SMOS model, a statistical parameter-level MOS model, from which statistically significant device model decks can be calculated.

The SMOS model is derived from the underlying mismatch variance model which contains the dependence of parameter variance on device size and spacing. Two statistical algorithms, principal component analysis and σ-space analysis, are employed to preserve parameter correlations within a transistor and parameter variances between transistors, respectively. The two statistical algorithms are integrated with the mismatch variance model to create a unified CAD-compatible statistical model for MOS transistors. The ability of the SMOS model to simulate circuit output variances based on intra-die statistics has been verified through experimental data gathered from two test chips. Simulated and measured circuit output variances and distributions showed excellent agreement.

Integration of this statistical model into a CAD environment will allow the analog circuit designer to estimate circuit yield based on a given set of processing-dependent model fitting parameters. Due to the ability of this model to accurately simulate the effect of device size and separation distance between devices on circuit output variances, we believe that this model can be an integral part of a circuit optimization scheme [27] which includes both device size and layout optimization. It is also possible that the SMOS model could be integrated into an automated circuit layout [28] or synthesis [29] environment to design circuits which meet yield requirements. Worst-case analysis [30] of analog MOS integrated circuits could also benefit from the SMOS model due to its ability to accurately model the effects of device mismatch.

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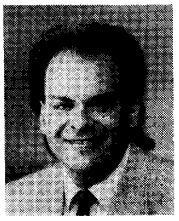
Christopher Michael was born in State College, PA, in 1964. He received the B.S., M.S., and Ph.D. degrees in electrical engineering from Ohio State University, Columbus, in 1986, 1988, and 1991, respectively. His dissertation work focused on statistical modeling and simulation for computer-aided design of analog MOS integrated circuits.

He was employed by Texas Instruments Incorporated, Dallas, TX, during the summers of 1989 and 1990, where he worked on fabrication equip-

ment modeling for process control. In 1991, he joined National Semiconductor Corporation, Santa Clara, CA, as a Senior Process Engineer. His primary responsibilities include device characterization and process integration for a mixed analog/digital process.

Dr. Michael was the recipient of a University Fellowship, a DuPont Graduate Fellowship, and a DuPont Teaching Fellowship while at Ohio State University.



Mohammed Ismail (S'80–M'82–SM'84) received the B.S. and M.S. degrees from Cairo University and the Ph.D. degree from the University of Manitoba in 1983, all in electrical engineering.

He has held several positions in industry and academia in the U.S., Canada, and overseas. He is currently with the Solid-State Microelectronics Laboratory at Ohio State University, Columbus, as an Associate Professor of Electrical Engineering. His current interests are in the areas of analog/digital VLSI design in CMOS/BiCMOS, CAD-compatible analog IC design, statistical modeling and simulation of device mismatch in VLSI circuits, and artificial neural information processing.

Dr. Ismail was an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS, 1989–1991, and of the *IEEE Circuits and Devices Magazine*, 1988–1990, and is currently the CAS Editor of the magazine. He is the founder and Editor-in-chief of *Analog Integrated Circuits and Signal Processing*, a new international journal. He is the Editor of the Kluwer Book Series on Analog Circuits and Signal Processing. He served on several technical committees and was the chairman of the IEEE Circuits and Systems (CAS) Society's Technical Committee on Analog Signal Processing (1987–1990) and the General Chairman of the 29th Midwest Symposium on Circuits and Systems (1986). He has published about 80 technical papers and co-edited and coauthored two books: *Analog VLSI Implementation of Neural Systems* and *Introduction to Analog VLSI Design Automation*. He is listed in *American Men and Women of Science* and in *Who's Who in Technology*. He has given numerous invited lectures and organized and chaired technical sessions, workshops, short courses and panel discussions at many international meetings. He has received several research and teaching awards including the U.S. National Science Foundation Presidential Young Investigator Award.