A Multigigabit DRAM Technology With $6F^2$ Open-Bitline Cell, Distributed Overdriven Sensing, and Stacked-Flash Fuse

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***Abstract*—A multigigabit DRAM technology was developed that features a low-noise $6F^2$ open-bitline cell with fully utilized edge arrays, distributed overdriven sensing for operation below 1 V, and a highly reliable post-packaging repair scheme using a stacked-Flash fuse. This technology, which can be used to fabricate a 0.13-μm 180-mm^2 1-Gb DRAM assembled in a 400-mil package, was verified using a 57.6-mm^2, 200-MHz array-cycle, 256-Mb test chip with 0.109-μm^2 cells.**

***Index Terms*—Array noise, DRAM, low voltage and high speed, memory cell, post-packaging repair.**

I. Introduction

HISTORICALLY, the development of dynamic random access memory (DRAM) has been the leading force in the advancement of semiconductor technology. The latest trend in DRAM technology emphasizes the reduction of costs, a result of the economic pressures imposed by the marketplace. Further development of DRAM technology in the areas of density, speed, and power will become increasingly difficult in the multigigabit era.

The development of higher density and smaller DRAMs necessitates a reduction of the cell area. Traditionally, the DRAM cell area has been reduced by a reduction of the feature size (F) and the cell area factors (cell area in units of minimum-feature-size-squared). However, the cell area factors have already reached 8, which is the minimum for the folded bitline (BL) cell [1]. The cell area is dependent on the feature size only as long as the development of a memory cell is based on the folded BL arrangement. The International Technology Roadmap for Semiconductors (ITRS'99) shows that memory cells smaller than the $8F^2$ cell are necessary to reduce the DRAM chip area, as shown in Fig. 1. ITRS'99 describes the required feature size and cell area factor to be 0.13-μm and 6, respectively, for 1-Gb DRAMs in 2002. Therefore, mass produced 1-Gb DRAMs having chip sizes less than 180 mm^2 assembled in a 400-mil package can be realized. Recently, a $6F^2$-trench capacitor cell has been proposed [2]. However, it needs additional tight-pitch layers to create a vertically folded BL arrangement, and a vertical-access transistor. Another candidate, a $6F^2$ capacitor-over-bitline (COB) cell has been reported [3]. It is difficult to produce these chips because of the additional transistors and the difficult timing control required to eliminate the array noise. Our proposed simple $6F^2$ open-BL cell array without the complicated structure and difficult timing control overcomes the inherent issues in the open-BL arrangement. These issues are the large noise and area penalty caused by the edge arrays. This paper describes the experimental array noise using a fabricated test chip to verify the efficacy of the noise-reduction schemes and fully utilized edge arrays.

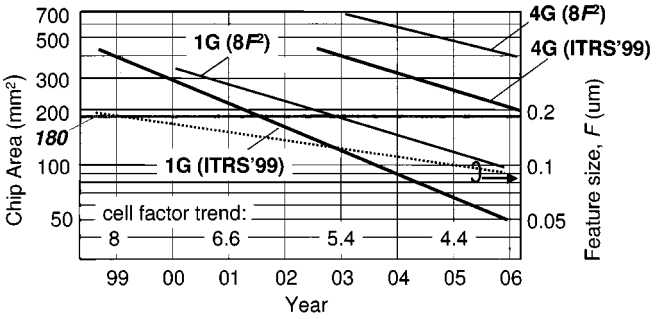

Fig. 1. DRAM chip area (cell efficiency 70%.

For low-voltage and high-speed operation, a high-bandwidth architecture and array sensing are essential. To decrease the speed gap between a microprocessor and a DRAM, a high-speed interface architecture such as Rambus-DRAM [4], double-data-rate (DDR) SDRAM [1], and DDR2-SDRAM [5] have been developed. They can improve the data-transfer rate, however, the array core speed cannot be improved. For high core speed at low voltage, we proposed a distributed overdriven sensing scheme.

Another concern of multigigabit DRAMs is redundancy for degraded cells (a variable retention time [6]) after packaging. Recently, an antifuse scheme using an oxide–nitride–oxide (ONO) storage capacitor was proposed [7]. However, use of this scheme will create two issues. One is that the reliability

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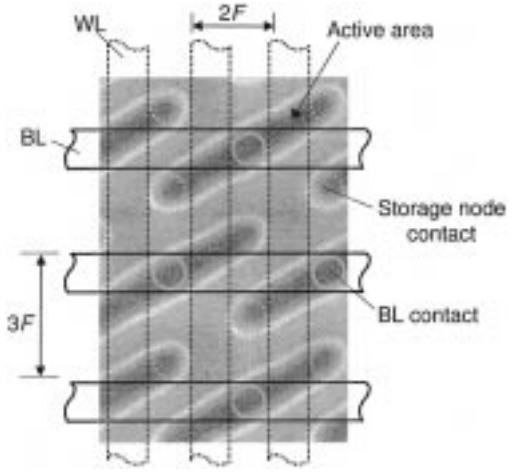

Fig. 2. $6F^2$ cell.

of a fuse must be assured for every change of capacitor structure. The other is that a high programming voltage of 8 V is needed to obtain the complete conduction of the fuse, and a high-voltage MOS transistor is also needed. Our proposal is a stacked-Flash fuse architecture. This scheme can be fabricated in the standard CMOS process without any additional process steps. The programming voltage for the Flash fuse is 5 V.

Our technologies are described in detail in the following four sections. In Section II, the fabricated $6F^2$ open-BL cell and experimental BL noise using the test chip are introduced. In Section III, a distributed overdriven sensing scheme to achieve low-voltage and high-speed array sensing is described. In Section IV, the post-packaging repair scheme using the stacked-Flash fuse is described. In Section V, the characteristics of the fabricated 256-Mb test chip are described.

II. $6F^2$ Open BL Cell Array

A. $6F^2$ Cell

To realize the simple structure $6F^2$ cell without any process changes is the key to mass-producing the chip. Fig. 2 shows the top view of our fabricated $6F^2$ cell, which is estimated as the simplest structure of the COB cells. This $6F^2$ cell features a 3F bitlines pitch and 2F wordlines pitch, and a simple open-bitline arrangement. The active area is the tilted structure.

B. BL-Signal Design Methodology

To be able to use an open-BL array, the noise reduction is essential when compared to the folded BL array. Therefore, we analyzed the BL signal and a portion of the noise margin in detail. Fig. 3 shows our target for the BL signal. The target must be considered for three margins: threshold voltage ($V_{\rm th}$) variation of sense amplifier transistors, retention time (tREF), and noise. For the $V_{\rm th}$ variation, ITRS'99 describes the $V_{\rm th}$ 3ϕ variation for 2002 as 42 mV, which depends on the voltages between the source and drain of the transistor. For the tREF margin, we have to guarantee that the margin corresponds to the 256-ms tREF required in multigigabit DRAMs. Consequently, the remainder of the signal is allocated to the noise margin, 42 mV in this work.

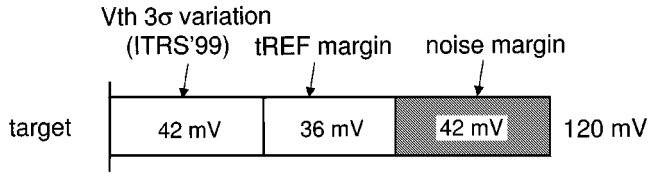

Fig. 3. BL-signal target. 0.13-μm technology, Cb = 120 fF (BL+SA), Cs = 25 fF, $V_{\rm array}(V_{dl})$ = 1.4 V, MC leakage current = 20 fA, retention time (tREF) = 256 ms.

C. Open-BL Noise

Previous open-BL cells suffered from a large noise imbalance between pairs of BLs, each of which is arranged in an adjacent array. The noise results from the large physical array size, which induces a large separation between each pair of BLs. As the feature size is miniaturized, each array becomes smaller with an almost fixed number of cells along each BL. This keeps each pair of BLs closer, thereby reducing any voltage imbalance between the adjacent arrays and making noise reduction easier. For example, in the 64-kb DRAM, the chip consisted of two or four unit arrays which are surrounded by the sense amplifiers and wordline drivers [9], and the scale of the unit array is about 3 mm^2. As the result, the chip itself is the noise source. On the other hand, the scale of the unit array of the current DRAM chip is less than 0.1 mm^2, based on a 0.13-μm technology. Therefore, noise reduction in current DRAMs becomes easier, when compared to that in the past DRAMs, because of the smaller activated area.

To demonstrate the accuracy of our assumption and perform an analysis of the open-BL noise—which are adjacent BL's noise, nonselected wordlines noise, cell plate (PL) noise, and p-well noise—we experimented with a quasi-open-BL array using a 256-Mb DRAM with 0.22-μm technology [10]. Fig. 4 shows the fabricated quasi-open-BL cell array and the simulation and experimental results of the noise. The simulated total noise was 76 mV and the measured total noise was 85 mV. This noise is very large compared to our target of 42 mV. Therefore, noise reduction is indispensable to the open-BL array.

D. Noise Reduction

The open-BL noise can be reduced by means of the noise reduction techniques featuring a low-impedance array and bridging of two arrays. To reduce the nonselected wordline noise, the wordline sheet resistance is reduced from 10 $\Omega/\square$ to 2 $\Omega/\square$. This is realized by the structure having a tungsten (W) and poly-Si double layer. To reduce the plate noise, plate-sheet resistance is reduced from 20 $\Omega/\square$ to 2 $\Omega/\square$. This is realized by a structure that piles W on the conventional titanium nitride (TiN) plate. The bridging of each array with a plate layer over the sense-amplifier region is also essential. To reduce the p-well noise, V_{BB} supply-voltage contacts are placed at both ends of a p-well.

Fig. 5 shows the experimental array noise of the test chip with 0.13-μm technology. The simulated array noise using the fabricated device parameters was 35 mV, and the measured array noise was 34 mV. This reduced noise is fairly small compared to our target noise margin of 42 mV.

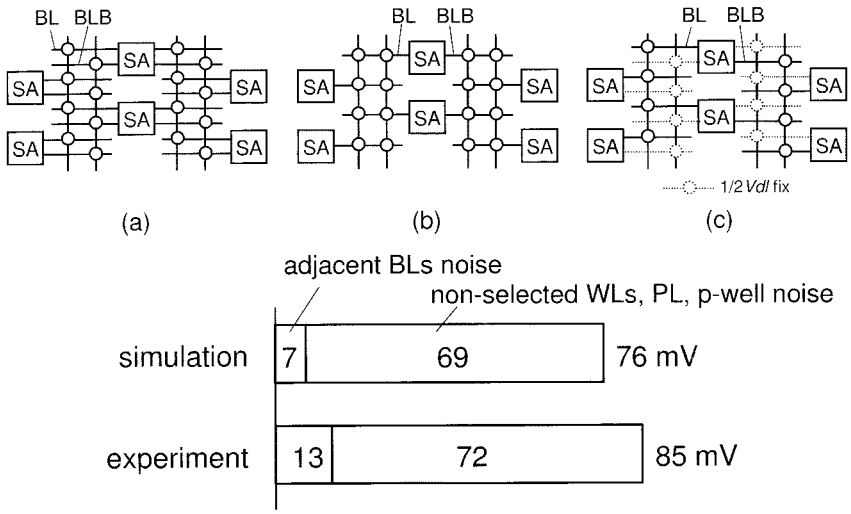

Fig. 4. Bitline noise of the quasi-open-BL array. (a) Folded. (b) Open. (c) Quasi-open.

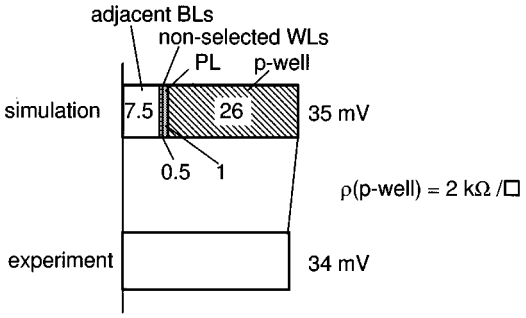

Fig. 5. Experimental results of the array noise.

E. Fully Utilized Edge Array

Another key feature of the $6F^2$ open-BL array is the full utilization of edge arrays. Fig. 6 shows the array architectures for the conventional and proposed edge arrays. In the conventional architecture [11], the edge arrays occupy about 5%–6% of the area of a 1-Gb DRAM using 0.13-μm technology. There are three features in our proposed architecture. The edge arrays consist of half-length BLs with the adjacent BLs connected to achieve the same capacitance as in the normal array. The edge arrays also provide redundancy. All the redundant WLs, which are distributed in plural arrays in the conventional scheme, are arranged in edge arrays. As the result, the area penalty can be reduced to below 2%. In addition, the cell signal almost doubles on the resultant BL because two cells (double Cs) are simultaneously activated. Thus, half-size edge arrays with stable operation and greater redundancy can be achieved.

III. Low-Voltage Sensing

Fig. 7 compares different array-sensing schemes. A conventional sensing scheme shown in Fig. 7(a) [12], in which the drivers are distributed in each sense amplifier region and combined using meshed power lines, could not achieve a high enough speed at an array voltage below 1.6 V, as shown in Fig. 8. This is because of the lower operating voltage (i.e., V_{DL} = array voltage $< V_{DD}$). Note that the $V_{\rm th}$ cannot be reduced to less than 0.1 V to obtain a low enough standby current. On the other hand, the conventional overdriven sensing scheme, shown in Fig. 7(b) [13], achieved a higher speed, even below 1.6 V, despite a high $V_{\rm th}$. This is because of a higher operating voltage (i.e., V_{DD}) at the early sensing stage. As the array voltage decreased to around 1 V, however, the parasitic resistance of long common-source lines (CSN, CSP) offset the advantage. Voltage losses due to deformed waveforms at the far ends of the lines were responsible for the speed degradation.

Our proposed distributed overdriven sensing scheme, shown in Fig. 7(c), features the combination of the two conventional schemes. This scheme enables a higher speed due to V_{DD} operation and reduced voltage loss by using the distributed drivers and meshed power lines. Consequently, the sensing time at 1.2 V, the minimum array voltage necessary for 1-Gb generation, improved by 6.9 and 2.0 ns compared with that for the conventional schemes, as shown in Fig. 8. This sensing scheme is promising for array voltage under 1 V in multigigabit era.

IV. Post-Packaging Repair Scheme

Fig. 9 shows the proposed post-packaging repair scheme using a more simplified stacked-Flash fuse architecture. As shown in Fig. 9(a), the floating gate consists of laterally connected pMOS and nMOS gates, which can be fabricated in the standard CMOS process. The control gate CG is the n-type well of the pMOS. The proposed stacked-Flash fuse circuit consists of Flash fuses, programming transistors and an address compare circuit, as shown in Fig. 9(b). This scheme features three series Flash fuses structure to realize reliability as high as that of the conventional metal fuse. This is necessary because there is the degradation issue of retention by the charge loss in the Flash structure. The resultant OR function can resolve this issue, because it can still maintain the fuse function until all of the stacked-Flash fuses are degraded.

Fig. 10 shows the control timing diagram of the Flash fuse circuit. The fuse controls of this scheme, which is the program and erase of the Flash fuses and data-read from Flash fuses to address compare circuit, are executed without the assignment of an extra pin after packaging. The test-mode state, which is defined as one of the mode register configurations, is assigned to

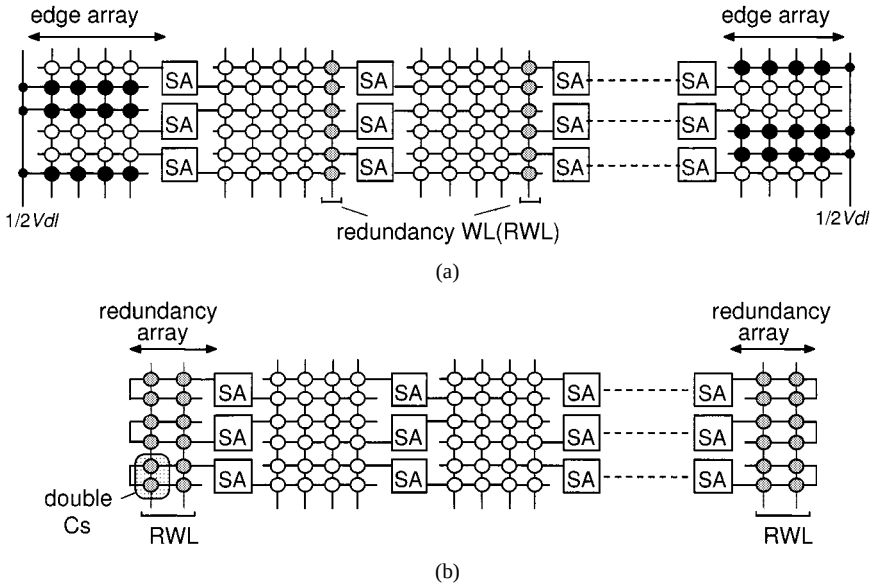

Fig. 6. Open-bitline architecture fully utilizing edge array. (a) Conventional. (b) Proposed.

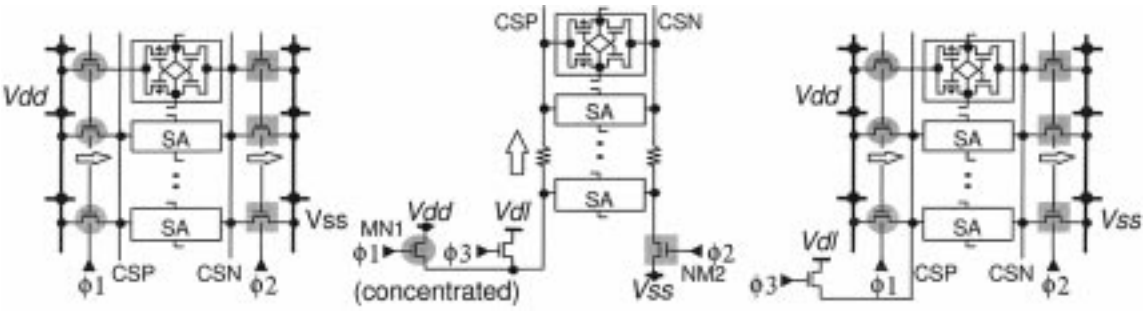

Fig. 7. Sensing schemes. (a) Nonoverdriven. (b) Conventional overdriven. (c) Proposed overdriven.

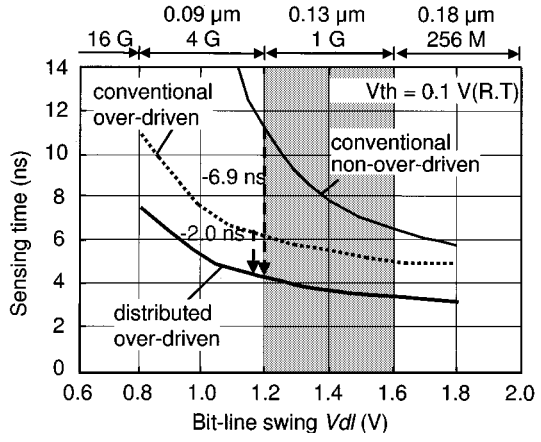

Fig. 8. Comparison of sensing times.

the program and erase modes. The data-read mode is executed by using the mode-resistor-set (MRS). In the program mode, the CG and SL are charged up to a high-voltage level and the BSL is at a low enough level to generate hot electrons in the programming transistors. After a certain programming time, the $V_{\rm th}$ of the three read nMOS transistors, for each of which the initial $V_{\rm th}$ before the program is below 0.5 V, becomes high. The erase of the programmed data uses Fowler–Nordheim (FN) tunneling electron ejection. The SL and BSL are charged up to a high-voltage level and V_{dl} level, respectively. The CG is set to V_{SS}. A read operation of the antifuse registers is executed by using the period of the MRS. In the read mode, the CG and $\phi 1$ are charged up to V_{dl} level after the precharge of the N2 node is completed. The total read time obtained from setting the MRS mode to the latched N2 node level was as fast as 5.8 ns.

Fig. 11 shows the Flash-fuse failure rate, which is noted as f. For the single Flash fuse, which is a nonstacked structure, the fuse failure rate has increased with decreases of gate-oxide thickness. This failure rate, which is the calculated result using the experimental formulation $f = ^{10-{\rm Tox}/0.5\ {\rm nm}}$, is not satisfied by our target fuse failure rate, which is less than 10^{-7}%, comparable to the soft-error rate. For the three-stacked Flash fuse, the failure rate can be reduced dramatically. For example, our scheme reduces the failure rate needed at the 1-Gb generation from the 0.18% of the single structure to 2×10^{-11}%. At 16-Gb generation, a four-stacked Flash fuse is sufficient.

V. Test Chip Design and Results

We verified this technology by designing and fabricating a 256-Mb test chip using 0.13-μm CMOS process technology. Fig. 12 shows a microphotograph of the chip. The chip scale

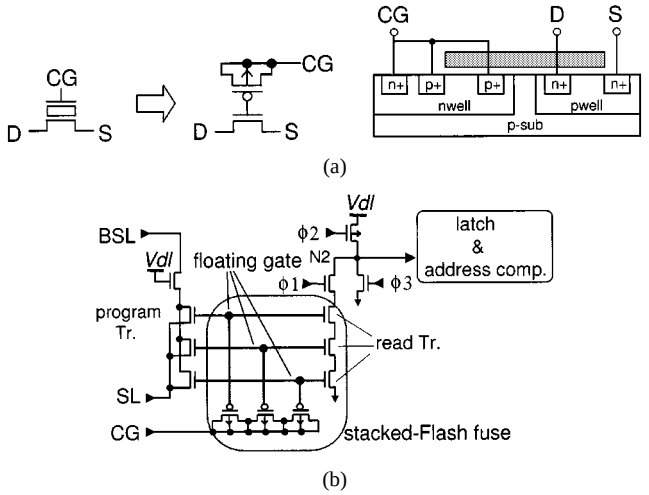

Fig. 9. Stacked-Flash fuse. (a) Single Flash fuse. (b) Stacked-Flash fuse circuit.

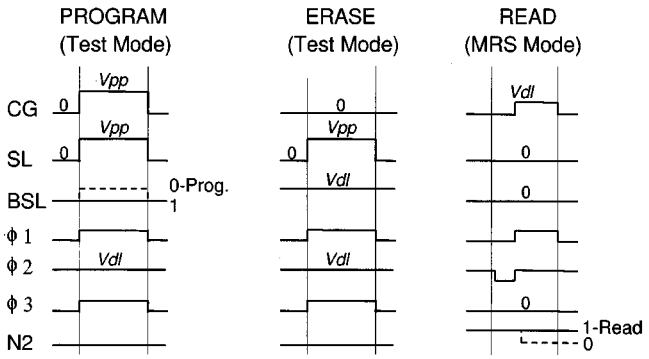

Fig. 10. Timing diagram of Flash-fuse circuit.

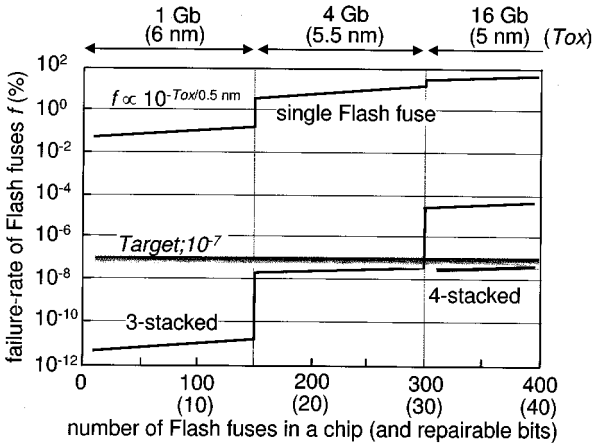

Fig. 11. Improvement of Flash-fuse failure rate.

was 11.76 × 4.99 mm. The unit array consisted of 512 word-lines and 1024 bitlines.

Fig. 13 shows the tCK shmoo plot of this test chip. The operating frequency of the array was 208 MHz, without the prefetch operation, at room temperature.

Table I shows the features of the 256-Mb test chip. The dual-gate and dual-oxide devices were used. The memory cell consisted of an MIM–Ta_2O_5 capacitor, and the memory-cell size was 0.109 μm^2. The chip size was 57.6 mm^2. The RAS access time was 26.5 ns.

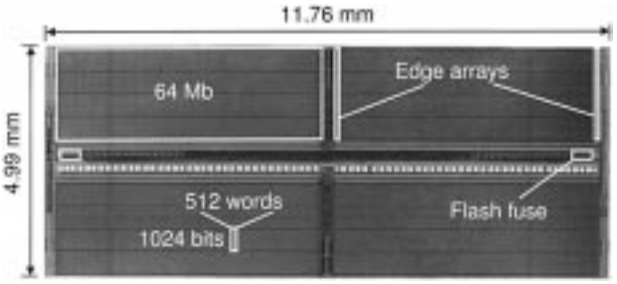

Fig. 12. 256-Mb chip microphotograph.

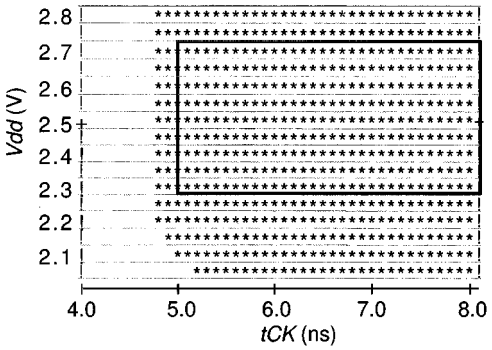

Fig. 13. tCK shmoo plot.

TABLE I
FEATURES OF 256-Mb TEST CHIP

Process:	0.13-μm CMOS, W-PolySi Gate
	Dual-Gate (P^+Gate-PMOS)
	Dual-*Tox* ;3.5 nm / 6.0 nm (optical)
Memory Cell:	$6F^2$ Cell with open bit-line array
	25 fF MIM-Ta_2O_5 capacitor
Cell size:	0.109 μm^2
Chip size:	57.6 mm^2
Power supply:	External 2.5 V/1.8 V
	Internal 1.4 V for array (typical)
Access time:	*tRAC*=26.5 ns
	Operating Frequency=208 MHz (non-prefetch)

VI. CONCLUSION

A multigigabit DRAM technology was developed that features a low-noise $6F^2$ open-bitline cell with fully utilized edge arrays, distributed overdriven sensing for operation below 1 V, and a highly reliable post-packaging repair scheme using a stacked-Flash fuse. The efficacy of this technology was demonstrated using a 57.6-mm^2 208-MHz array-cycle, 256-Mb test chip. This technology enables a 0.13-μm 180-mm^2 1-Gb DRAM which can be assembled in a 400-mil package.

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Dr. Itoh received the IEEE Paul Rappaport Award in 1984, the Best Paper Award of ESSCIRC90, and the 1993 IEEE Solid-State Circuits Award. He has won many awards in Japan including Commendation by the Minister of State for Science and Technology (Person of Scientific and Technological Merits) in 1997, and a National Medal of Honor with Purple Ribbon in 2000.