ESD Protection Device Issues For IC Designs

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Abstract

Electrostatic discharge (ESD) has been a major concern for IC chip quality. In this paper, the IC damage phenomena due to ESD and the protection techniques will be reviewed. Also, the severe impact of the advanced process technologies on the ESD robustness, and the special circuit requirements that make the protection design even more challenging will be addressed. The recently developed simulation and modeling methods to improve the protection designs will also be discussed.

Introduction

For the current advanced IC technologies, electrostatic discharge (ESD) and its potential destructive effects on VLSI chips are well known [1]. The damage phenomenon is from human handling as well as with contact from machines in automated assembly areas. Most of the failure modes have been related to thermal damage at the junctions (Fig. 1) or gate oxide rupture (Fig. 2), both of which can be prevented with effective protection clamp designs at the I/O signal pins. The IC chip functionality could also be affected with ESD damage to the internal core circuits, requiring protection at the power pins.

During the past 20 years major advances in IC ESD protection methods have been made. However, constantly changing process technologies and high performance chip design techniques have made the design for ESD very challenging. In this paper, the state-of-the-art ESD design techniques will be reviewed after an introduction to the basic ESD issues. The use of simulation and modeling method to improve the protection design efficiency will also be presented. Finally, the design verification methods for ESD reliability will be discussed.

ESD Stress Models

The major impact comes from the Human Body Model (HBM) ESD events that can occur when a charged person (100 pF) touches a packaged device through a finger resistance of 1500 Ohms. With an HBM charge level of 2000 V, this contact with an IC pin can result in a discharge event with a peak current of 1.3 Amps for a duration of 150 ns. On the other hand, the contact with equipment is represented by the machine model (MM) with a capacitance of 200 pF and a much lower series resistance that results in relatively higher peak currents of 3-4 Amps (for 200 V stress level) at pulse widths of 30 ns. Both HBM and MM usually result in the same type of thermal damage phenomena. The overall ESD reliability requires a minimum HBM level of 2 kV and a MM level of 200 V.

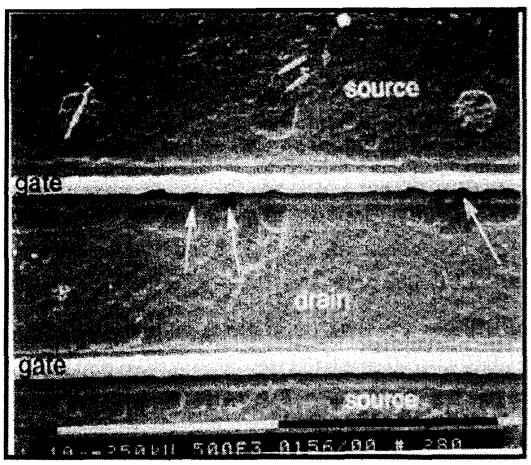

Figure 1. Typical thermal damage in an NMMOS transistor due to ESD.

ESD events in production areas can also occur when an electro-statically charged device is abruptly discharged to metallic ground. This gives

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rise to a very fast transient of several Amps (8-10 Amps) of peak current with a rise time less than 500 ps. This is called the Charged Device Model (CDM) that is rapidly becoming the main concern for ESD reliability. For CDM, the protection device trigger efficiency and the IR drops in the metal or poly-silicon lines become significant as they can lead to gate oxide damage. Thus the proper design of clamp circuits plays an important role for preventing ESD damage due to any of these stress models. The newer advanced technologies with the LDD junctions and silicided diffusions, as well as ultra-thin gate oxides, are making this protection design very challenging.

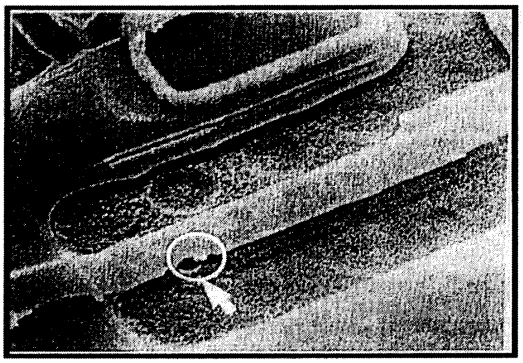

Figure 2. Gate damage to an input buffer under CDM stress. (Chaine, ESD Symp., 1994).

NMOS High Current Behavior

Fundamental to the ESD protection design is the high current behavior of an NMOS transistor. As indicated in Fig. 3, high field at the drain causes avalanche that leads to electron-hole pair generation and the hole flow towards the substrate (Isub) forward biases the source-substrate junction. The IV curve shown in Fig. 3 represents the parasitic bipolar turn on with the drain as the collector, substrate as the base, and source as the emitter. As shown in Fig. 4, the parasitic bipolar turns on with avalanche at the drain junction (Vt1). The substrate current then forward biases the source-substrate junction turning on the parasitic bipolar npn transistor which is indicated by the snapback region. This is followed by the second breakdown point (Vt2, It2) where thermal damage occurs. It2 represent the failure current normalized to the device finger width.

The robustness to ESD is measured by It2 which can be typically at 5 mA/μm as measured by 100 ns wide square wave pulses. This It2 then roughly translates to 10 V/um for the HBM. Therefore, a 200 μm wide transistor should provide 2 kV HBM level but this is not possible since the multi-fingers of the NMOS will not typically allow uniform turn on of the parallel bipolar transistors.

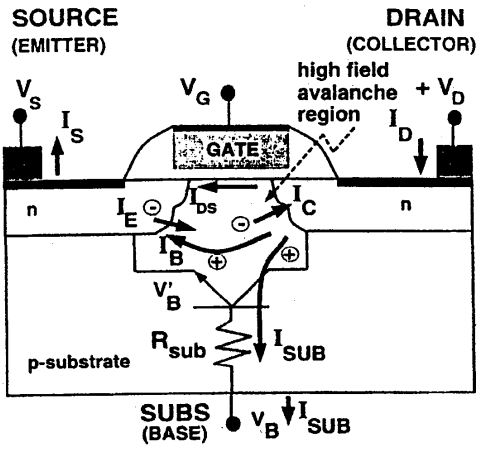

Figure 3. Cross-section of an NMOS transistor with advanced LDD junctions and silicided diffusions (shown as dark regions from drain/source contact to the sidewall edge of the gate) [4].

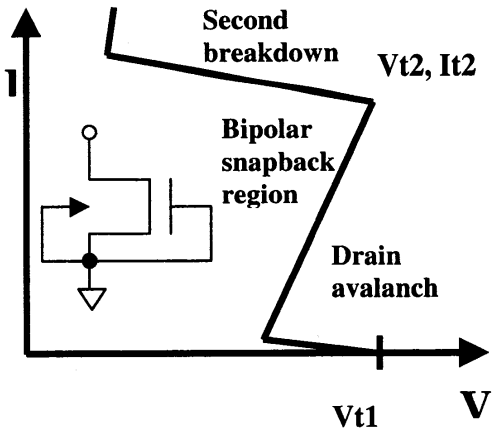

Figure 4. High current IV characteristics of an NMOS transistor under ESD pulses.

The Effects of Advanced Technologies

The parameter It2 is determined by the heating at the drain junction. If the drain contact is too close to the gate edge, the heating is not uniform and this is traditionally overcome by keeping the drain contact a few microns away to give a ballasting effect [2]. However, the introduction of silicided diffusions (see Fig. 3) degraded this design option [3,4]. The It2 is also determined to some extent by the junction depth. The use of lightly doped drain (LDD) transistors with shallow junctions also contributed to the degradation of It2. Lower the It2, the more difficult it is to design robust protection devices in a given silicon area.

The degrading effects of LDD and silicide can be overcome by implementing deeper implants at the source/drain or blocking the silicide with a mask. The It2 is also dependent on the substrate resistance. The transistor parameters that have impact on It2 are the channel length and the finger width. The gate bias and substrate bias can also have a further impact on It2. In mixed voltage technologies the output transistor has different implants for hot carrier reliability than the ESD transistor and thus obtaining good It2 requires process optimization [5]. Longer channel transistors will have lower It2 because of lower bipolar efficiency.

Another feature of the advanced technologies is the scaling of oxide thickness. Although the oxide breakdown under the short pulse ESD conditions is about 1.5X of the DC breakdown value, for very thin oxides this breakdown can approach close to the drain avalanche of the bipolar npn of the NMOS transistor. Therefore, any NMOS clamp used to protect an input gate oxide will not leave much margin for consistent and safe protection design [6].

ESD Chip Design

The basic concept of a protection clamp is to prevent damage to the input gates or the diffused junctions of an output buffer. As shown in Fig. 5, a primary protection (Clamp 1) with secondary protection schemes is used to protect the internal circuits. The primary device can be a large NMOS or an SCR type device [7]. The isolation resistor can be made of nwell, diffusion, or polysilicon [7,8]. The purpose of the secondary (Clamp 2) is to trigger the primary device as well as offer protection at the local gate of the input buffer. For the outputs, a secondary is not usually needed since the output can be the trigger device. In some cases large outputs can form as self-protecting devices if they have good It2.

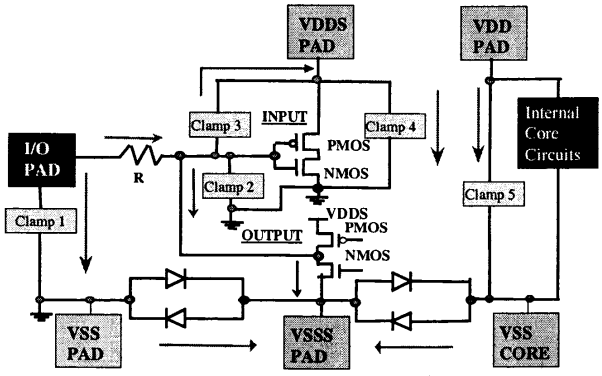

Figure 5. The I/O and Vdd pins are protected with various clamps.

In the case of inputs, Clamp 3 is required to protect the PMOS gate oxide. For CDM stress the inclusion of clamps 2 and 3 can be critical. Also, clamp 2 is effectively placed very close to the input buffer and its ground is connected to the same as the input ground. In the case of outputs, for noise isolation purposes the output ground (Vsss) could be different from the substrate ground (vss). The anti-parallel diodes shown between grounds are included to provide the complete ESD discharge current paths.

Besides I/O protection, the internal core must also be protected for direct stress on power pins (Vdd to Vss) or for indirect stress (I/O negative to VDD) leading to internal current paths. Clamps 4 and 5 ensure that this protection is provided. Incidentally, for very large chips with >10 nF Vdd capacitance, a protection device on the power pin is not really necessary. The common concerns for the future designs are the available I/O area for the protection circuit and the associated parasitics from the ESD device. These issues can become critical for high speed RF circuits and analog circuits. For minimizing the area, placing the ESD device under the bond pad is a good option

[9] as long as the other appropriate reliability aspects are carefully considered.

Protection Circuit Options

The NMOS as the parasitic npn protection device has been the most popular choice since the 2 μm technologies. Once successfully implemented, it can provide area-efficient protection at 1-1.5 V/μm ^2. However, the multi-finger NMOS may not turn on uniformly under ESD conditions, especially with silicided diffusions and/or low resistance epi substrates. This can happen since Vt1 is grater than Vt2 in Fig. 4. However, either gate coupling or substrate biasing can be used to lower Vt1 below Vt2 for uniform trigger [4,10]. The gate coupling, which is done by tying the gate to ground through a large (>10 kohm) resistor, would generate substrate current that would lower the Vt1 point in Fig. 2 to below Vt2, thus allowing more of the parallel npn's to turn on [10,11]. An optimum design window can be determined by process characterization as shown in Figure 6 [12]. Note also that the gate bias should not be too high since It2 can role off [11,12].

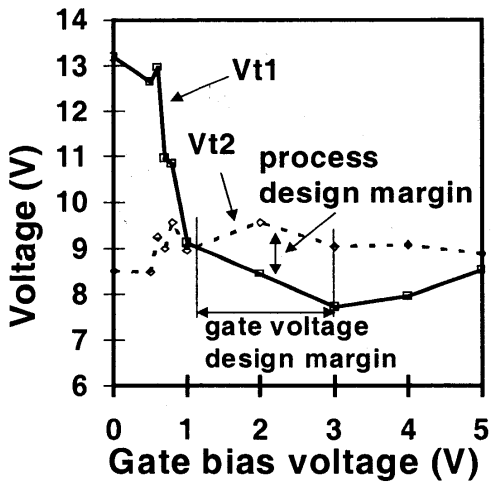

Figure 6. The Vt1 and Vt2 points of Figure 2 are a function of gate bias and for optimum protection design the window shown must be maintained [12].

Instead of gate coupling, gate driven techniques can also be used [15]. Any of these methods are effective but require SPICE simulations to verify that the gate potential is optimum. The gate coupling method works well for non-silicided technologies but may not be very effective if the silicide effect is combined with very low resistance substrates. In this case, substrate triggering techniques can be used to help the bipolar turn-on [4,11]. Figure 7 shows that a lateral diode connected to Vdd can also form a vertical pnp to pump the substrate. For this to be effective, the the diode is placed very close to the protection NMOS. The Vdd capacitance will have an effect on how well this scheme works [13].

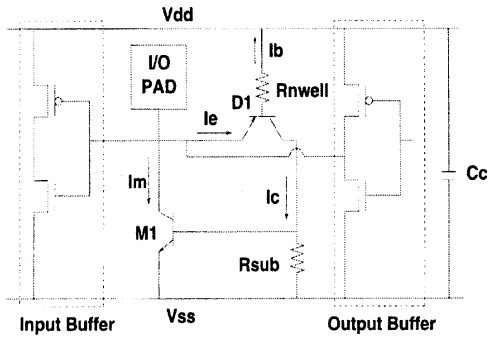

Figure 7. The I/O pad is connected to a lateral diode to Vdd which can also form as a vertical pnp to pump the substrate [13].

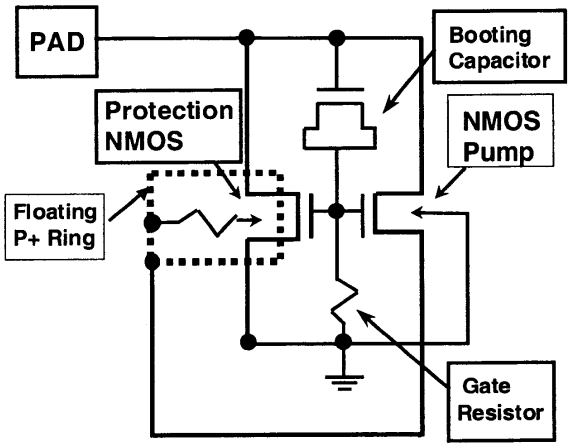

Figure 8. An NMOS source follower connected to a floating p+ ring can provides transient substrate bias. The design can be optimized with simulations [14].

In the case of low Vdd capacitance or when a diode to Vdd is not allowed (fail-safe operation), a secondary NMOS pump can be used as shown in Fig. 8 [14]. In this implementation, a floating

p+ ring is biased with source-follower pump. The capacitor and the resistor allow transient pump operation to generate substrate bias around the protection NMOS for uniform trigger. This technique is effective even for technologies with low resistance substrates and silicided diffusions.

Mixed Voltage Protection

Another consideration is voltage-tolerant protection where the gate oxide stress can limit the use of single MOSFET's as protection devices. In these cases, cascoding can be used as shown in Fig. 9. For the cascoded NMOS the effective It2 degradation as well as the integrated layout approach should be considered [15]. For 5-V tolerant signals a stack of diodes to Vdd can be used as shown in Fig. 10. [16].

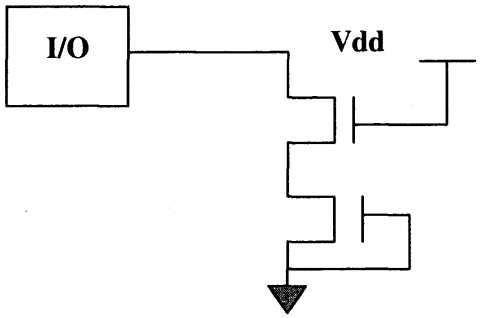

Figure 9. A cascoded approach for NMOS protection.

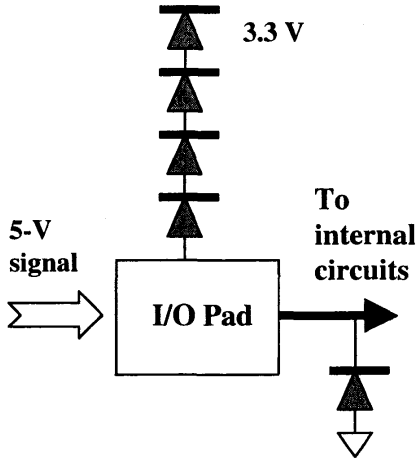

Figure 10. Mixed voltage protection with diode stack. The diode to ground can be replaced with cascoded NMOS devices. The Darlington Effect can cause leakage and hence snubbing resistors should be added.

Special Protection Designs

Besides standard CMOS, there are other technologies that require special ESD considerations. In BiCMOS the inherent bipolar devices can form as effective protection elements [17]. The bipolar npn is relatively more efficient and can be used as a protection device for BiCMOS outputs. Similar to the NMOS design (Fig. 7), the base of the bipolar is triggered. For SOI technologies, the NMOS as npn can be used but due to the isolated substrate the channel heating effects can reduce the It2 with gate coupling [18]. The protection device techniques are either gate coupling [18] or substrate coupling [19]. Power MOSFET's such as lateral DMOS (LDMOS) and drain-extended NMOS (DENMOS) are sensitive to ESD since the parasitic bipolar is difficult to turn on compared to the low voltage CMOS. These require custom designs as for example given in reference [20].

High Speed and RF Protection Designs

In general, NMOS protection devices have limitations when the It2 of the technology is too low and cannot be optimized without process changes that might have impact on other reliability concerns and/or circuit performance. In such cases dual diode protection is a viable approach provided that an efficient clamp is placed between Vdd and Vss.

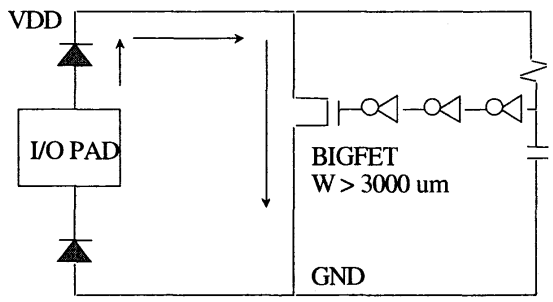

Figure 11. For high speed protection designs a diode to Vdd and a diode to GND can be used as the protection scheme. The inclusion of the BIGFET clamp ensures that the ESD current is discharged without any voltage buildup [21].

In the scheme shown in Fig. 11, a large NMOS, known as BIGFET [21] is designed with an RC timer such that when Vdd charges up during stress on the I/O pin with respect to GND, the MOS device goes into conduction for the entire ESD event. However, this device needs to be several thousand microns wide to handle the high ESD current. Design of this approach requires careful consideration such that bus resistance drops do not disable the timer circuit.

In the past, most of the RF designs have been made on BiCMOS and GaAs processes. The protection design for BiCMOS has been well investigated by Chen [22] but for GaAs the good protection has been difficult to achieve making them sensitive to ESD. Recently there has been an increasing interest in RF applications in CMOS. In these applications the parasitic load of the ESD device should not degrade the high frequency signal. A typical specification for a 2 GHz high speed application circuit could be 200 fF of loading capacitance with no series resistor. For analog operation, the linearity of this capacitance with signal bias should not exceed 20%. One recent study [23] established that the dual diode protection scheme as shown in Fig. 11 can meet this criteria for advanced CMOS technologies. Although still in the initial development stage, the use of heterojucntion Si-Ge bipolar transistors (HBT) integrated with mainstream advanced CMOS seems to offer both excellent analog and RF performance as well as robust ESD [24]. As the demand for even higher speed operations surface, alternate protection schemes such as distributed networks may have to be investigated [25].

Internal Chip Protection

The total ESD protection should also take into consideration current paths between the power supplies. If protection at the Vdd pin is not effective, the ESD current can go through the internal circuits and cause Idd leakage as shown in Figure 12 [26]. When the I/O pad is stressed negative to Vdd, the current flow is from Vdd to the I/O pin and any large clock driver close to Vdd tends to turn on. For this reason, it is usually effective to place a protection device very close to the Vdd pad. Bus resistance plays a very important role. Internal protection is expected to become more critical as the technologies are scaled down. If the I/O's operate at 3.3 V and core at 1.8 V, both 3.3 V and 1.8 V protection devices have to be used for the respective power supplies.

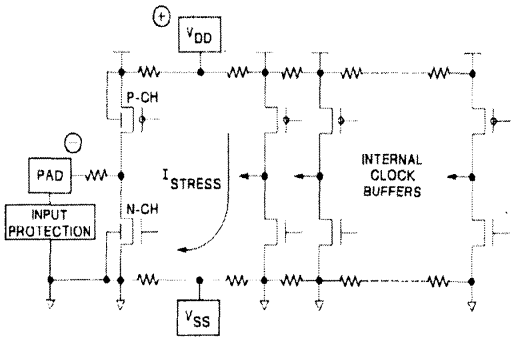

Figure 12. When an I/O pad is stressed negative to Vdd, current go through the internal circuits [26].

ESD Failures and Design Verification

The most demanding aspect of ESD from the product design groups is that adequate protection levels be available for the new IC chip to meet both internal and external customer qualification requirements. Many design/product engineers do not realize that the ESD protection device performance involves complex issues such as the sensitivity of the protection device to layout and process fluctuations, as well as numerous parasitic effects. In many cases, all of these cannot be fully comprehended until the design goes into silicon thus making it very difficult to achieve first pass success. This can be at least partly addressed with improved simulation methods for predictive capability [27]. Another approach is to implement software programs that detect ESD design and layout errors before a chip is released for mask. Some common errors are: wrong type of protection circuits, wrong hook-up of the protection circuits, insufficient placement of contacts, improper bus connections that cause excessive resistance and unintended layout errors that can result in interaction to nearby diffusions [28]. Note that certain minimum spacings must be maintained to avoid the last parasitic failure.

Also, these spacing rules depend on the specific technology that is used. An ESD checker software program (Fig.13) that can be used for compliance to the ESD guidelines has been reported in [29].

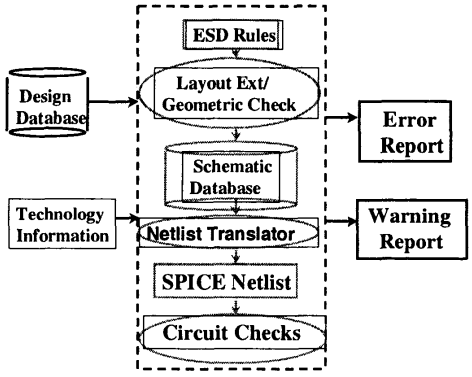

Figure 13. Flowchart for a software program that can detect design and layout ESD errors [29].

ESD Simulations

There has been much progress in using SPICE simulations for ESD circuit design and optimization. The most important aspect is to take

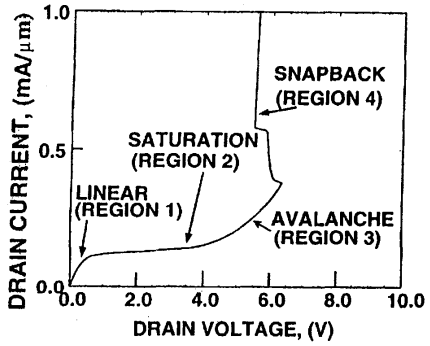

Figure 14. IV curves of an NMOSFET. Regions 1 and 2 are modeled for circuit operation, but regions 3 and 4 are important for ESD behavior [27].

the NMOS into the high current bipolar regime as shown in Figure 14 [27]. This program considers the bipolar behavior of the NMOS transistor as indicated in Figure 3 where the high field avalanche current and substrate current are considered. The key to predict the MOS behavior under ESD is to model the behavior for gate bias, substrate bias, and scalable effects with channel length and width. Indeed for accurate simulations the substrate resistance network modeling is important [30].

An example of ESD SPICE simulation is shown in Fig. 15 [31]. In this case the internal clock circuit failed for 2 kV stress between Vdd and I/O pins (see Fig. 12). The failure was in the circled NMOS. One single finger (35 um) of N1 goes into bipolar npn mode. In Fig. 15 the HBM simulation equivalent (a) and the simulation results (b) are shown. Although most of the ESD current was through the Vdd protection (SCR), some branch of it (300 mA) through N1 caused it to fail since it exceeded the It2. Simulation as in this example can be used to optimize the layout to prevent the internal failure.

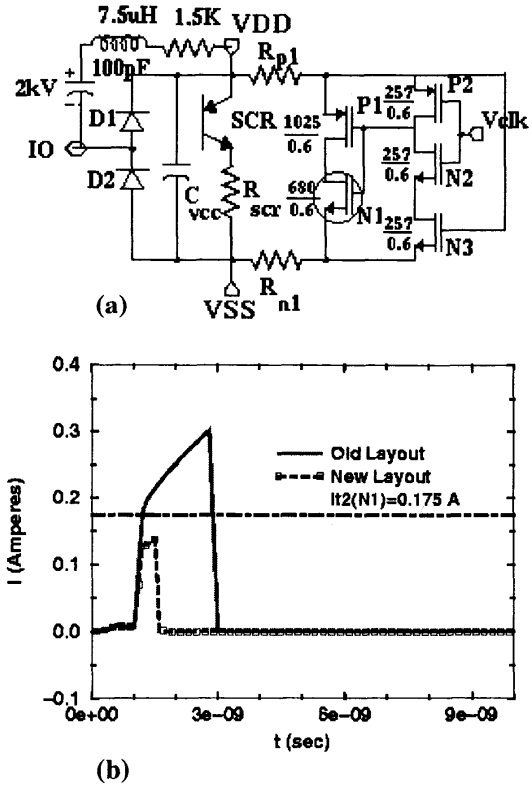

Figure 15. (a) ESD simulation circuit for HBM sress between Vdd and I/O. (b) Waveforms showing current through N1 for which a single finger of 35 um goes into bipolar conduction. Old Layout shows the current above the failure level at 175 mA, and the New Layout where an increase in Rp1 limits the current through N1 to below the failure point.

Future ESD Issues

Cell based library approach is the most common practice for delivering ESD protection circuits to the design groups. These libraries must contain all standard cells as well as special application designs. High speed analog circuit applications now demand more innovative protection circuit concepts.

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