Substrate Pump NMOS for ESD Protection Applications

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Abstract - The use of a substrate pump to achieve uniform npn protection in a multi-finger NMOS is reported for advanced CMOS technologies with silicide. The novel feature of this device technique is the implementation of a floating guardring to effectively pump the local substrate of the protection NMOS. SPICE simulations are presented to illustrate the device concept as well as the device design optimization.

Introduction

The advances in submicron CMOS technologies continue to challenge the effective design of on-chip protection circuits. The use of silicided junctions has played the most significant role on the development of ESD designs that use NMOS devices as the lateral bipolar npn [1]. Some early work [2] as well as some recent significant work [3,4] were reported to understand the effect of silicide and how to improve the ESD robustness with its presence. However, many in the industry continue to use some form of silicide block to ease the protection designs. While this is generally effective provided the source/drain junctions are optimized for ESD robustness, it can add expense to the process as at least one extra mask is required. Therefore, an ideal method is still to use design techniques to overcome the effects of silicide to achieve good protection. This paper will present an effective method to bias the substrate of the protection NMOS to achieve excellent ESD levels under all different design conditions for sub-half-micron fully salicided CMOS technologies. The flexibility of meeting the design specifications will be one of the key issues for a practical design.

I. NMOS Protection Device Concepts

The ESD design concepts of gate bias and substrate bias for uniform bipolar npn turn-on of the multi-finger NMOS under ESD conditions was first mentioned by Polgreen et al. [5]. This paper very clearly identified the difficulty in achieving uniform *npn* trigger in a multi-finger NMOS and how these techniques might help. These methods which have been effectively used by several authors include the gate-coupled NMOS (GCNMOS) with a large gate resistor to ground for gate bias effect during ESD [6], gate modulated NMOS (GMNMOS) with gate bias control [7], substrate trigger NMOS (STNMOS) with vertical PNP substrate pump [3], and lateral PNP gate driven NMOS (PDNMOS) which is more efficient than the GCNMOS [8]. All of these devices have their own limitations. For example, the GCNMOS seems to only work effectively for non-silicided technologies and is generally ineffective for thin epi substrates, especially when combined with silicided diffusions.

The STNMOS, on the other hand, is effective even for thin epi by using a substrate trigger effect through the vertical *pnp* formed with implementation of a lateral diode to Vdd near the NMOS, but its effectiveness can be limited by the Vdd capacitance [9]. The PDNMOS overcomes this Vdd capacitance effect but, like the STNMOS, has an inherent diode to Vdd at the signal pin making it inapplicable for fail-safe operation where the input signals are required to go above Vdd. In this paper, a new device concept with an NMOS substrate pump that overcomes these limitations and is effective for wider circuit applications is reported.

II. Substrate NMOS Pump Design

The NMOS substrate pump concept is shown in Figure 1. The protection NMOS gate is shared with a source-follower NMOS that forms the substrate pump. The source of the pump device is not connected directly to Vss but is instead connected to a floating P+ guardring that uniformly surrounds the protection NMOS. The guardring is indicated by the dashed line in Figure 1 along with the parasitic resistances. Note that the gate booting capacitor and the gate resistor allow the design of effective gate coupling during ESD. The capacitor can be an NMOS with its source and drain shorted to form a MOS capacitor and the resistor could be built with nwell.

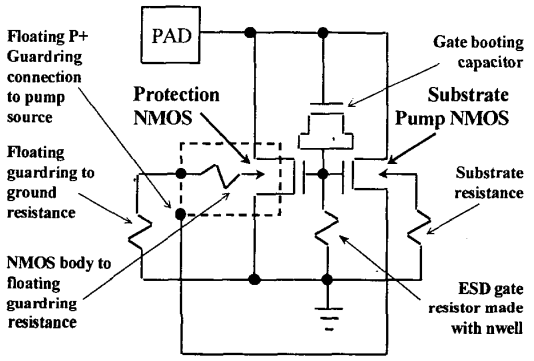

Figure 1: Circuit schematic of the substrate pump NMOS protection device. The floating p+ guardring is shown by the dashed line.

Since the protection NMOS and the substrate pump NMOS share the same drain and gate, these transistors can be integrated to make the layout more compact as well as uniquely efficient. In the actual implementation used, the multifingers of both devices are integrated as shown in Figure 2 The floating P+ ring that surrounds the composite structure is connected with metal to the source fingers of the pump device. There are three distinct advantages for this type of layout: 1) the ratio of the protection device width to the pump device width can be easily tuned to optimize the design, 2) the pump current is effectively fed to the floating guardring to provide substrate bias without any loss due to IR drops, and 3) the ring approach allows uniform substrate resistance as seen by all fingers of the protection NMOS. The importance of pump design is described later. The capacitor and resistor elements can be placed outside of this multifinger structure. In the layout of Figure 2, the placement of the guardring for latchup protection can play a critical role in the effectiveness of the device operation.

III. Device Operation

The key feature of this device concept is the application of a very brief (<1 ns) substrate bias transient to effectively turn on the *npn*. With a positive ESD pulse at the pad with respect to ground, the protection and pump MOS devices simultaneously turn on and the current flow through the latter supplies a transient bias to the floating substrate ring. The effectiveness of this scheme is determined by several factors: 1) the relative size of the pump NMOS, 2) the floating guardring resistance to ground which in turn is determined by its layout and separation to nearby latchup P+ Vss guardring as indicated in Figure 2 by parameter **d,** 3) the NMOS body resistance to ground which is determined by the substrate technology, and 4) the booting capacitor. High current ESD SPICE simulations can be used to optimize the design for any technology.

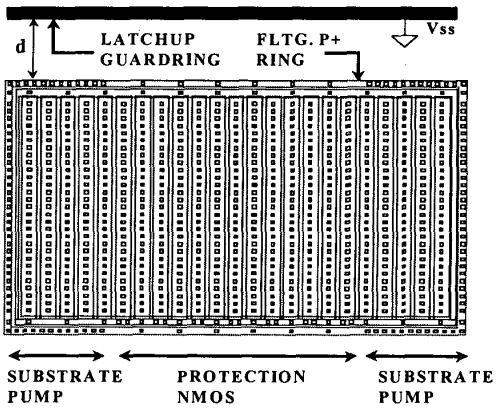

Figure 2: Layout of the substrate trigger NMOS device with the integrated substrate pump. The sources can be programmed to change the pump ratio. Note that the gate capacitor and gate resistor of Figure 1 are not shown.

To understand the effective operation and the design criteria for this device, the various equivalent resistance values extracted from the layout should be first considered. A cross-section of the protection scheme is shown in Figure 3 for a thin (3.5 μm) epitaxial substrate technology.

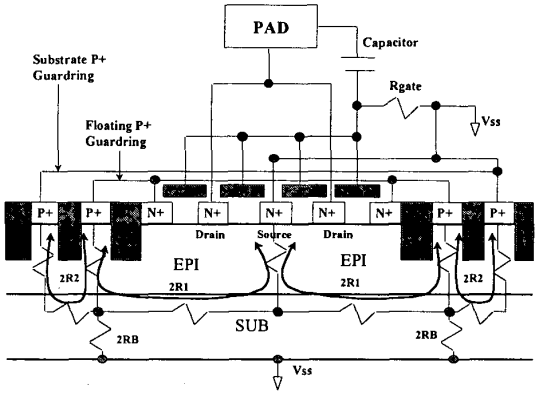

Figure 3: Cross-section of the substrate pump NMOS protection device with the parasitic resistances from the floating P+ and latchup P+ guardrings.

The effect of the nearby latchup guardring is also included. There are several effective resistance values that need to be considered. The shape and aspect ratio of the floating P+ ring determine the effective resistance R1 (which is shown as 2R1 for each side due to symmetry). With this ring approach, each finger of the protection NMOS essentially should see the same amount of resistance. The placement of the P+ latchup ring determines the effective resistance R2. Resistance RB is mainly determined by the substrate technology. For this protection scheme to properly work all of these resistances have to be taken into account and this in turn will be important for the effective pump design.
This device concept is demonstrated here for a 3.5 μm epi substrate, fully salicided mixed voltage technology with 0.5 μm channel length, 80 Å gate oxide, 3.3 V transistors; and 0.30 μm, 40 Å gate oxide, 1.8 V transistors. The source and drain are LDD built with Phosphorus and Arsenic implants.

Both the 3.3 V and 1.8 V NMOS transistors have an It2 value of 5 mA/μm. In this technology, the GCNMOS failed below 1000 V HBM because of the combined silicide and low substrate resistance effect. The implementation of the NMOS substrate pump designed with circuit simulations to significantly improve its ESD performance is described in the next section.

IV. Design Simulations

Figure 4 shows the equivalent schematic for simulations. The critical point of the simulations is to establish a proper bias at VSUB to uniformly turn on the *npn*. The pump current IP and the device substrate current IB contribute to this effect. The parasitic resistances RB, R1, and R2 were extracted from the layout using a substrate resistance extractor program described in reference [10]. The gate resistor RG is typically 15 kOhms and the gate capacitor represents the equivalent capacitance of a 10 μm/ 2 μm NMOS.

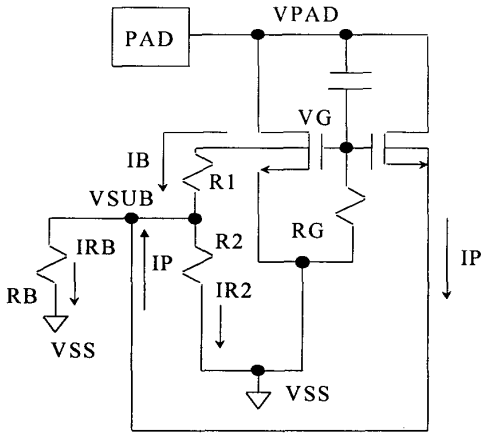

Figure 4: The schematic representation for simulations. R1, R2, and RB correspond to the effective resistance values indicated in Figure 3. IP is the pump current and IB is the substrate current.

The simulations were done with the high current SPICE program reported in reference [11] after modeling the NMOS transistors for this technology. For this design the protection NMOS is 480 μm wide and the pump device is 320 μm. Both are 3.3 V, 0.5μm channel length transistors. A positive 4 kV ESD HBM pulse was applied to the schematic shown in Figure 4 from VPAD to Vss. The voltage waveforms for the first

500 ps are shown in Figure 5. The pad voltage clamps around 5 Volts with the *npn* turn on and at this time the gate voltage is at 1.6 Volts. This is an ideal condition for the peak substrate current (IB). The current waveforms, for the same conditions shown in Figure 6 indicate that the peak IB is 5 mA. Note that IB tracks with the VGATE waveform in Figure 5.

The pump current IP is 25 mA and the total current of 30 mA branches into IRB and IR2 (see Figure 4). With an effective resistance of 23 Ohms from the parallel combination of RB and R2 for this device, this leads to 0.7 V for VSUB as seen in Figure 5.

The key feature for this device is the substrate bias to uniformly turn on the *npn* [3,12]. Note

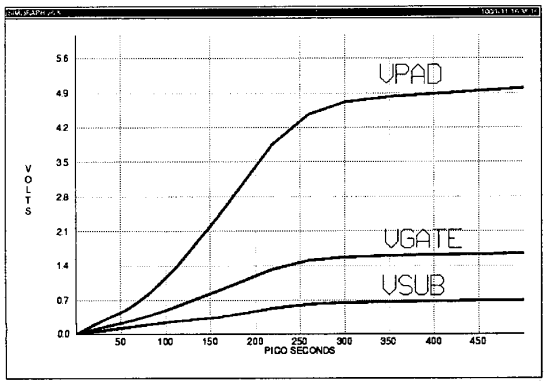

Figure 5: Simulation waveforms for a 4 kV HBM pulse for the circuit in Figure 4. The substrate voltage reaches 0.7 V as the pad voltage begins to clamp.

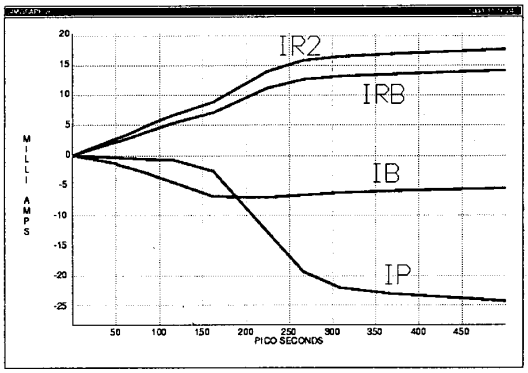

Figure 6: Simulation waveforms for a 4 kV HBM pulse for the circuit in Figure 4. Note that IB plus IP in magnitude is equal to IR2 plus IRB.

that if the NMOS pump is absent as in the standard GCNMOS, the substrate current IB alone would not produce sufficient VSUB for the multi-finger *npn* trigger. This now gives an insight as to why the GCNMOS does not effectively work for thin epi substrates. If the diffusions are not silicided or a silicide block is used, the ballasting of the NMOS with sufficient contact to gate spacing might help the GCNMOS. However, for overall efficient operation in the advanced thin epi or the low-resistance non-epi substrate technologies the substrate pump is essential to achieve consistent and uniform *npn* conduction under ESD.

V. ESD Results

For the 0.5 μm transistors, the **It2(@200 ns)** is 5 mA/μm which can roughly translate to 11 V/μm HBM level. HBM characterization showed that the minimum failure level for this 480 μm wide device was 5200 V with a spread of 5.2 kV to 5.6 kV. The IV curve taken with a Barth Electronics curve tracer with 100 ns pulses is shown in Figure 7. Note that the NMOS device clamps at about 5.5 V in agreement with the simulation in Figure 5 and has an on-resistance of less than 2 Ohms.

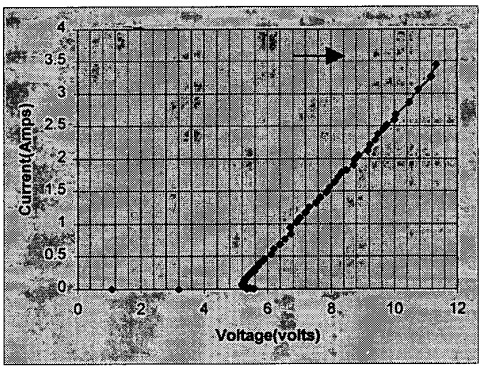

Figure 7: High current TLP data for the substrate pump NMOS of 480 μm wide. The failure current indicated at the arrow is 3.5 A.

The failure point is reached at 3.5 Amps. This corresponds to an expected **It2(@100 ns)** of 7.8 mA/μm and demonstrates uniform *npn* turn on for both HBM and TLP. Further, the HBM levels

were fully scalable with device width as shown in Figure 8. The data was taken with 250 V steps and the failure corresponded to a sudden increase in drain leakage current from nA to uA range. The Machine Model performance was between 225 and 250 V. This corresponds to an HBM/MM ratio of about 20-23 as expected for a silicided NMOS. The Charged Device Model performance was 1000 V with the field induced model. The failure was for negative CDM stress at 11 Amps peak with a drain-source melt filament indicating that the substrate pumped NMOS triggers as an *npn* [13] even under the fast FCDM event with an **It2 (@CDM)** of ~21 mA/μm.

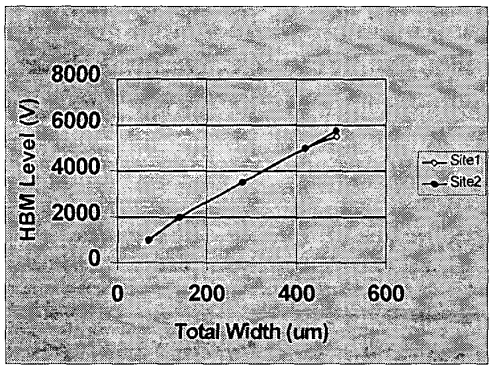

Figure 8: HBM ESD level as a function of device width for two different sites. The data was taken with 250 V steps for positive to Vss. Note the full scalability with 11 V/um of performance.

VI. I/O Protection Implementation

In the previous sections the substrate trigger NMOS ESD device concept, its design, and its performance for HBM, MM, and CDM stress models was demonstrated. However, the practical implementation requires consideration of the I/O function. This protection device has been used for both input and output pins as well as Vdd power pins as described below.

a. Inputs

In the case of inputs the stand-alone device forms the protection device as shown in Figure 9. In this application it forms a fail-safe protection since it can effectively work without the need for a diode to Vdd. Although the gate resistor R1 is essential for the substrate pump concept, it can influence the maximum tolerable capacitance. This is overcome by adding the additional circuitry of N1, N2, and R2. When Vdd is on, the transistor N1 essentially shorts out the gate resistor R1. The purpose of N2 and R2 is to allow a delay time in case Vdd charges up during ESD testing [14]. For example, when I/O pins are stressed in sequence the floating Vdd pin can pick up charge and change the effective resistance of R1. In such a case R2 will provide the time delay while N2 keeps the gate of N1 off during the transient event only. Thus the control circuitry will short out the gate R1 during normal operation but allows it to be effective for the short transient ESD pulses.

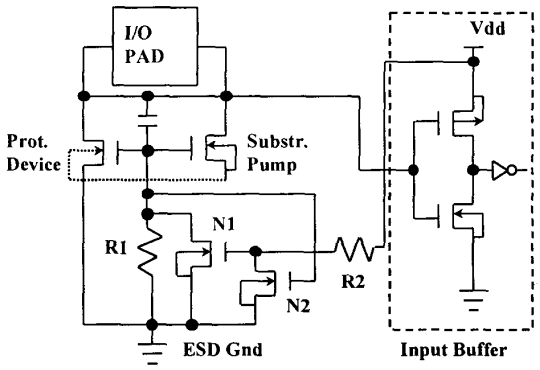

Figure 9: Input buffer protection scheme with the substrate pump NMOS. N1, N2, and R2 form the control circuitry to short out R1 during normal operation while allowing to be effective during the ESD transients.

b. Outputs and Bidirectionals

For the outputs, the same protection device can be placed in parallel to the output transistors as shown in Figure 10. For the bi-directionals, the protection device is combined with input and output.

No series resistor between the ESD protection transistor and the output NMOS is required since the substrate pump allows the protection device to turn on first. As recently reported in reference [15], for a mixed voltage technology application when the output transistor is optimized for hot carrier reliability its It2 can decrease. Even for

such a case, this concept is still applicable. However for optimum CMOS output protection implementation, the vertical *pnp* diode pump as described in reference [3] can still be used for improved reliability. This is achieved with the diode D1 in Figure 10. In this case both the NMOS pump and the vertical *pnp* pump provide enough substrate current to protect the output regardless of the Vdd capacitance size. The diode D1 can be used for any I/O pin as long as there is no fail-safe operation required.

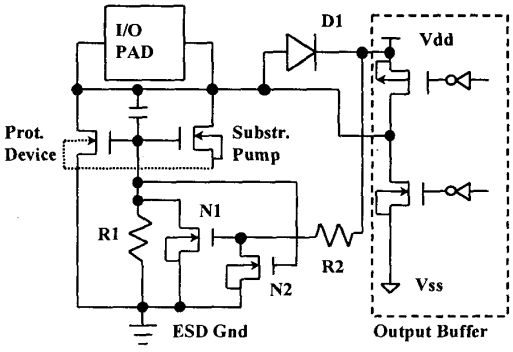

Figure 10: Output buffer protection scheme with the substrate pump NMOS. N1, N2, and R2 form the control circuitry to short out R1 during normal operation and prevent R1 being shorted during ESD transients. Diode D1 provides additional substrate pump to from the vertical *pnp*.

c. Power Pin Protection

Although the same basic protection can be used for the Vdd power supplies, the design should consider the effective capacitance of the Vdd bus. If for example the Vdd capacitance is in the order of few hundred picofarads the slower rise time of the ESD pulse would discharge the gate of the protection device to nearly zero volts before the drain avalanche is reached. This can be overcome by increasing the size of the booting capacitor in Figure 1. The IV curve for the protection device on a 1.8 V Vdd pin (well below its failure point) is shown in Figure 11. After about 1 V the internal circuits turn on and at around 4.5 V the protection NMOS trigger can be seen. For this core 1.8 V power supply, burn-in voltages of up to 4 V can be applied with no destructive effects. The 3.3 V Vdd pin also can use the same type of protection device.

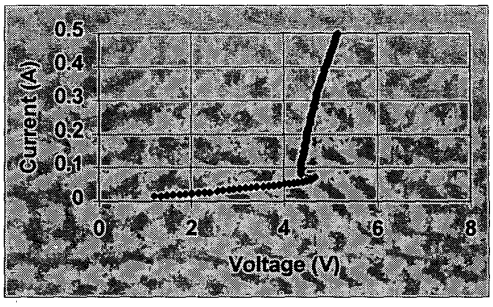

Figure 11: Pulse I-V curve for substrate trigger protection device for 1.8 V Vdd supply pin. The initial current after 1 V corresponds to the internal circuit turn on. Note that this I-V was not taken to failure.

VII. Chip Design Implementation

In the overall implementation of this protection design the ground connections and Vss bus resistance can play a critical role. It is usually assumed that every I/O pin is identical on a chip but this would not be the case if there are bus resistance effects as will be illustrated in this section.

In Figure 10 the protection device ground is shown as ESD Gnd and the output device ground is shown as Vss. The separate ground for the outputs is often required for noise isolation. Anti-parallel diodes are placed between the two grounds to form an effective path during stress. However, when the I/O pin is stressed with respect to Vss relatively more current can go through the output transistor because of the additional diode drop in series with the protection NMOS. In our technology with the differential Vt1 between the ESD NMOS and output NMOS this scheme is still effective without requiring any series resistor to the output. Data has shown that these silicided outputs can have > 4 kV HBM level without any series resistors that can compromise the VOL and VOH levels. Further, series resistors would require the output transistor to be made larger to overcome the performance degradation. Thus this substrate trigger concept has been used to achieve good ESD without impact on output design.

The ground bus resistance however did show a negative effect, especially for the fail-safe inputs. In Figure 12 the HBM levels on identical input pins are shown as a function of distance from the nearest Vss pin. This is shown for five different Vss pin locations and in each case the protection level dropped from about 5200 V next to the Vss pin (1 pad away) to just 2 kV beyond 4 pads away. It should be noted that the distribution of Vss, Vdd, Input, Ouptut, and I/O pads is a complex function of the chip layout and this particular product happened to have several inputs that were more than the critical 4 pads away.

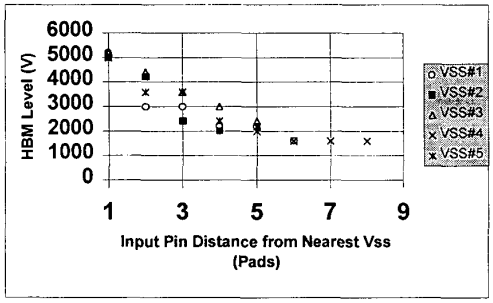

Figure 12: HBM ESD level as a function of distance from the nearest Vss pad for fail-safe inputs. Data for the five different Vss pad locations indicates degradation of ESD as function of distance from the Vss pin.

Although this bus resistance effect is very pronounced for the inputs with no diode to Vdd, the same effect was present for all the other types of pins. This is apparent in Figure 13 where the ESD level to Vss for each pin of the 144-Pin TQFP except for the power pins is shown. The Vss pin locations are indicated by vertical lines. It is clear that next to each Vss pin the ESD level is high and then goes through valleys in between the Vss pins. The effect is dramatic when the span between Vss pins is about 25. In Figure 13 Input 1 represents no diode to Vdd and Input 2 represents the presence of a small PMOS pull-up transistor. The Input 2 pins with a parasitic diode to Vdd as well as the I/O's and Outputs with a design diode to Vdd have relatively less drastic bus resistance effects compared to the pure inputs with no diode (Input 1). This is understood by the fact that the diode to Vdd takes part of the ESD current reducing the effect. Nevertheless, the bus resistance effect gives a very non-uniform distribution of ESD levels for identical pins of each group.

To understand the debiasing effects that could cause the protection levels to degrade, the overall layout of the protection devices and the buffer devices was examined. This is shown for one local area of the chip in Figure 14.

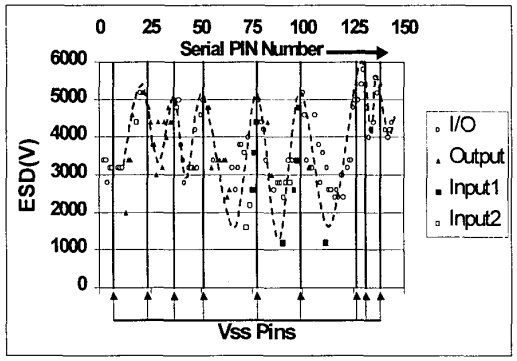

Figure 13: HBM ESD level for all Input, Output, and I/O pins. The locations of the Vss pins on the chip (144-TQFP) are as indicated. Note that Input 1 has no diode to Vdd and Input 2 has a small PMOS pull-up to Vdd. The variation of the ESD level correlating with the Vss pin location is obvious.

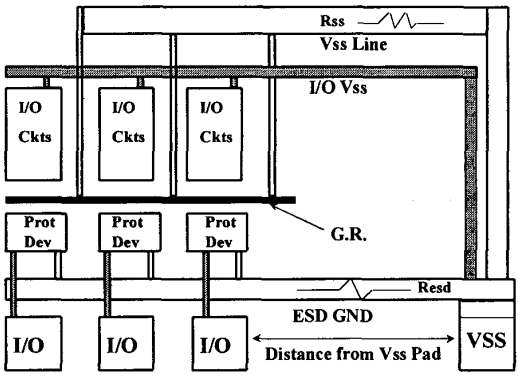

Figure 14: ASIC implementation of the product chip with the protection device and ground connections. Note that in this particular case the I/O buffer Vss is a separate line but is connected at the VSS pad.

The layout of any chip is invariably complex. In the example shown in Figure 14 the I/O circuits are connected to a different ground line from the

protection device ground line for flexibility and layout convenience. If an application requires noise immunity the output transistor ground line (I/O Vss) line is connected to a separate ground pad. In the example above, both are the same. Note also that the P+ latchup guardring (G.R.) has a separate metal bus of its own and is connected to a Vss line with resistance Rss.

The debiasing effects of Figure 12 and Figure 13 are due to the combined effect of the latchup guard ring resistance, Rss, and the ESD ground bus resistance, Resd, in Figure 14. This is determined by the distance from the nearest Vss pad. The equivalent schematic for this effect is represented in Figure 15. A new node VE is also represented in the figure.

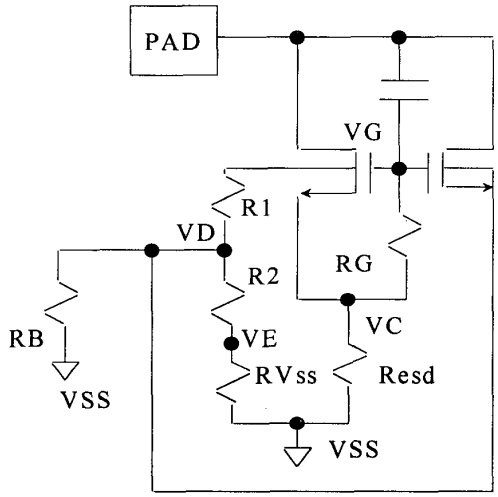

Figure 15: The schematic representation of the bus resistance effects in Figure 15. RB = 50 Ohms, R1 = 40 Ohms, R2 = 40 Ohms, and RVss and Resd vary depending on the pin location.

As shown in Figure 15, the protection device sees a bus resistance of Resd whereas the guardring sees the combination of R2 plus RVss in parallel with RB. When Resd is excessive, the substrate potential, which is effectively (VD – VC), can be reduced. To illustrate this effect simulations were performed for RVss = Resd at 0.01 Ohms and 5 Ohms. Case 1 with small Rvss and Resd is shown in Figure 16. It is clear from Figure 16 that when the bus resistance is negligible (VD-VC) approaches above 0.7 V at 300 ps for the device to uniformly turn on. The simulations for Case 2 with Rvss=Resd =5 Ohms are shown in Figure 17.

Because of the bus resistance, VPAD and VC do go high but the relative drain-source potential stays the same after the *npn* turn on. As a consequence of increase in VC, the potential (VD- VC) reduces. This is more clearly illustrated in Figure 18 where (VD-VC) is plotted for the different cases. Note that the substrate collapses for Case 2, which can cause the protection device level to be reduced or even fail

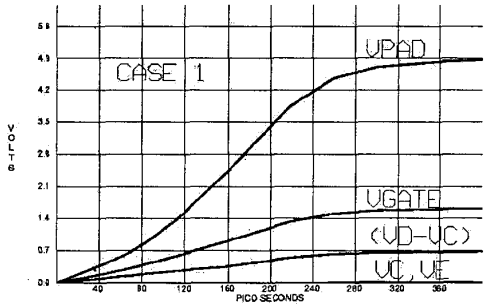

Figure 16: Case 1 simulation results with Rvss = Resd = 0.01 Ohms. The effective substrate bias is (VD-VC).

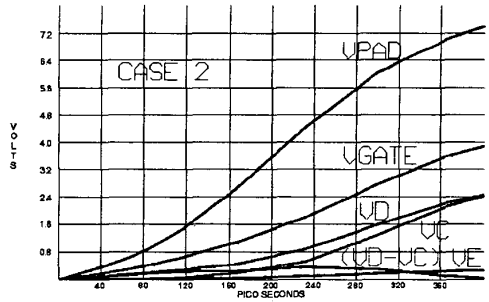

Figure 17: Case 2 simulation results with Rvss = Resd = 5 Ohms. Because of the bus resistance the absolute voltages at VPAD and VC go high but the drain to source voltage remains the same.

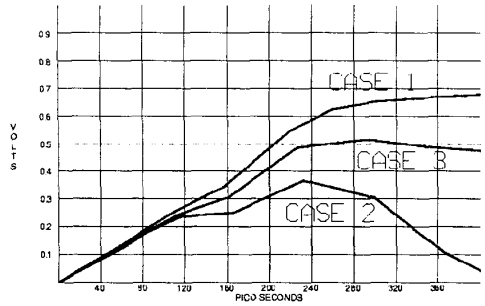

Figure 18: The effective substrate bias (VD-VC) for the three cases. The pump bias collapses for Case 2 but is restored with a design fix (see Figure 21) for Case 3.

below 2 kV. For case 2, the substrate bias starts to significantly drop off around 240 ps. The pulsed IV taken for input pin next to Vss and 4 pads away from Vss are compared in Figure 19. The on-resistance difference between the two indicates that with the debiasing effect only about one third of the protection device turned on. This correlates with the reduced protection level as indicated in Figure 12. Also note that at around 70 mA of drain current this effect begins to takes place and the simulations of Figure 18 indicated that for Case 2 at 240 ps the drain current (not shown) is about the same. Thus the debiasing effects of Figure 19 correlate with simulations.

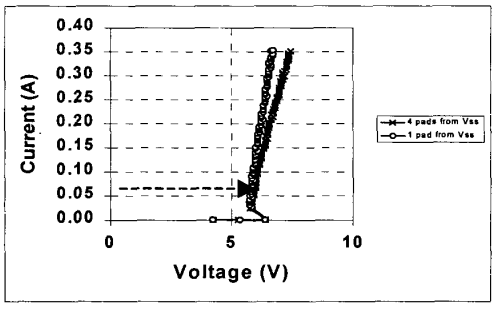

Figure 19: Pulsed IV showing the debiased effect on input 4 pads away from the Vss pad. Note at around 70 mA the protection device on-resistance increases indicating non-uniform turn-on of the *npn*.

A design fix to overcome this is to essentially short the nodes C and E in Figure15. This is shown as a layout metal strap in Figure 20 and is

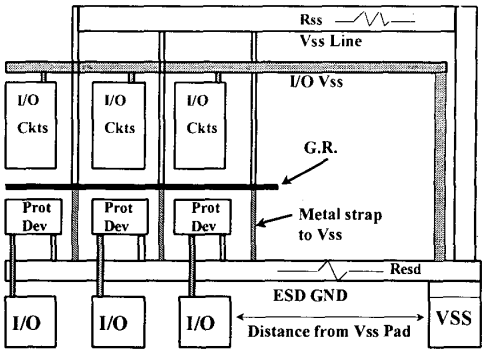

Figure 20: The debiasing effect can be eliminated by tieing the guardring to the ESD GND at every I/O location. This is schematically represented in Fig. 21.

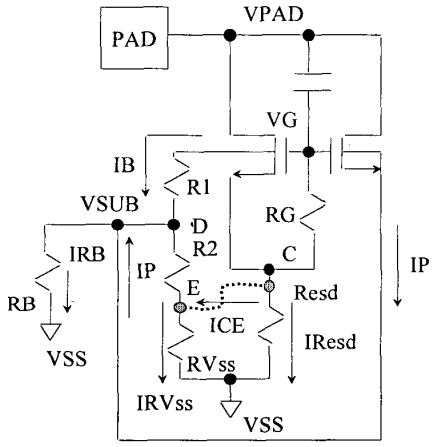

Figure 21: The metal strap shown in Figure 20 to eliminate the debiasing effect is schematically represented by the dotted line.

represented as the dotted line in the schematic of Figure 21. The simulation for this is shown as Case 3 in Figure 18 where it is seen that the collapse of the substrate pump is eliminated. With the strap, VE follows VC and in turn VD follows VE to maintain (VD – VC) which is the effective substrate bias. The metal strap shown also serves to reduce the effective ground resistance for the protection device. Actually, with the inclusion of the metal tie the *npn* current is split into IResd and ICE (see Figure 21). These current components are shown in Fig. 22. Thus the metal strap has to be made wide enough to handle a good portion of the ESD current.

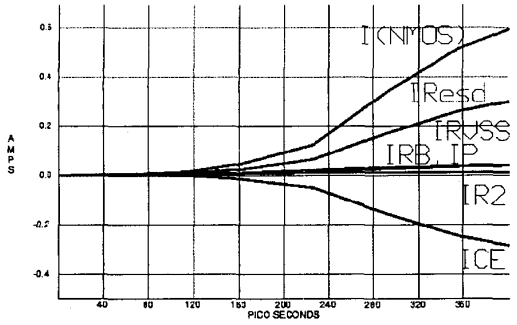

Figure 22: The simulated current waveforms with the metal tie shown in Figure 21. The protection drain-source current now splits into IResd and ICD, the current through the metal short.

Finally, the improvement to achieve consistent ESD performance is shown in Figure 23 after the metal tie fix was implemented. In contrast to the pre-fix data in Figure 12, the new results shown for inputs illustrate that the ESD level is 5 kV or above with only slight statistical variations and definitely independent of the location with respect to the Vss pad. All of the other types of pins also showed this same uniform behavior.

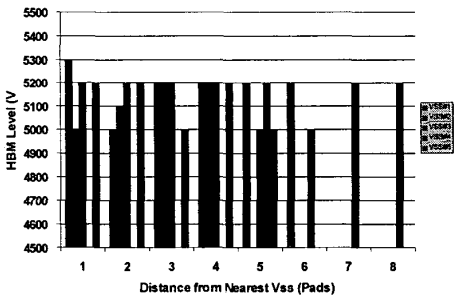

Figure 23: The input ESD level as a function of its location with respect to the Vss pad. Uniform protection level, independent of the effect in Figure 12, can be observed.

VIII. Product and Technology Implementation

With the layout and design approaches described in the previous section, this total scheme was effectively used in the ASIC back-plane for 0.5 μm to 0.2 μm technologies with both thin epi substrate and low- resistance non-epi substrate. This concept is applicable to any deep submicron technology.

The substrate pump design should take into consideration the substrate resistance for the technology. For example, our studies have shown that the required pump size can be as small as 25% for a non-epi 2 Ohm-cm substrate, 50% for a 6.5 μm epi substrates, or 75% for the 3.5 μm epi substrate technology. This sizing of the pump is easily tuned with different connections of the sources (Figure 2). The final successful implementation is of course coupled with both the substrate process and the layout effects as shown in this paper.

IX. Conclusions

This paper reported a novel NMOS substrate pump protection scheme that is very useful for advanced CMOS technologies with silicided diffusions and/or with thin epi substrates. Excellent ESD levels using this concept were demonstrated.

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