Adaptive Bandwidth DLLs and PLLs using Regulated Supply CMOS Buffers

Stefanos Sidiropoulos[1], Dean Liu[2], Jaeha Kim[2], Guyeon Wei[2], and Mark Horowitz[1,2]
[1]Rambus Inc and [2]Stanford University

ABSTRACT

A technique for designing DLLs and PLLs using CMOS buffers with a regulated supply is presented. By scaling the charge pump current and the output resistance of the regulating amplifier, the proposed loops achieve a wide bandwidth that tracks the operating frequency, a constant damping factor, large operating range and low noise sensitivity. Prototype loops designed in 0.35-μm CMOS processes exhibit >10× operating range and less than 1% input tracking jitter.

Introduction

Delay and Phase Locked Loops are integral components of contemporary digital and mixed signals ICs. Integrating these semi-analog blocks in the environment of a large IC requires dealing effectively with the unavoidable supply and substrate noise. To address this issue, designers usually employ differential delay elements combined with some form of high bandwidth biasing scheme [1], [2]. However, decreasing supply-to-threshold voltage ratios, have also led to the adoption of buffers based on variants of static CMOS gates with regulated supply which acts also as the control voltage [3]. The advantages of CMOS based delay buffers are their simple and portable design and their relaxed supply headroom requirements. Their main disadvantage, however, is their high control-voltage to delay gain; typically 1-% of delay per 1-% of regulated supply/control-voltage. This high gain does not directly affect the buffer noise sensitivity in a well regulated environment. However, in order to compensate for high gain, designers are forced to reduce the loop bandwidth - typically regulated supply PLLs and DLLs achieve loop bandwidths that are 1-2 orders of magnitude lower than their theoretical maximum (1/10th of the reference clock frequency). This low bandwidth results in loops with long acquisition times, high phase error accumulation, and limited operating range. This paper discusses techniques that eliminate these shortcomings. The proposed Delay and Phase Locked Loops exhibit wide bandwidth, low noise sensitivity, short acquisition times, and large operating range.

Delay Element Design

Conventional regulated-supply voltage-controlled delay lines and oscillators (VCDLs/VCOs) comprise a cascade of buffers with their supply voltage connected to V_{DD} through a high impedance element. Typical designs employ a cascoded current source or a linear second order integrating regulator [3], [4]. The "virtual-supply" node (V_C) is heavily coupled to V_{SS} in order to isolate V_{DD} variations and make V_{SS} noise transparent to the delay buffers. Thus, conventional designs exhibit an unavoidable trade-off between increased noise rejection and regulator bandwidth. Maximizing noise rejection by decreasing the frequency of the pole formed on node V_C also means that the overall loop bandwidth has to be compromised. To ensure stability the loop main pole(s) have to be set well below the regulator bandwidth. In contrast the proposed design uses a single-pole regulating amplifier to regulate the virtual-supply without compromising either noise rejection or the overall loop bandwidth.

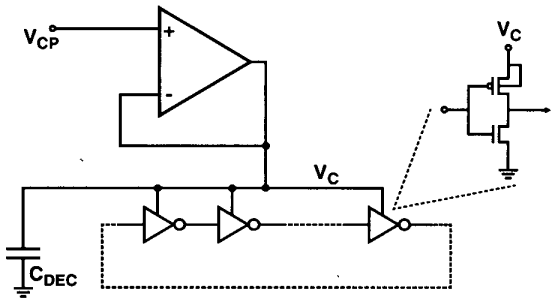


Figure 1: VCDL and VCO design

Figure 1 illustrates the VCDL/VCO design. The control voltage V_{CP} drives a simple regulating amplifier which generates the delay element virtual supply (V_C). The delay element design is not limited to inverters - any CMOS gate or differential element whose delay changes with variations on its supply can be used for that purpose. The delay T_D of these buffers is proportional to their output time constant, i.e: $T_D \propto R_{ON} \cdot C_{LD}$, where C_{LD} is the load capacitance of the delay buffer and R_{ON} is the "on resistance" of a linear MOSFET:

$$R_{ON} = 1/|\beta \cdot (V_C - V_T)| \propto 1/g_{mBUFF} \quad (1)$$

where β is the process transconductance, V_T the device threshold, and g_{mBUFF} the transconductance of a device biased at V_C. The VCDL and VCO gain is then given by:

$$K_{DL} \propto C_{LD}/|\beta \cdot (V_C - V_T)^2| \quad (2)$$

$$K_V \propto \beta/C_{LD} \quad (3)$$

The regulating amplifier, depicted in Figure 2, is a two stage current mirror based design. Since the inter-stage mirroring ratio R_M is kept low, the amplifier is virtually a single pole system and does not require stabilizing compensation. The differential pair bias current is set by a current mirror driven by the loop control voltage V_{CP}. The transconductance of the amplifier in unity gain configuration is simply $g_{mOP} = R_M \cdot g_{mIN}$. Since g_{mIN} tracks g_{mBUFF}, the bandwidth of the regulating loop g_{mOP}/C_{DEC} tracks the operating frequency and does not compromise the enclosing PLL/DLL stability even with variations in process and operating environment. The current dissipated by the amplifier also scales with operating frequency. To minimize the offset between V_{CP} and V_C and maintain high saturation margins in the amplifier, the amplifier current is set to be 2-3 times larger than the current consumed by the VCDL/VCO delay elements. The remaining small offset does not affect the DLL/PLL operation since the regulating loop is enclosed within the larger phase or delay locked loop.

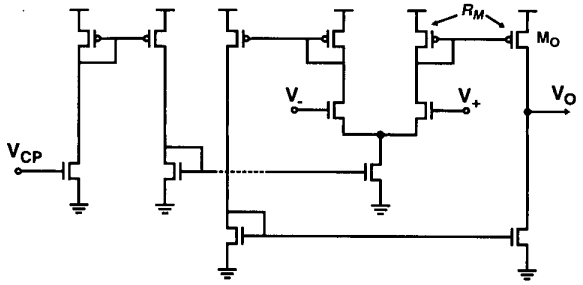


Figure 2: Regulating amplifier

As long as the amplifier output PFET M_O remains saturated, the static supply rejection of the design is dictated by the regulating amplifier open loop gain. The dynamic supply rejection is determined by the low-pass filter formed by the output impedance of M_O and the total capacitance on node V_C. The regulating loop attenuates supply steps by more than a factor of 15 achieving a worst case supply sensitivity of less than 0.06%-delay/1%-supply. The maximum operating frequency of

 0-7803-6309-4/00/$10.00 © 2000 IEEE

the VCDL or VCO is determined by the "virtual supply" voltage needed to run the delay buffers at the required clock period, plus the voltage headroom required to keep M_O in the saturation region.

DLL Design

A common property among regulated-supply and current starved delay buffer designs is that their delay range is very broad. However, as Equation (2) indicates, this broad delay range comes at the expense of a non-linearly varying delay gain over the operating frequency range. This property causes DLLs employing this type of buffers to either have a very narrow range or increased jitter. Consider a conventional charge pump DLL with a single pole (ω_P) transfer function:

$$H(s) = \frac{1}{1 + s/\omega_P} = \frac{1}{1 + s \cdot C_{CP}/(I_{CP} \cdot K_{DL} \cdot F_{REF})} \quad (4)$$

where C_{CP} and I_{CP} are the charge pump capacitor and current respectively, K_{DL} the delay line gain and F_{REF} the operating frequency. Increasing K_{DL} means that the ratio ω_P/ω_{REF} increases with decreasing F_{REF}. This effect undermines the loop stability and limits the DLL operating range. Even when a broad operating range is not a requirement, minimizing the DLL's steady state ripple requires that the I_{CP}/C_{CP} ratio must be set to an appropriately low value considering the highest delay gain K_{DL} (usually at the slowest process and temperature at a particular F_{REF}). To eliminate this problem we can linearize the loop gain by adopting a technique similar to the differential buffer self-biasing proposed in [2]. If the DLL charge pump current is set by V_{CP} through the same scheme used in the regulating amplifier, the resulting charge pump current will be given by:

$$I_{CP} = sc_{cp} \cdot \beta \cdot (V_C - V_T)^2 \quad (5)$$

where sc_{cp} is the scaling factor in the charge pump bias current mirror. By combining Equations (2), (4) and (5) we obtain:

$$\omega_P \propto sc_{cp} \cdot F_{REF} \cdot C_{LD}/C_{CP} \quad (6)$$

Equation (6) shows that the process and environmental condition dependent terms (V_T, β) cancel, and the loop bandwidth tracks the operating frequency. The ratio of ω_P to F_{REF} is determined by a well controlled scaling factor sc_{cp} and the ratio of C_{LD} to C_{CP}. Since C_{LD} and C_{CP} consist predominantly of gate capacitance their ratio tracks very well over process resulting in predictable loop characteristics.

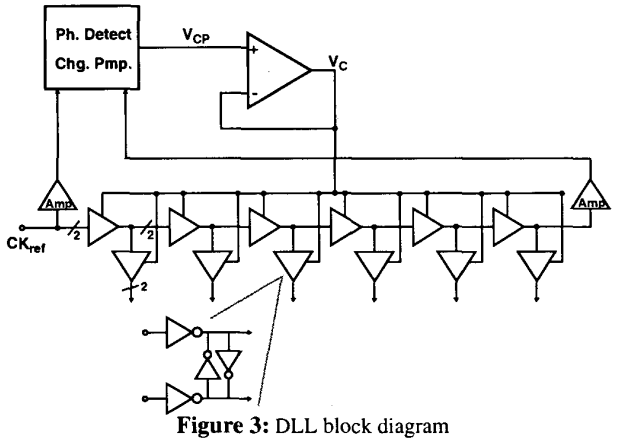


Figure 3: DLL block diagram

The proposed design technique has been applied in a DLL integrated in the parallel I/O transceiver discussed in [5]. The DLL implements the dual-interpolating architecture proposed in [6]. The core loop, shown in Figure 3, consists of a regulated-supply delay line comprising six pseudo-differential delay elements, the regulating amplifier of Figure 2, a self-biased charge pump, and a linear phase detector. The

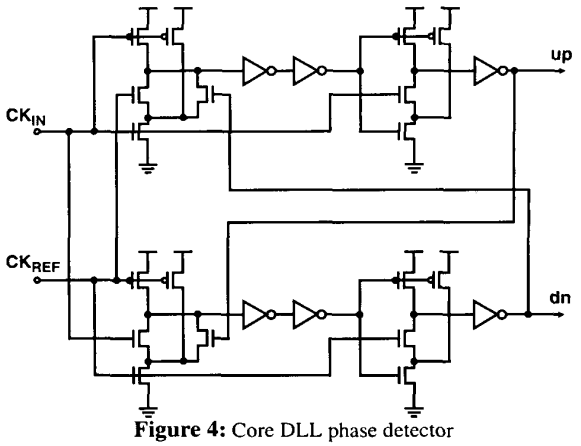


Figure 4: Core DLL phase detector

six pseudo-differential outputs span 180° and drive the interpolating peripheral loop which generate the I/O interface clocks, under the control of a receiver-replica phase detector and a Finite State Machine. To minimize the transceiver's power dissipation and achieve output clock dither jitter that is constant in degrees, the peripheral loop and the rest of the transceiver are powered by a switched power supply that replicates the core DLL's control voltage V_{CP}.

Although the analysis above assumes a linear DLL, the proposed technique can be also applied to a "bang-bang" type DLL. In the latter type of design, scaling the charge pump current with V_{CP} results in a DLL whose dither jitter is a constant fraction of the reference clock period. However, since typical designs strive to minimize dither jitter by decreasing the I_{CP}/C_{CP} ratio, a "bang-bang" DLL will usually exhibit a lower "bandwidth" than its linear counterpart. For that reason the prototype DLL uses the linear phase detector shown in Figure 4. This precharged design is a Phase-Only-Detector which, similarly to a state machine Phase-Frequency-Detector (PFD), outputs two overlapping pulses of equal duration when the input phase error approaches zero. The absence of extra states eliminates loop start-up problems, while (unlike the phase-only detector proposed in [6]) the resulting steady state ripple and offset are minimized without impacting ω_P. To eliminate the deadband of the original precharged design in [7], extra delay is inserted between the master and slave stages and the intermediate nodes of the NFET stack are precharged.

PLL Design

Conventional PLLs (Figure 5), lock the phase of the output clock of their voltage-controlled oscillator to the phase of the incoming reference clock. This is accomplished under the feedback provided by combination of the loop PFD, charge pump, and filter. Since, the loop transfer function contains two poles at the origin (one from the filter integrator and one from the VCO), a zero is required to stabilize the loop. This zero is commonly implemented by using a resistor in the loop filter. A higher order pole is usually employed to filter the high

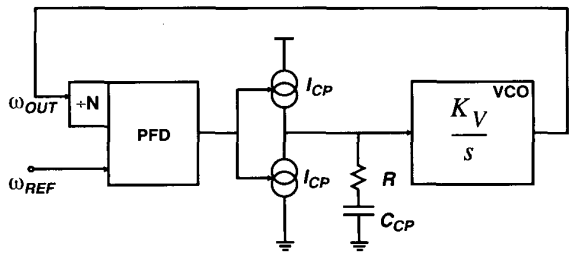


Figure 5: Conventional PLL block diagram

frequency phase noise resulting from the resistor charge-pump combination. The closed-loop transfer function of the conventional PLL can be shown to be [8]:

$$H(s) = N \cdot \frac{1 + 2 \cdot \zeta \cdot s/\omega_B}{1 + 2 \cdot \zeta \cdot s/\omega_B + (s/\omega_B)^2} \quad (7)$$

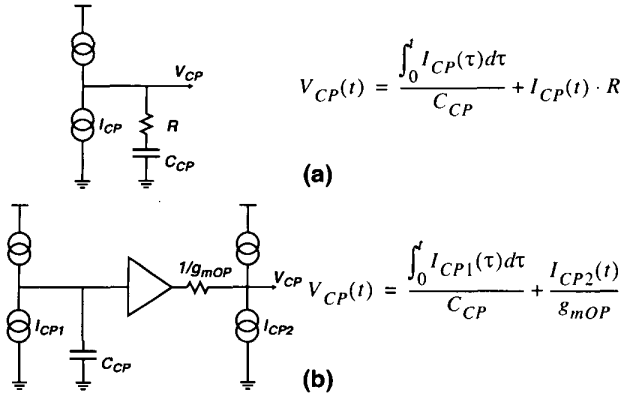
where the loop damping factor ζ and bandwidth ω_B are given by:

$$\zeta = 0.5 \cdot R \cdot \sqrt{I_{CP} \cdot K_V \cdot C_{CP}/N} \quad \text{and} \quad \omega_B = 2 \cdot \zeta/(R \cdot C_{CP}) \quad (8)$$

Achieving a non-overly uderdamped loop response requires ζ larger than 0.7, while minimizing phase error accumulation requires maximizing the loop bandwidth ω_B. Both of these goals are difficult to achieve under varying process, environmental conditions and loop multiplication factor N. PLL designs have to first satisfy stability constraints under worst operating conditions. As a result conventional PLLs achieve relatively low bandwidths and accumulate phase error for a large number of cycles. Regulated supply delay elements exhibit a static supply sensitivity which is typically 2-3 times larger than the sensitivity of their differential counterparts (although their dynamic supply rejection is usually better). This property combined with a low PLL bandwidth results in relatively poor tracking jitter performance, albeit acceptable cycle-to-cycle jitter for microprocessor applications [3]. Attempting to maximize the loop bandwidth by varying I_{CP} alone (as was done in the proposed DLL), would compromises the loop stability by overly reducing ζ at lower frequencies. What is needed instead is to vary both I_{CP} and R such that $R \cdot \sqrt{I_{CP}}$ remains constant over the operating frequency range. According to Equation (5) this requirement is satisfied if $R \propto 1/\beta \cdot (V_C - V_T)$. The output impedance of the regulating amplifier conveniently exhibits this property:

$$R_{OP} = 1/g_{mOP} = 1/(sc_{OP} \cdot g_{mBUFF}) \quad (9)$$

Furthermore, if the loop's stabilizing resistor is formed by the output impedance of the VCO regulating amplifier, ω_B will track $F_{REF} = g_{mBUFF}/(2 \cdot n \cdot C_{LD} \cdot N)$ (where n is the number of VCO buffers). Implementing a PLL stabilizing resistor through active components has been originally proposed in [9] and adopted by the self-biased differential PLL in [2]. As illustrated in Figure 6-(a) the



$$V_{CP}(t) = \frac{\int_0^t I_{CP}(\tau)d\tau}{C_{CP}} + I_{CP}(t) \cdot R$$

$$V_{CP}(t) = \frac{\int_0^t I_{CP1}(\tau)d\tau}{C_{CP}} + \frac{I_{CP2}(t)}{g_{mOP}}$$

Figure 6: Implementing the PLL stabilizing zero

control voltage of a conventional PLL at any point in time is determined by the aggregate charge stored on the loop capacitor plus the instantaneous voltage across the filter resistor. This configuration is equivalent to the one depicted in Figure 6-(b) where the integral voltage across C_{CP} is first buffered by the unity gain amplifier and then augmented by the instantaneous voltage formed by the second charge pump and the amplifier output impedance.

Figure 7 illustrates the proposed PLL. The VCO consists of five

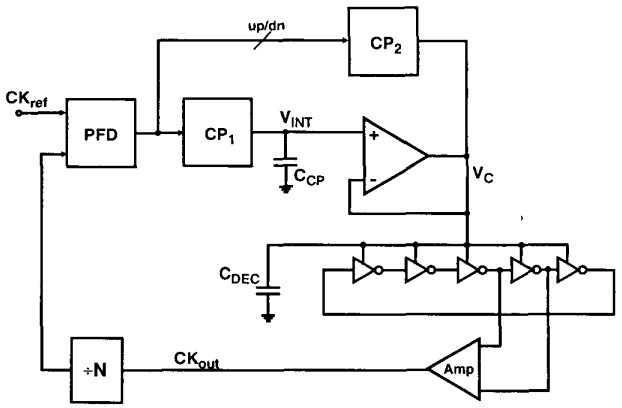


Figure 7: PLL block diagram

inverters whose "virtual supply" is regulated by the amplifier of Figure 2. The VCO output clock is converted to full CMOS levels by a simple two stage current-mirror based amplifier. The clock feedback path consists of a 2-8 programmable divider whose output drives the loop PFD. The output of the phase detector drives two charge pumps. The first "integral" charge pump CP_1 generates the loop integral control voltage V_{INT}. This voltage is then buffered by the regulating amplifier whose output is shunted with the output of the second "proportional" charge pump CP_2 to form the VCO control voltage V_C. The PLL higher order pole is determined by the "virtual supply" capacitance C_{DEC} and the amplifier output impedance and tracks the operating frequency as well. By combining Equations (3), (5), (8), (9) we can show that the loop has the same properties as a differential self-biased PLL:

$$\omega_B \propto n \cdot F_{REF} \cdot \sqrt{sc_{CP} \cdot N \cdot \frac{C_{LD}}{C_{CP}}}, \quad \zeta \propto \frac{1}{sc_{OP}} \cdot \sqrt{\frac{sc_{CP}}{N} \cdot \frac{C_{CP}}{C_{LD}}} \quad (10)$$

A side benefit of the loop configuration of Figure 7 is that I_{CP1} and I_{CP2} can be scaled independently to compensate for varying frequency multiplication factor N, thus enabling the loop to always achieve close to optimal characteristics. Figure 8 shows the charge pump that was used in the prototype PLL to take advantage of this fact. The charge pump is biased through a current mirror based DAC whose bias is established by the loop integral control voltage V_{INT}. In the prototype PLL the bias DAC control words are externally configurable to allow testing flexibility. In a production-grade PLL the two charge pump control words can be generated by a lookup table driven by N. The 3-2 predriver circuit is also optimized such that the charge pump output currents overlap over varying conditions to minimize period jitter.

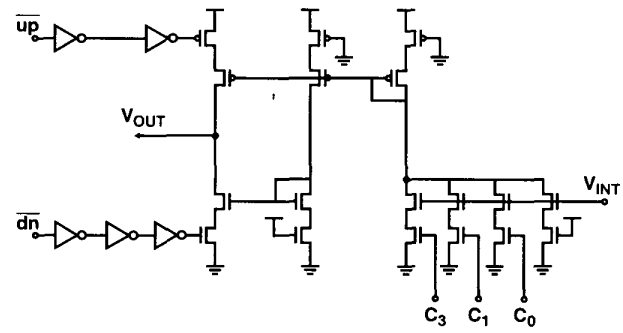


Figure 8: Charge pump schematic

0-7803-6309-4/00/$10.00 © 2000 IEEE

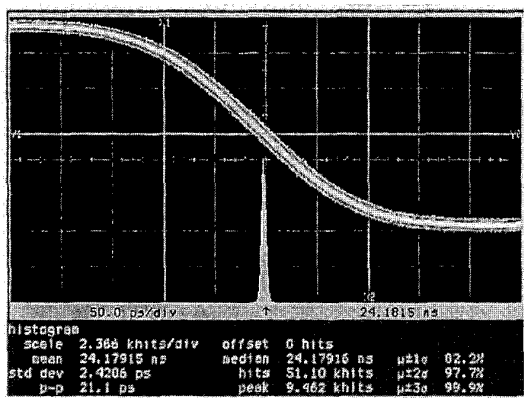


Figure 9: DLL core loop jitter

Results

Both the DLL and PLL have been designed in CMOS processes offered by MOSIS. The DLL has been fabricated along with the transceiver chip described in [5] in the 0.35-μm HP CMOS10 process. The DLL core loop operates from 33-500 MHz, while the peripheral loop operating range was more narrow 100-500 MHz (limited by the input receiver design). Figure 9 shows the loop jitter (22-ps pk-pk) while operating at 400-MHz with an active transceiver core. Table I summarizes the measured DLL characteristics.

The proposed PLL has been designed for the MOSIS/TSMC 0.35-μm process and is currently being fabricated. Simulation results (performed with backannotated netlists) indicate that the operating range is 20-600 MHz. Figure 10 shows the simulated acquisition and noise response while the PLL is operating at 500-MHz with N=2 (PFD input offset, output cycle time and output clock duty cycle are plotted). After the control voltage V_{INT} is reset to a V_T drop below the supply the loop acquires lock within 100 cycles. A 10% supply bump with 1-ns rise time applied at 400-ns, results in negligible cycle-to-cycle jitter (20-ps peak) and small input tracking peak jitter (75-ps). Table II summarizes the simulated PLL performance.

Conclusion

A technique for designing adaptive-bandwidth DLLs and PLLs using regulated supply delay buffers has been proposed. The loops designed in 0.35-μm CMOS processes achieve high bandwidth, and scalable power. In addition their noise performance is comparable to that of differential buffer based loops.

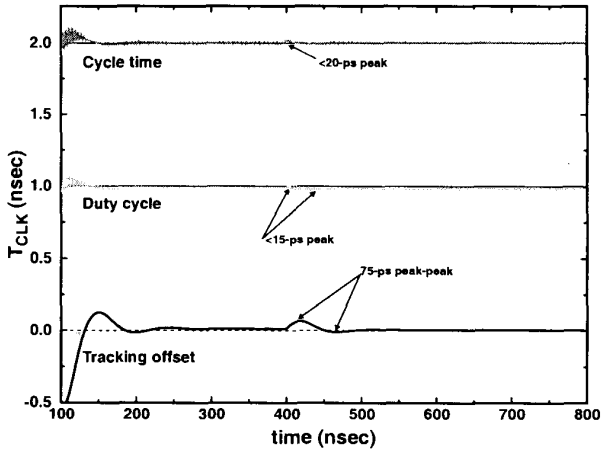


Figure 10: Simulated PLL acquisition and noise response

Operating Range	33-500 MHz
Active Area	0.035 mm^2
Phase Offset	<20-ps
Core-loop Jitter	22-ps peak
Dual-loop Jitter	45-ps peak
Power Dissipation	37-mW (core) @3.3-V
	19-mW (peripheral) @3.3-V
Technology	0.35-μm HP/CMOS10B

Table I: DLL performance summary (@400-MHz)

Operating Range	30-650 MHz
Active Area	0.047 mm^2
Phase Offset	<15-ps
Tracking jitter	<80-ps peak (10% Vdd noise)
Period jitter	<20-ps peak (10% Vdd noise)
Power Dissipation	21.5-mW @3.3-V
Technology	0.35-μm TSMC/CMOS

Table II: PLL performance summary (@500-MHz)

Acknowledgments

The authors want to thank Ken Chang, Pak Chau, Jun Kim, and Jared Zerbe for helpful comments.

References

[1] I. Young *et. al.* "A PLL clock generator with 5-110 MHz lock range for microprocessors," *IEEE JSSC*, vol. 28, no. 12, Dec. 1993.

[2] J. Maneatis, "Low-jitter process independent DLL and PLL based on self-biased techniques," *IEEE JSSC*, vol. 31, no. 11, Nov. 1996.

[3] V. vonKaenel et. al. "A 320 MHz CMOS PLL for microprocessor clock generation," *IEEE JSSC*, vol. 31, no. 11, Nov. 1996.

[4] S. Kuge et. al. "A 0.18 μm 256Mb DDR-SDRAM with low-cost post-mold-tuning method for DLL replica," in *Dig. Tech. Papers ISSCC 2000.*

[5] G. Wei *et. al.* "A variable frequency parallel I/O interface with adaptive power supply regulation," in *Dig. Tech. Papers ISSCC 2000.*

[6] S. Sidiropoulos, M. Horowitz, "A semi-digital dual DLL," *IEEE JSSC*, vol. 32, no. 11, Nov. 1997.

[7] H. Notani, "A 622-MHz CMOS PLL with precharge-type phase frequency detector," *in Dig. Tech. Papers, VLSI Symposium* 1994.

[8] F. Gardner, "Charge-pump phase-locked loops", *IEEE Trans. Come.*, vol. 28, no. 11, Nov. 1980.

[9] I. Novoff et. al. "Fully integrated CMOS PLL with 15-240 MHz range", *IEEE JSSC* vol. 30, no. 11, Nov. 1995.