

WA 17.3 Asynchronous Interlocked Pipelined CMOS Circuits Operating at 3.3-4.5GHz

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Chip performance, power, noise, and clock synchronization are becoming formidable challenges as microprocessor performance moves into the GHz regime and beyond. Interlocked pipelined CMOS (IPCMOS), an asynchronous clocking technique, helps address these challenges. Figure 17.3.1 shows how a typical block (e.g., Block D) is interlocked with all the blocks with which it interacts. In the forward direction, dedicated Valid signals emulate the worst-case path through each driving block and thus determine when data can be latched within the typical block. In the reverse direction, Acknowledge signals indicate that data has been received by the subsequent blocks and that new data may be processed within the typical block. In this interlocked approach local clocks are generated only when there is an operation to perform.

Measured results on an experimental chip demonstrate robust operation for IPCMOS at 3.3GHz under typical conditions and 4.5GHz under best-case conditions in a 0.18µm 1.5V CMOS technology. The block diagram of Figure 17.3.2 shows the core of what is implemented. The logic between the latches consists of two stages of a worst-case path through the 3to2 compressor tree of a 64b floating-point multiplier with a total of ten of these stages included in the path. The asynchronous handshaking local clock circuits are each loaded with 40 latches to simulate practical loading. Since the locally-generated clocks for each stage are active only when the data to a given stage is valid, power is conserved when the logic blocks are idling. Furthermore, with the simplified clock environment it is possible to design a simple single-stage latch that can capture and launch data simultaneously without the danger of a race.

The general concepts of interlocking, pipelining and asynchronous self-timing are not new and have been proposed in a variety of forms [1-3]. However, the techniques used in those approaches are too slow, especially for macros which receive data from many separate logic blocks. IPCMOS achieves high-speed interlocking by combining the function of a static NOR and an input switch to perform a unique cycle dependent AND function as exemplified by the strobe circuit diagrams of Figure 17.3.3a and b. Every local clock circuit in Figure 17.3.2 has a strobe circuit which implements the asynchronous interlocking between stages.

The operation of the strobe circuit can be understood by starting at the end of a cycle when the external valid signals (VALID₁, VALID₂) and CLK_R which is generated from the acknowledge signals (ACK) are low, the switches are open, and the internal valid signals (Vint₁, Vint₂) and Rint are high. The strobe outputs, CLKE and ACK, which are high and low, respectively, transition to low and high, respectively, only when all of the internal valid signals (Vint₁, Vint₂) and Rint go low. For this to happen, each external valid signal must first be reset high, thereby turning on its associated switch. Next, each of the valid inputs transitions low, as data for that input becomes valid. This causes the associated internal valid signal to also go low. The strobe circuit outputs ACK and CLKE will transition high and low, respectively, when the last of the external valid signals makes its downward transition and CLK_R has gone high. When this occurs all the internal valid signals and Rint will be low. ACK transitioning high turns each Switch off, since all the external valid signals are low at this time. ACK is also the handshaking signal, to the transmitting blocks that data is received, and they can send more data. Immediately after ACK turns the Switch off, CLKE precharges each of the internal valid nodes (Vint) and Rint high.

This in turn causes ACK to go low and CLKE high. In the Strobe circuit, the p-channel load device of the static NOR is connected to only one internal Valid signal. The Valid signal to which the load is connected should be the nominally last arriving. However, in actual operation if another signal arrives last, the circuit functions normally but with some additional power dissipation.

The unique way the Strobe circuit ANDs the valid inputs and at the same time keeps track of the cycle in which they occur is seen in the wave forms of Figure 17.3.4 for a circuit with three valid signals. Initially all the external valid signals are high. They all transition low and the Strobe circuit generates a low CLKE pulse output. Subsequently, a strobe output is generated only after all 3 valid inputs have transitioned low to high to low. Thus the Strobe circuit keeps track of the cycle that each input occurs in by not generating an output until all the inputs have transitioned from a low to a high and back to a low.

Measured local clock signals running at 4.5GHz are shown in the picoprobe waveforms of Figure 17.3.5. The way the interlocking automatically compensates for delay variations, which result from power supply noise, across chip line width variations, and parameter variations, is also seen in the wave forms when the data valid input of local clock stage 2 is intentionally delayed for a period of time by the externally generated Valid Inhibit signal going high. Because of the handshaking, the local clocks for all the stages before and after stage 2 is also delayed as shown in the wave forms, until Valid Inhibit goes low again and all the stages resume their normal mode of operation with no loss of data.

A significant power reduction results when there is no operation to perform and the local clocks turn off. This is similar to what happens in the wave forms of Figure 17.3.5 when the data valid signal of clock stage 2 is intentionally inhibited. The wave forms also show that the clock transitions are staggered in time, reducing the peak di/dt and therefore noise compared to a conventional approach with a single global clock.

The IPCMOS circuits show robust operation with large variations in power supply voltage, operating temperature, threshold voltage, and channel length. One example of this is given in Figure 17.3.6, where a plot of measured frequency versus I_{eff} for both normal and low threshold devices are given. This data again demonstrates the ability of IPCMOS to operate at extremely high frequencies, while realizing the power and noise reduction of an interlocked asynchronous approach.

References:

- [1] Sutherland, L., "Micropipelines" Communications of the ACM, v 32, # 6, June 1989.
- [2] Mead and Conway, "Introduction To VLSI Systems" Addison-Wesley Publishing Company Inc., 1980, Chapter 7.

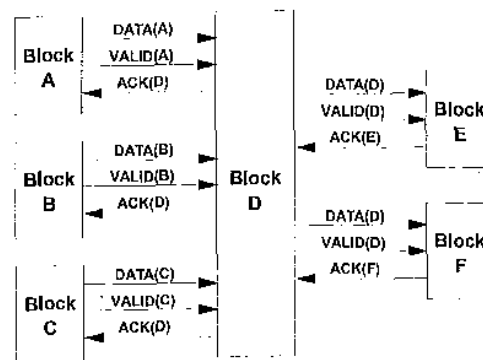


Figure 17.3.1: Interlocking at block level.

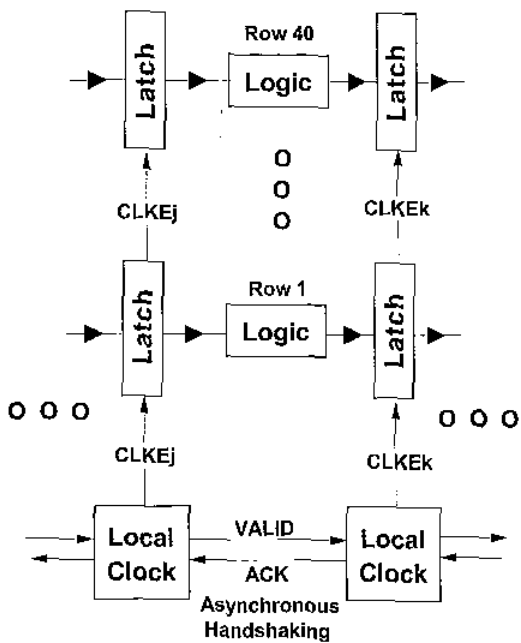


Figure 17.3.2: Multiplier core with local clocks.

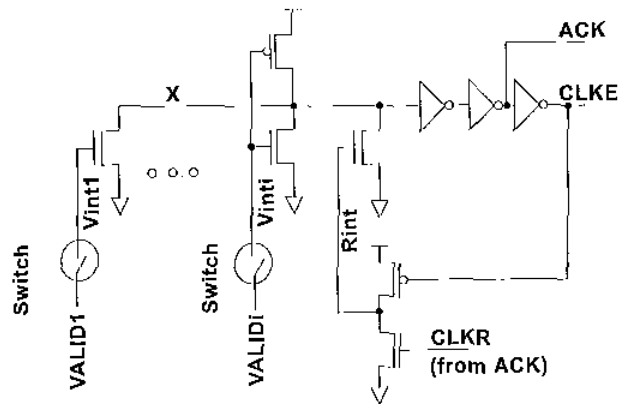


Figure 17.3.3a: Local clock strobe circuit.

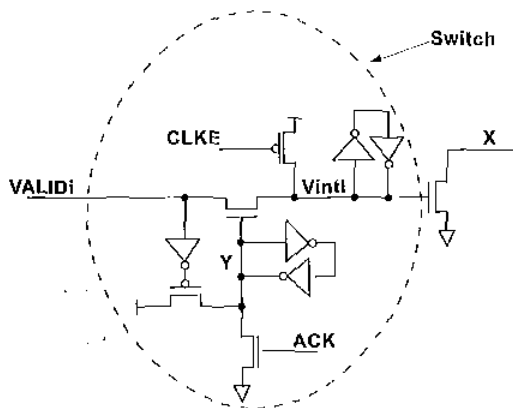


Figure 17.3.3b: Strobe circuit switch.

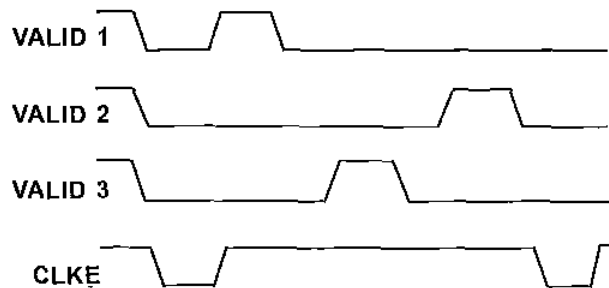


Figure 17.3.4: Strobe circuit unique “AND” function.

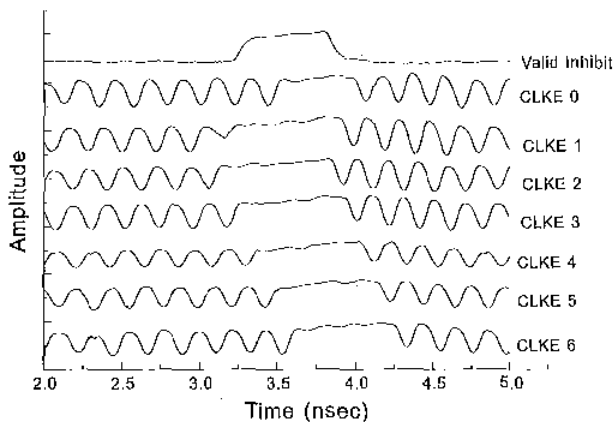


Figure 17.3.5: Measured local clock waveforms at 4.5GHz.

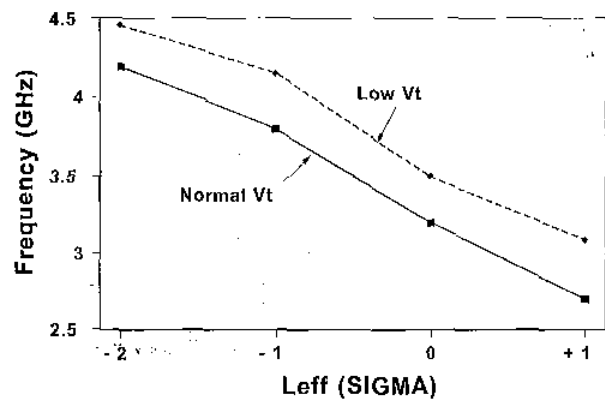


Figure 17.3.6: Frequency vs. channel length.