

A 390-mm², 16-Bank, 1-Gb DDR SDRAM with Hybrid Bitline Architecture

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Abstract— A 390-mm², 16-bank, 1-Gb, double-data-rate (DDR) synchronous dynamic random access memory (DRAM) (SDRAM) has been fabricated in fully planarized 0.175- μm , 8F² trench cell technology. The 1-Gb SDRAM employs a hybrid bitline architecture with 512 cells/local-bitline (LBL). Four LBL pairs are connected through multiplexers to each sense amplifier (SA). Two of the LBL pairs are coupled to the SA by wiring over two other LBL pairs using hierarchical bitlines. This results in a reduction of the number of the SA's to 1/4, reducing the chip size by 6%. A hierarchical column-select-line scheme is incorporated with a hierarchical dataline (MDQ) architecture. This makes 16-bank organization possible while sharing hierarchical column decoders and second sense amplifiers. A hierarchical 8-b prefetch scheme employs four MDQ's for each read-write drive (RWD) and two RWD's for each DQ. This reduces the frequencies of the MDQ's and the RWD's to 1/8 and 1/2, respectively. A 1-V swing signaling on the RWD is used to reduce the burst current by 18 mA. The 1-V swing signaling is successfully converted to 2.1 V with self-timed first-in, first-out circuitry. The hardware data demonstrate 400-Mb/s/pin operation with a 16-mm TSOP-II package. Seamless burst operation at various frequencies has also been confirmed. These features result in a 1.6-Gb/s data rate for $\times 32$ 200-MHz DDR operation with a cell/chip area efficiency of 67.5%.

Index Terms— Double-data-rate (DDR), dynamic random access memory (DRAM), hierarchical column-select-line (CSL), hybrid bitline, low voltage, 1 Gb, prefetch, synchronous DRAM.

I. INTRODUCTION

THE EVOLUTION of submicrometer CMOS technology [1] has steadily improved microprocessor speed. Quadrupling every three years, it has realized product chips with clock frequencies over 500 MHz [2]–[4] and even an experimental chip with a 1-GHz clock frequency [5]. It is highly desirable to have dynamic random access memories (DRAM's) not only with high density [6] but also with high performance.

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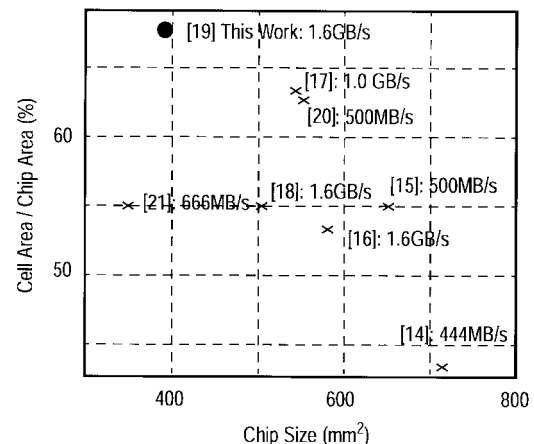


Fig. 1. Summary of the 1-Gb SDRAM's.

Synchronous DRAM's (SDRAM's) employed a three-stage-pipeline architecture [7] and 2-b prefetch architecture [8] for the consecutive column burst operation with an internal burst address counter, improving the data rate up to 125 Mb/s/pin for the 16-Mb generation. The 64-Mb SDRAM [9] introduced an address incremented pipeline scheme, realizing up to 150 Mb/s/pin. The 256-Mb SDRAM's [10], [11] employed a wave-pipeline scheme with first-in/first-out (FIFO) circuitry, boosting the data rate to approximately 250 Mb/s/pin.

In a revolutionary step, the 72-Mb Rambus DRAM (RDRAM) [12] employed 8-b prefetch and a protocol-based design with Rambus-signaling-level (RSL) interfaces, realizing up to 800 Mb/s/pin with $\times 16$ DQ's, resulting in 1.6-Gb/s. The experimental 72-Mb synchronous-link DRAM (SLDRAM) [13] used a similar protocol-based design but also introduced source-synchronous buses and DQ calibration to overcome the DQ skewing problem in a different manner from the RDRAM RSL approach. This resulted in 400 Mb/s/pin. Although these RDRAM's [12] and SLDRAM's [13] can effectively improve the DRAM data rate at the system level, the chips exhibit less than 50% cell/chip area efficiency and are at least 10% larger than conventional SDRAM's with 60% cell/chip efficiency. Hence, the SDRAM approach would be the more cost-effective solution if it could achieve high performance.

Fig. 1 summarizes the 1-Gb SDRAM's [14]–[21]. It shows the chip size, the cell/chip area efficiency, and the chip

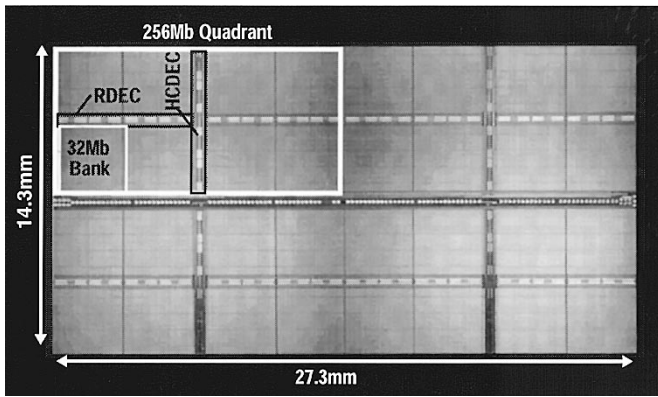


Fig. 2. Microphotograph of the 1-Gb DDR SDRAM.

maximum bandwidth (data-rate/pin \times the number of the DQ's). From the first report of the 1-Gb SDRAM's [14] in 1995, the 1-Gb DRAM chip size was reduced from approximately 700 mm² [14] to 500 mm² [18] in three years. This results in a chip size reduction of 70 mm² per year. The cell/chip area efficiencies vary, but the average is about 60%. With this cell/chip area efficiency of 60%, the expected 1-Gb SDRAM chip size with 0.175- μ m, 8F² cell technology is 440 mm². The maximum bandwidth previously realized was 1.6 Gb/s [16], [18] with 200 Mb/s/pin for $\times 64$ DQ's. However, these chips' cell efficiencies were less than 55%, and therefore were not a cost-effective solution.

This paper describes a 390-mm², 16-bank, 1-Gb, double-data-rate (DDR) SDRAM [19] with 0.175- μ m trench cell technology [1]. The chip employs an RDRAM-like 8-b prefetch [12] and an SLDRAM-like source-synchronous bus [13], realizing 400 Mb/s/pin with a 16-mm TSOP-II module. This results in 1.6 Gb/s with $\times 32$ DQ's, similar to RDRAM performance [12] for the 1-Gb generation. Cell/chip area efficiency of 67.5% has been realized.

Section II gives an overview of the chip. Section III discusses key design attributes, including:

- a) hybrid bitline architecture;
- b) hierarchical column-select-line (CSL) scheme;
- c) hierarchical 8-b prefetch;
- d) 1-V swing read-write-drive (RWD) signaling.

Section IV shows hardware results. The paper's conclusion is stated in Section V.

II. CHIP OVERVIEW

Fig. 2 shows a microphotograph of the 1-Gb DDR SDRAM [19]. The 390-mm² chip size is 27.3 mm \times 14.3 mm, allowing it to fit in the existing 16-mm TSOP-II package used for the 256-Mb DRAM [22]. The chip is powered from a 2.5-V external supply, which is regulated internally to 2.1 V for support circuitry, 1.5 V for the array, and 1.0 V for RWD. The chip contains four 256-Mb quadrants, each containing eight 32-Mb banks, which are arranged in a 4 \times 2 matrix. Row decoders (RDEC's) are located horizontally in the center of each 256-Mb quadrant. Hierarchical column decoders (HCDEC's) divide the 256-Mb quadrant, resulting in four 64-Mb units. Row redundancy fuses and decoders are located horizontally in

RDEC's design space. Each 32-Mb unit is divided into two 16-Mb domains, where 27 flexible row redundancy replacement elements are realized without using a separate redundancy block [23]. Column redundancy fuses and decoders are arranged vertically in the HCDEC's design space. Each 32-Mb unit is divided into eight 4-Mb domains, where up to four column redundancy replacements are possible. A total of 2752 fails can be repaired by programming redundancy with 30 646 laser blowable fuses. This is about twice the amount of fuses and repairability as in the 220-mm², 256-Mb SDRAM [10]. A depletion-mode NMOS current limiter [23] is also designed for each column in order to reduce wordline-to-bitline short-circuit current. The flexible test-mode concept [24] is used including more than 100 stackable test states. These are actively used for debugging and characterization. The array voltage generators are arranged at the right and left edges of the 256-Mb quadrant. This arrangement allows the bitline sensing voltage to be effectively supplied from the power bus located horizontally over the quadrant. The break between two 32-Mb banks within a 64-Mb unit are used for arranging the power bus for the RDEC's vertically. The space under the power bus is used for allocating a decoupling capacitance with trench cells for the array voltage supply. This reduces noise generated by a bitline sensing operation. Support circuits are located between the top and bottom 512-Mb chip halves, where 88 bonding pins and 42 option and test pins are arranged in a single row.

When a pulsed RAS occurs, two out of 32 32-Mb banks (or one from each chip half) are activated as a bank for $\times 16$ organization. This allows a 16-independent bank configuration with 12 rows, four banks, and ten column addresses. A chip configuration with 32 DQ's is also available as a bonding option, where four out of 32 32-Mb banks are activated as a bank. The $\times 32$ organization chip has eight independent banks with 12 rows, three banks, and ten column addresses. The two quadrants in the left chip half are associated with 8 DQ's (16 DQ's for $\times 32$) at the left chip edge, and the two quadrants in the right chip half are associated with 8 DQ's (16 DQ's for $\times 32$) at the right chip edge.

III. KEY DESIGN ELEMENTS

A. Hybrid Bitline Scheme

Each 32-Mb bank (Fig. 3) is organized into four 8-Mb blocks, each consisting of 2-K wordlines (WL's) and 4-K bitline pairs (BL's). The single-sided WL architecture [10] supports 4-K trench cells per WL stitched with 0.13- Ω /sq aluminum *M*₂. A hybrid BL scheme is used to improve array efficiency. Here, 512 cells are connected to each local-BL (LBL) wired with the tungsten *M*₀ layer. This is twice the number of cells/BL used for 256-Mb DRAM's [10], [22]. Four LBL pairs are connected to each sense amplifier (SA) multiplexed through switches (MUX{0:3}) located adjacent to the SA. Two of the LBL pairs are connected to the SA multiplexers (MUX{1, 2}) by wiring over other LBL's using the aluminum *M*₁ layer. This scheme results in a reduction of the number of SA's to 1/4 that of the 256-b/BL architecture, reducing chip size by 6%. Two-K SA's located in each 8-Mb block boundary are interleaved and multiplexed for two

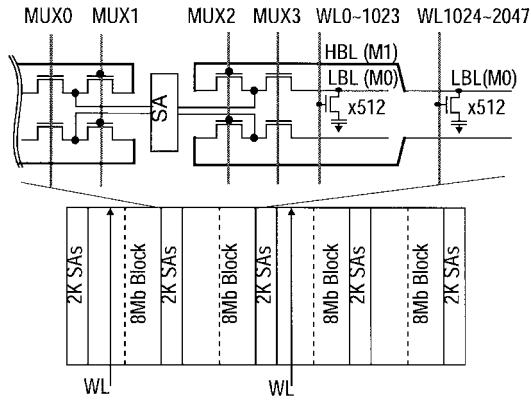


Fig. 3. Hybrid-BL architecture.

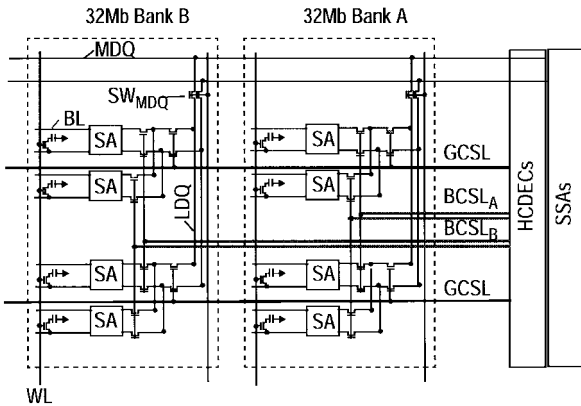


Fig. 4. Hierarchical CSL architecture.

adjacent 8-Mb blocks. This makes it possible to interleave the HBL's at the center of each 8-Mb block, increasing the HBL pitch to twice the LBL pitch. The HBL capacitance is approximately 1/4 the LBL capacitance. Since half of the LBL's are directly coupled to the SA's, the additional refresh current is only 11% greater than the standard 512-cells/BL architecture. A sensing signal of about 100 mV is maintained by utilizing a 35-fF deep-trench storage capacitor with 1.5-V array voltage. Unlike previously reported hierarchical BL schemes [25], this hybrid BL scheme uses a simple four multiplexers for sharing sense amplifiers, resulting in no access speed penalty. No additional array breaks are required, minimizing the area penalty of the MUX's.

B. Hierarchical CSL Scheme

A hierarchical column-select scheme [15] is incorporated with a hierarchical dataline architecture [10], [22]. This improves the third-metal (M3) utilization for column select and hierarchical datalines over the array. This also makes 8-b prefetch with two independent banks possible with minimum silicon area penalty. Each 64-Mb unit (Fig. 4) contains two banks: A and B. Each 64-Mb unit is configured as eight 8-Mb double segments (DSEG's). The boundary of the segment is aligned to the second-metal (M2) WL stitch break. Each 8-Mb DSEG contains eight hierarchical dataline pairs (MDQ's). The banks A and B share 64-s sense amplifiers (SSA's), which are located adjacent to the hierarchical column decoders

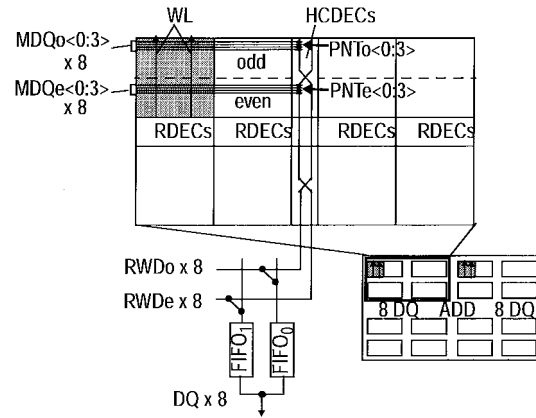


Fig. 5. Hierarchical 8-b prefetch.

(HCDEC's). They connect to the 64 MDQ's across the eight DSEG's, which then connect to local datalines (LDQ's) in each sense amplifier block through MDQ switches (SW_{MDQ}). This allows the bits to be read from the BL's in the selected 8-Mb block to the MDQ's, or vice versa for the write mode. The MDQ switches are activated with a row access command, resulting in no access penalty for the column access speed. In order to reduce the banking penalty, the HCDEC's drive 256 global column-select lines (GCSL's), which are common to banks A and B. Additionally each bank has four independent bank column-select-lines ($BCSL_A$ and $BCSL_B$) per 32 GCSL's to decode two column addresses with a bank address. A BL is coupled to the LDQ only when both the GCSL and BCSL are simultaneously activated. This allows bank A to be operating in signal-development mode while performing a column access in bank B by activating GCSL and $BCSL_B$ while disabling $BCSL_A$. Only 256 GCSL's, 64 BCSL's, and 64 MDQ pairs are allocated over each 64-Mb unit. The array power and ground wires are arranged in the remaining space, reducing the voltage drop that occurs when 64 bits are read or written simultaneously for the hierarchical 8-b prefetch.

C. Hierarchical 8-b Prefetch

Each 64-Mb unit (Fig. 5) is logically divided into even and odd 32-Mb column-address regions. Each region contains eight sets of four even MDQ's ($MDQ_e\langle 0:3 \rangle$) or eight sets of four odd MDQ's ($MDQ_o\langle 0:3 \rangle$). Each set of $MDQ_e\langle 0:3 \rangle$ and $MDQ_o\langle 0:3 \rangle$ supports eight burst bits for the corresponding DQ as a hierarchical 8-b prefetch. Sixty-four bits, or eight burst bits \times 8 DQ's, are simultaneously read or written with eight sets of $MDQ_e\langle 0:3 \rangle$ and $MDQ_o\langle 0:3 \rangle$ per column access. Two out of eight burst bits on $MDQ_e\langle 0:3 \rangle$ and MDQ_o are then selected by one out of four pointers ($PNT_e\langle 0:3 \rangle$ for $MDQ_e\langle 0:3 \rangle$ and $PNT_o\langle 0:3 \rangle$ for $MDQ_o\langle 0:3 \rangle$), transferring two consecutive burst bits to the corresponding RWDe and RWDo simultaneously. For a sequential burst with an odd starting addresses, the $PNT_e\langle 0:3 \rangle$ are generated from incremented addresses. For example, if the starting column address is zero, $PNT_e\langle 0 \rangle$ and $PNT_o\langle 0 \rangle$ are simultaneously activated. On the other hand, if the starting column address is one, incremented $PNT_e\langle 1 \rangle$ and $PNT_o\langle 0 \rangle$ are activated simultaneously. The two even and odd bits on RWDe and RWDo are then sent to two

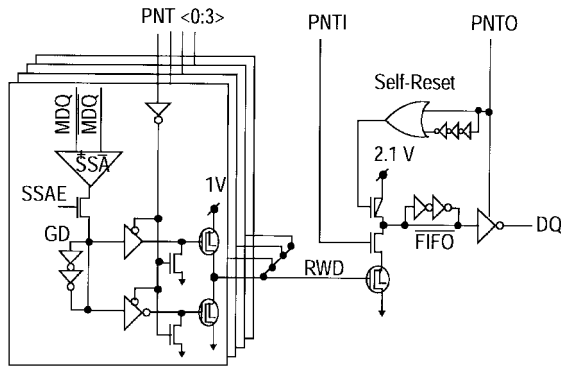


Fig. 6. A 1-V swing single-ended RWD.

FIFO circuits (FIFO₀ and FIFO₁) when the FIFO input pointer (PNTI) is enabled. PNTI includes a reordering switch so that the even and odd bits are stored as the first and second burst bits in FIFO₀ and FIFO₁, respectively. The eight RWD_e's and eight RWD_o's for eight DQ's are twisted at the center of each HCDEC and shared with the adjacent 64-Mb unit, eliminating 32 wires or 75 μm per chip [26]. This hierarchical 8-b prefetch architecture reduces the array and datapath frequencies to 1/8 (or 20-ns cycle time) and 1/2 (or 5-ns cycle time), respectively, for the 200-MHz DDR operation. Final one out of two selection is enabled by the FIFO output, boosting the column burst frequency over 400 Mb/s per DQ.

D. 1-V Swing Read-Write-Drive Signaling

Reducing the column burst current is an important design goal particularly for $\times 32$ 200-MHz DDR operation. The signal transfer from the second sense amplifiers (SSA's) to the FIFO circuitry is a significant contributor to the column burst current. Single-ended RWD signaling [10] was proposed to reduce RWD current. The result was a reduction of 50% of the current for complementary RWD signaling [22]. A 75% current reduction would be expected on average, assuming a random data pattern. The previous single-ended RWD signaling, however, consumed 60 mA for 200-MHz DDR operation. This causes a voltage drop from the external power bus, limiting the burst frequency. When CMOS drivers are used to realize low-voltage signaling [15], [27]–[28], the gate overdrive of the PMOS pullup device is reduced as the voltage is reduced, causing a speed penalty.

To improve performance, low-voltage RWD signaling is implemented with the NMOS-only driver, shown in Fig. 6. The NMOS pullup device has increased the gate overdrive as the voltage is reduced, resulting in a high-speed RWD swing. Low-threshold-voltage NMOS's (shown encircled in Fig. 6) are used in the RWD driver and FIFO receiver to further improve performance at low voltage. During a read operation, a CMOS cross-coupled SSA amplifies the 200-mV signal on the MDQ pair, which is latched at the node GD. MDQ's are quickly reset when the SSAE signal turns off for the next column command in a pipeline manner. PNT<0:3> sequentially selects one out of four GD<0:3>, resulting in a 4-bit burst transfer per RWD. The FIFO circuitry uses a

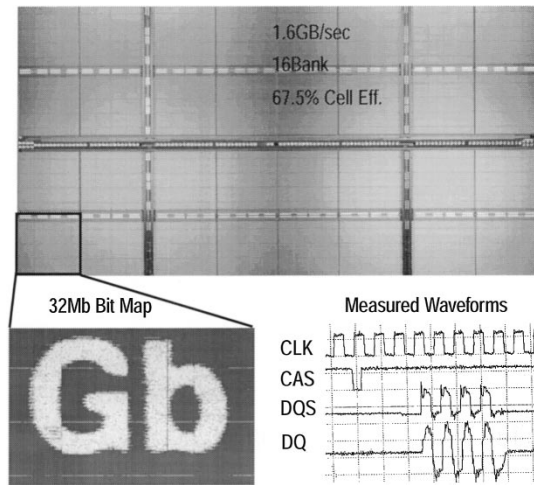


Fig. 7. Measured 32-Mb bitmap and waveforms.

self-timed dynamic latch, where the 1-V-swing RWD data are fetched at the node $\overline{\text{FIFO}}$ when the input pointer (PNTI) goes high. The node $\overline{\text{FIFO}}$ is precharged to 2.1 V after the data have been transferred to DQ with output pointer (PNT0). An RWD delay monitor is used to synchronize the RWD operation with the PNTI. The 1-V-swing single-ended RWD reduces the peak burst current by 36 mA and reduces the average burst current by 18 mA compared to the CMOS level (2.1 V) swing RWD for the $\times 32$ 200-MHz DDR operation.

IV. HARDWARE RESULTS

Fig. 7 shows the measured 32-Mb bitmap, which was obtained using the following image-sensing procedure, which visually demonstrates cell operation. The array is first written with a physical "1" data pattern. A clear film with opaque letters "Gb" is placed over the array, and the chip placed under a microscope. The microscope light is used to illuminate the chip. The cells that are not masked by the template collect photo-induced electrons in the n+ junction of the storage node of these cells. The collected charge changes the data in the unmasked cells from a physical "1" to a physical "0." These cells appear as fails or dark areas on the bitmap. The cells under the template retain their data and appear as passes or light areas on the bitmap. The resulting bitmap, shown in Fig. 7, demonstrates the successful functionality of the chip. Fig. 7 also shows the measured CLK, CAS, DQS, and DQ waveforms measured at 85°. After the preamble of the DQS, DQ starts to swing, while synchronizing with the DQS in a source-synchronous manner.

Fig. 8 shows a scanning electron microscope cross section of the array showing the deep trench as having over 35 fF capacitance, wordline (WL: poly), local bitline (LBL: $M0 Al$), hierarchical hybrid bitline (HBL: $M1 Al$), and master wordline for the stitched WL architecture (MWL: $M2 Al$). Note that the MWL is also pitched limited, which is successfully realized with planarized 0.175- μm , 8F² trench technology [1].

Fig. 9 shows a chip microphotograph of an experimental 128-Mb DRAM. This chip was designed prior to the 1-Gb DRAM for studying hybrid BL architecture, hierarchical

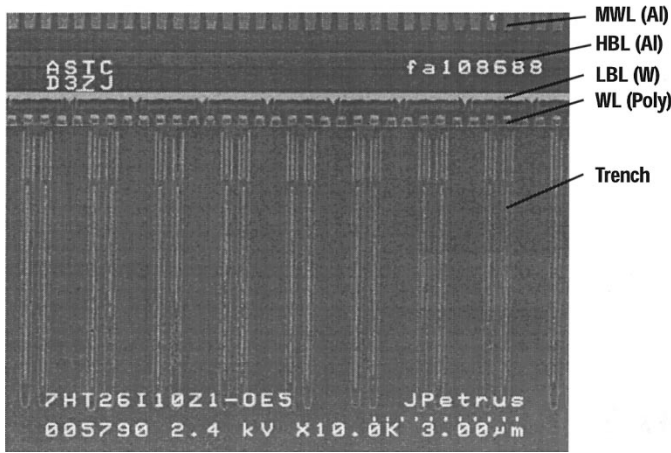


Fig. 8. 0.175- μ m, 8F² trench technology.

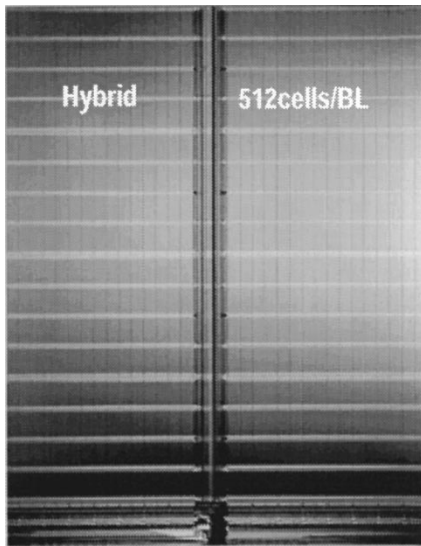


Fig. 9. Microphotograph of the experimental 128-Mb DRAM.

column-select circuitry, 8-b prefetch, and 1-V-swing RWD signaling. The 128-Mb DRAM is almost identical to the 128-Mb double units used in the 1-Gb DRAM. It does, however, include 512 cells/BL for the right 64-Mb unit and hybrid BL with 256 cells/BL for the left 64-Mb unit. By opening the BL multiplexer with a test mode [24], 1024 cells/BL and hybrid BL with 512 cells/BL operation can also be studied. Fig. 10 shows the measured refresh currents of: 1) 512 cells/BL, 2) hybrid 256 cells/BL, and 3) hybrid 512 cells/BL, which agree with the calculated numbers. Although the 512 cells/BL scheme consumes 50% more current over that measured in the conventional 256 cells/BL, the chip size reduction due to the reduction of the sense amplifiers is significant. The additional refresh current required for the hybrid BL scheme with 512 cells/BL is only 11%. Fig. 10 also shows the measured RWD waveforms with signaling voltages of 0.5, 0.75, 1.0, and 1.5 V, demonstrating 200-Mb/s data rate with 0.75 V \sim 1.5 V.

Fig. 11 shows the DQ waveforms and the burst currents measured in the 1-Gb DDR SDRAM at 85° at the wafer level.

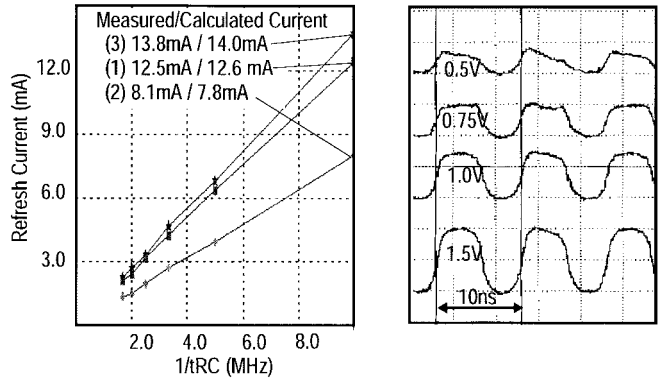


Fig. 10. Measured refresh current and RWD waveforms.

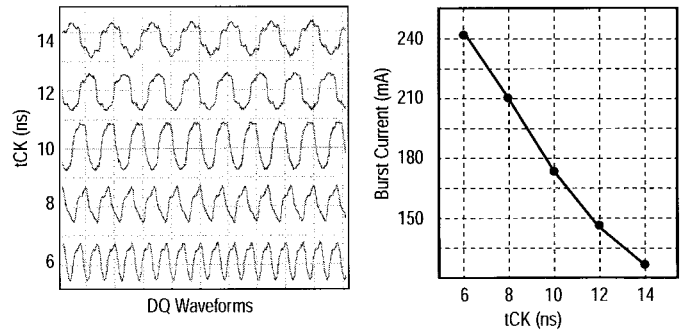


Fig. 11. Measured seamless burst read waveforms for various frequencies.

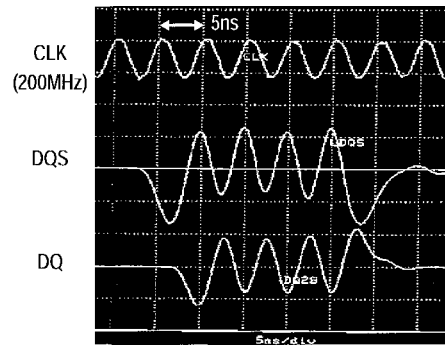


Fig. 12. 400-Mb/s/pin burst read waveforms measured from the chip in 16-mm TSOP-II module.

Seamless burst read operations were performed for various frequencies. Excellent functionality is observed for a wide range of frequencies. The current dissipation for 167-MHz DDR operation is 240 mA. Fig. 12 shows the clock, data output (DQ), and data strobe (DQS) for 200-MHz DDR operation. The waveforms were measured from the chip in a TSOP-II module with stub series terminated logic (SSTL) interfaces for the 8-b burst mode. After the preamble of DQS, the DQ swings, demonstrating 400 Mb/s/pin. This results in 1.6-Gb/s/chip bandwidth with $\times 32$ organization. The maximum operating frequency could not yet be confirmed due to the tester limitations. Operation over 600 Mb/s/pin is predicted by simulation, realizing 2.4 Gb/s.

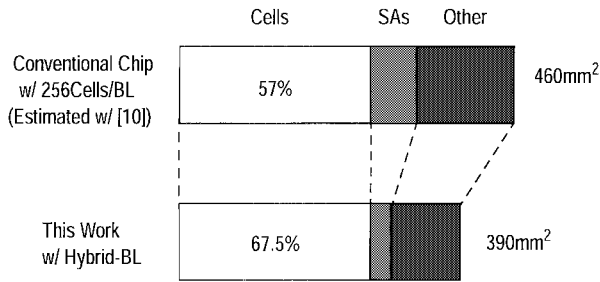


Fig. 13. Components of the chip size reduction.

TABLE I
SUMMARY OF THE 390-mm², 1-Gb DDR SDRAM

| | |
|--------------|---|
| Technology | 0.175 μ m 8F ² CMOS Trench |
| Chip Size | 14.3mm x 27.3mm (390.39mm ²) |
| Package | 16mm x 29.5mm 88pin TSOP-II |
| Memory Cell | 0.35 μ m x 0.7 μ m |
| Voltage | V _{DD} : 2.5V V _{SUPPORT} = 2.1V V _{ARRAY} = 1.5V V _{RWD} = 1.0V |
| Organization | 4Mb x 16banks x 16DQs 4Mb x 8banks x 32DQs |
| Interface | SSTL/LVTTL |
| Performance | 800MB/sec for x16 1.6GB/sec for x32 |
| Refresh | 8K / 16K |

V. CONCLUSIONS

A 390-mm², 16-bank, 1-Gb DDR DRAM with 0.175- μ m CMOS trench technology has been demonstrated. This chip realized high performance of 1.6-Gb/s or beyond while maintaining superior cell/chip area efficiency of 67.5%. This demonstrates the feasibility of over 200-MHz DDR SDRAM operation with an approach that is more cost effective than other approaches [12], [13], [16], [18], making DDR SDRAM a potential candidate for future computer systems. These accomplishments have been realized by the following key ideas:

- 1) hybrid-BL architecture;
- 2) hierarchical CSL scheme;
- 3) hierarchical 8-b prefetch;
- 4) 1-V swing RWD signaling.

This paper also discussed the important advantages of the trench cell technology over the stacked cell technology to enable 512 cells/BL, an additional layer for the hybrid BL, and 4-K stitched WL architecture in 0.175- μ m minimum features. Fig. 13 shows the components of chip size reductions, where the chip size reference is extrapolated from a 256-Mb DRAM [10]. The 14.3 x 27.3 mm², 1-Gb DRAM [19] has realized 67.5% cell/chip efficiency, which is approximately 15% smaller than a conventional chip [10] with 57% cell/chip

efficiency. Table I summarizes the chip's features and process technology.

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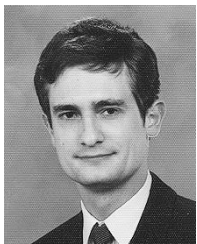
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