

SP 25.5: A Noise-Immune GHz-Clock Distribution Scheme using Synchronous Distributed Oscillators

H. Mizuno, K. Ishibashi

Hitachi, Ltd., Central Research Laboratory, Tokyo, Japan

In the near future, microprocessor clock frequencies will go beyond 1GHz.[1] In GHz microprocessors, a single-phase-locked loop (PLL) is difficult to use since the delay in distributing and buffering the clock from the single PLL is more than 1 clock cycle. A multiple-PLL method that distributes many PLLs on a chip solves this problem, but significantly increases the skew and jitter induced by noise.

Figure 1 shows a scheme for clock distribution comprising a single-PLL with multiple outputs. The PLL is constructed of a phase frequency detector (PFD), a charge pump (CP), a low pass filter (LPF), and voltage-controlled oscillators (VCOs). The divide-by-2 circuit for generating an accurate 50% duty is omitted from the figure for simplicity. #1-n are VCOs, and the numbers shown on the right side of each last-stage inverter are its relative driving capability. These numbers correspond to the number of nearest-neighbor oscillators. The outputs of VCOs are connected by equal-length lines of length l (in line configuration). These interconnections force all ring oscillators to oscillate with no skew. The globally-distributed VCOs are synchronized, and these outputs are fed to the local clock distribution network via short wires. If the frequency and/or phase of one ring oscillator is changed by interference, the other ring oscillators cooperate to maintain the same frequency and/or phase. The ring oscillators thus work as a decoupling capacitor for power distribution.

Voltage V_c is a frequency-control signal for the VCOs and controls all VCOs via a global V_c distribution network. In conventional clock distribution, the global clock is distributed across the entire chip. In contrast, this method distributes V_c , which is not a clock signal but is a level. The noise immunity of the level signal is enhanced by shielding, buffering, and filtering.

The SDOs are not limited to in-line configuration. A $m \times n$ matrix configuration permits the VCOs to be distributed over the entire chip as shown in Figure 2. This configuration allows the VCOs to be placed near each local-clock-distribution network. This eliminates the clock-skew and delay in distributing the conventional global clock.

Microprocessors are becoming increasingly noisy environments, so the delay variation due to the noise is becoming significant. Unfortunately, as with the conventional multiple-PLL method, distributing the VCOs over the entire chip causes the problem that jitter and skew are increased by variations in the fabrication process (static), temperature, and power supply (dynamic).[2]

Figure 3 shows the simulated open-loop analysis of increases in static τ_{jitter}^{VCO} and τ_{skew}^{VCO} caused by variation in threshold voltage.

The threshold voltage of one VCO is changed by up to $+0.1V$. Here τ_{skew}^{VCO} is the phase difference among VCOs. And τ_{jitter}^{VCO} is the frequency difference caused by varying the threshold voltage. Thus, it does not contain an intrinsic jitter of the PLL. Lines conv represent the conventional multiple-PLL method. In this method, each VCO is not connected with the interconnections. In contrast, m33 and m44 represent 3×3 and 4×4 configurations, where l is set to 3 mm for m33 and to 2 mm for m44. The drive capability

of each VCO is adjusted to maintain the same oscillator output shape. As shown in Figure 3, τ_{jitter}^{VCO} and τ_{skew}^{VCO} are reduced to 1.9% and 3.5%, respectively. These values are 1:6.5 and 1:3.5 smaller than those of the multiple-PLL method.

Figure 4 shows the simulated open-loop analysis of increases in dynamic τ_{jitter}^{VCO} and τ_{skew}^{VCO} caused by change in supply voltage.

The supply voltage of one VCO is reduced by 10% compared to that of others. Consequently, τ_{jitter}^{VCO} and τ_{skew}^{VCO} are reduced to about 1.9% and 3.5%, respectively. These values are 1:6.5 and 1:3.5 smaller compared to those of the conventional method.

The transient response of m44 (in Figure 4) with 10% change in supply voltage for 3-9ns is shown in Figure 5. Dashed line N.N. shows the waveform when there is no supply voltage noise. Dotted line conv represents the model of the conventional multiple-PLL method. The other 16 solid lines are the output of each VCO. The clock-skew of the conventional model (conv) accumulates to 650ps in 3-9ns. In contrast, that of the proposed method is 50ps. Thus, long-term jitter is reduced by 1/13. In the conventional model, when the noise is applied, cycle-to-cycle jitter accumulates to as much as 39% (140°) of the clock cycle. This phase error must be corrected using PLL feedback. However, that of the proposed method continues to be 2.3% (8.3°) independent of this period. This reduction means that the method provides more PLL loop gain design tolerance and reduces intrinsic jitter of the PLL.

To demonstrate the operation of the SDO, a test chip is fabricated by using a 0.25 μ m CMOS technology shown in Table. 1. Figure 6 shows a micrograph of the chip. 264 17-stage ring oscillators are implemented with various values of l (113, 226, 451 ... 3606 μ m) with in line configuration (Figure 1). The chip is 7.3x1.1mm (including bonding pads for measurement). Figure 7 shows the measured waveforms of jitter and skew using the FET-probe for (a) oscillator #1 and (b) oscillator #65 with l of 113 μ m. In both measurements, oscillator #1 is used for the trigger. Note that measured power supply has about ± 100 mV high-frequency power-supply noise induced by many ring oscillators. The jitter for oscillator #1 is 97ps (4.2%). Oscillator #65 is 7213 μ m away from oscillator #1. Here, the jitter is 170ps (7.4%). Mean skew between oscillators #1 and #65 is 17ps (0.7%).

Acknowledgments:

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References:

- [1] Gieseke, B., et al., "A 600MHz Superscalar RISC Microprocessor with Out-Of-Order Execution," 1997 ISSCC Digest of Technical Papers, pp.176-177, Feb., 1997.
- [2] Young, I., et al., "A PLL Clock Generator with 5 to 110MHz of Lock Range for Microprocessors," IEEE Journal of Solid-State Circuits, Vol. 27, No. 11, pp.1599-1607, Nov., 1992.

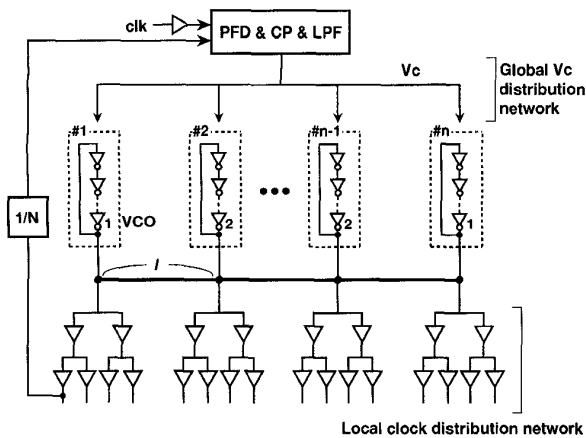


Figure 1: Newly developed clock distribution using synchronous distributed oscillators.

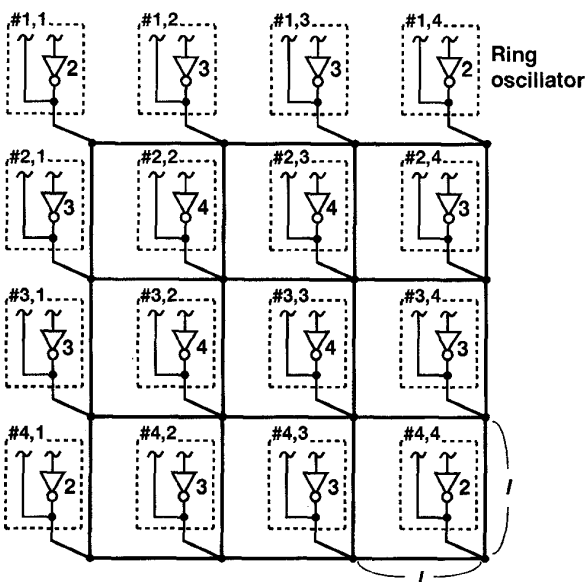


Figure 2: Synchronous distributed oscillators in matrix configuration.

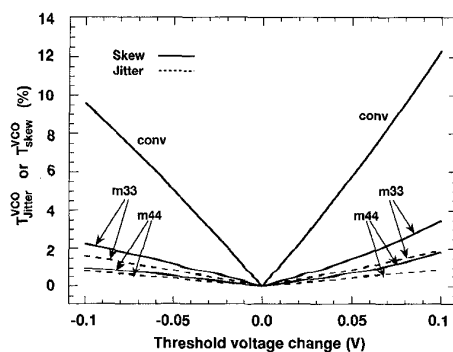


Figure 3: Jitter or skew sensitivity to threshold voltage variation.

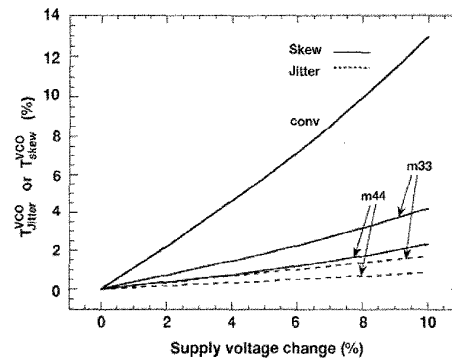


Figure 4: Jitter or skew sensitivity to supply voltage change.

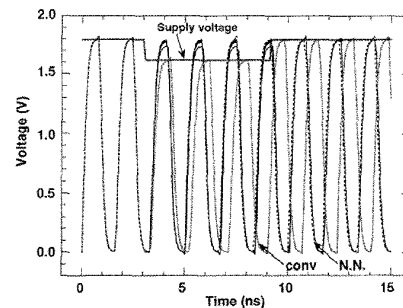


Figure 5: Transient response to 10% power-supply reduction.

Figure 6: See page 474.

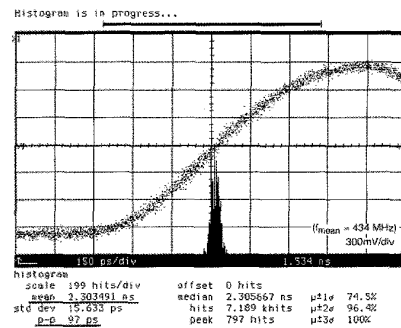


Figure 7: Measured waveforms (a) Oscillator #1, (b) See page 474.

Technology	0.25μm CMOS, 1-poly, 5-metal
MOSFET	tox 4.5nm
Vth*	0.15V(n)/-0.15V(p)
Metal pitch	0.98μm
Supply voltage	1.8V
Temperature	75° C

*Vth=Vgs at Ids = 10nA, W=15μm

Table 1: Device and process parameters.

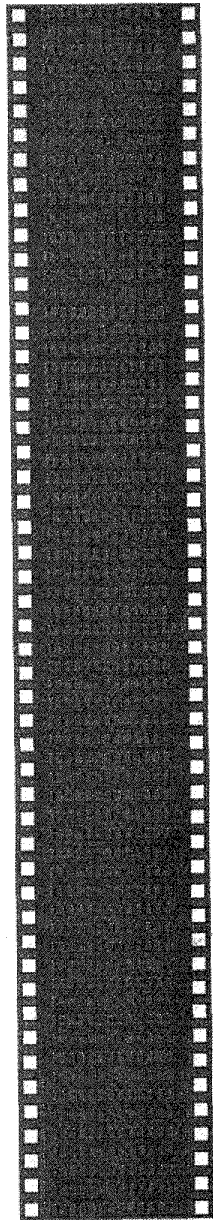


Figure 6: Chip micrograph.

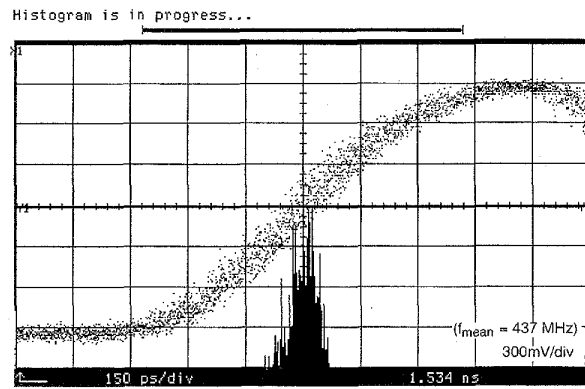


Figure 7: (b) Oscillator #65.