Design Methodology for Optimizing Gate Driven ESD Protection Circuits in Submicron CMOS Processes

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Abstract - This paper describes the design methodology for gate driven NMOS ESD protection in submicron CMOS processes. A new PNP Driven NMOS (PDNMOS) protection scheme has been presented. Without requiring any additional process steps or introducing any additional impedance in signal path, the PDNMOS is effective even for small analog/mixed-signal designs. SPICE simulation is used to optimize the design. High ESD performance of PDNMOS protection in both non-silicided and silicided submicron processes has been demonstrated in this work.

I. Introduction

On-chip Electrostatic Discharge (ESD) design in advanced submicron CMOS processes becomes more challenging as process feature sizes continue to scale down. Shallow junctions, thick salicides, and thin epitaxial layers in advanced CMOS process have shown a negative impact on the ESD capability [1-3]. Approaches such as developing a built-in ESD robust process [4], using an extra implant to make the junction deeper [5], can be used to improve process ESD capability and thus improve the product ESD protection level. For a given process technology, however, the level of product ESD protection performance would rely heavily on the ESD protection circuit design methodology and its implementation.

In submicron CMOS processes, the thin gate oxide and low drain breakdown voltage make the NMOS the most vulnerable element to an ESD event. The NMOS thus usually dictates ESD protection performance in the processes. For ESD protection design, the gate grounded NMOS (GGNMOS) protection scheme was originally used for an output NMOS protection. The problem with the GGNMOS is that many NMOS fingers do not necessarily turn on during an ESD event [2,6]. Using additional process steps to block the salicide in the ESD NMOS and output NMOS could achieve an adequate ESD performance [7]. This method, however, increases product cost due to additional process masks needed and adds an extra impedance into a signal path due to the non-silicided contact-to-gate spacing of the output NMOS. This additional impedance in signal path degrades circuit's high current drive capability, which is usually required in most analog/mixed-signal applications. The Gate Coupled NMOS (GCNMOS) [6] and the Gate Modulated NMOS (GMNMOS) [8] were also proposed for CMOS input, output, and I/O pin ESD protection. These two designs were based on a protection NMOS gate driven effect. But the GCNMOS is not effective in silicided submicron CMOS processes especially with thin epi layers [9] and the GMNMOS needs a complex predrive circuit network. Recently, a Substrate Triggered NMOS (STNMOS) protection scheme for advanced submicron CMOS processes was presented, without the use of additional masks or additional impedance [10]. But the requirement of a large chip capacitance (>1 nF) limits its application in small analog/mixed-signal chip designs.

This paper describes the design methodology for gate driven NMOS ESD protection in submicron CMOS processes. A new PNP Driven NMOS (PDNMOS) protection scheme for both nonsilicided and silicided submicron CMOS processes is given. The protection scheme does not require any additional process steps or masks and is effective even for IC's with smaller chip capacitance. Detailed design methodology and optimization of this new protection scheme are

presented. As shown here, layout of the protection scheme can follow the minimum process design rules to result in a relatively small protection area. High ESD performance, no added impedance in the signal path, and the use of only a small chip capacitance on power supplies in PDNMOS make it suitable for small analog or mixed-signal chip designs. The PDNMOS scheme has been used for digital/analog CMOS input, output, and power supply pin protection. ESD protection levels of > 4 kV HBM, >350 V MM, and > 1.5 kV CDM for mixed-signal IC with a small chip size of 95 mil x 136 mil have been obtained in production.

II. ESD Protection Design Methodology

II-A. Issues for NMOS ESD protection designs in submicron CMOS processes

In general, there are two basic requirements for an ESD circuit design. First, a good clamping capability, which indicates that the primary ESD device can handle a large ESD current while the pad voltage should be clamped below the failure voltage of both the device being protected and the protection device itself. Second, a low trigger voltage, which allows the primary ESD device to turn on before the device being protected reaches its failure voltage. In submicron BiCMOS processes, a Bipolar SCR (BSCR) [11] or Multi-Emitter Finger NPNP (MEFNPN) [12] could be used as a primary ESD protection device and a zener breakdown voltage of base-emitter junction could be used as the trigger voltage. In submicron CMOS processes, unfortunately, the low voltage zener diode is not available. The lowest junction breakdown voltage is the NMOS drain junction breakdown voltage. The most efficient bipolar device for handling ESD current is the parasitic lateral NPN of an NMOS device.

Figure 1 shows a typical high current-voltage curve for a gate grounded NMOS transistor, where Vt1 is the trigger voltage of the parasitic lateral NPN (LNPN) of the NMOS, Vsp is the snapback voltage, Vt2 and It2 are the second breakdown voltage and current. It2 is a key process ESD parameter to monitor the high current handling capability of an NMOS. Beyond second breakdown (Vt2, It2), the NMOS enters the regime of thermal runaway which results in the device being destructively damaged. The snapback of the NMOS I-V characteristic is due to the turn-on of the parasitic lateral NPN (LNPN) of the NMOS. After snapback, the lateral NPN of the NMOS conducts most of the drain terminal current, with a small on-resistance *Ron*. It is found that It2 strongly depends on the beta of the LNPN, NMOS channel length, salicide thickness, drain junction depth, and epi layer thickness [3].

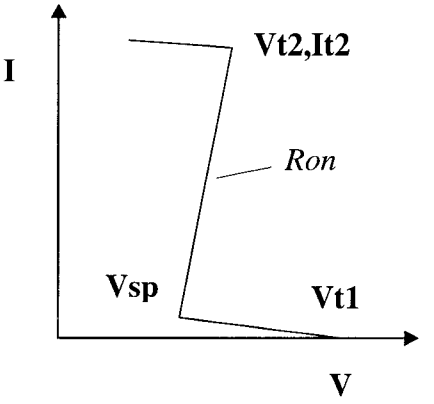

Figure 1. A typical high current I-V curve of a gate grounded NMOS in submicron CMOS process.

The value of NMOS It2 in a relatively ESD robust submicron CMOS process can be between 3 and 10 mA/um, measured using a Transmission Line Pulse (TLP) tester with 200 ns pulse width, for a single NMOS with 40 ~ 50 um width and minimum channel length. This It2 value makes it possible to use an NMOS as the primary ESD protection device in submicron CMOS processes, even though it is less than those of BSCR (20 mA/um) [11] and NPN (12 mA/um) in submicron BiCMOS processes [12]. Due to its relatively low It2, compared with BSCR and NPN, a relatively large size of NMOS is needed in order to achieve a good ESD protection if the It2 scales with the NMOS size. It was found, however, that the It2 value decreases with increase of NMOS width for a single finger NMOS. For instance, a value of 4 mA/um It2 for a single finger 50/0.8 um NMOS can degrade to 2.8 mA/um for a single finger 100/0.8 um NMOS in the same process. Therefore, an ESD protection NMOS is laid out as a multi-finger device with an optimal finger width in order to conduct a large ESD current.

For a gate grounded multi-finger NMOS, it was found that, in most submicron CMOS processes, It2 does not necessarily scale with the number of the NMOS fingers, due to the second breakdown voltage Vt2 being less than the LNPN trigger voltage Vt1 (shown in figure 1). Hence, for a given process, success of a multi-finger NMOS ESD protection depends on its

ability to turn on multiple LNPNs (or NMOS fingers of a protection NMOS) to uniformly conduct ESD current.

Turn-on of multiple LNPNs can be achieved in design if Vt2 is higher than Vt1 [2]. When Vt2 > Vt1, each LNPN of a NMOS finger would, during an ESD event, turn on to conduct the ESD current before any single LNPN reaches second breakdown.

Vt2 can be increased above Vt1 by increasing the drain/source contact to poly gate spacing (CGS) in nonsilicided processes. It, in turn, increases the snapback on-resistance, *Ron* [2]. In silicided processes, a silicide block is needed for such implementation. On the other hand, by increasing substrate potential or applying a small positive substrate bias to substrate, Vt1 can be reduced to below Vt2 [2,10]. The reduction of Vt1 can also be achieved by an approach of increasing the NMOS gate potential [2, 6]. Figure 2 shows the high current I-V curves of an NMOS under different gate biased condition, measured by a TLP system with 200 ns pulse width (200 ns pulse width were used in all TLP measurements in this work). As indicated in the figure, when the gate is biased high enough, Vt1 is

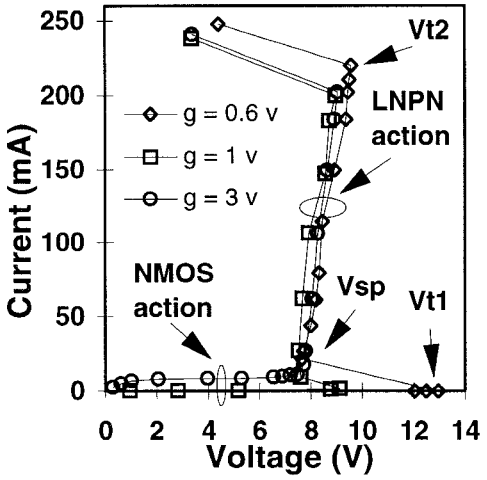

Figure 2. I-V curves of a 36/0.72 um NMOS in a 0.72 non-silicided CMOS process for different gate biases. A 200 ns pulse width was used in TLP measurements.

approximately equal to the snapback voltage (Vsp) which is less than Vt2. Note that once the bipolar transistor turns on in the snapback region, the gate voltage has no influence on the current in the snapback region, indicating that the NMOS action has been drastically reduced. Based on this gate driven effect, a new PNP Driven NMOS (PDNMOS) ESD protection scheme has been developed. In the PDNMOS protection, the parasitic LNPN of a protection NMOS is used as a primary protection device. The gate of the protection NMOS is driven by a PNP during an ESD event.

II-B. Concept of the PDNMOS ESD protection scheme

Conceptually, the PDNMOS protection scheme consists of a multi-finger protection NMOS, a resistor, a capacitor, and a PNP device as shown in figure 3. The emitter of the PNP and the drain of the protection NMOS are connected to the pad being protected. The collector of the PNP and the gate of

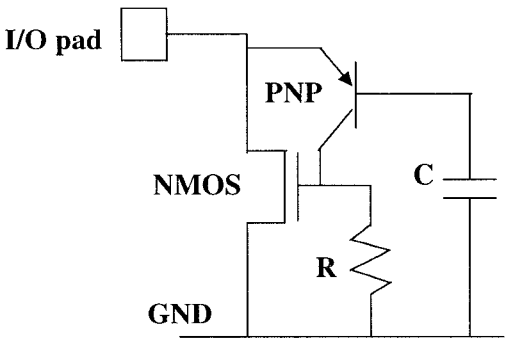

Figure 3. A simplified schematic of a PDNMOS.

the protection NMOS are connected to ground through a resistor R. The base of the PNP is connected to a capacitor. During an ESD event, the transient charge current of the capacitor provides the base current of the PNP to turn on the PNP. The collector current of the PNP biases the gate of the protection NMOS to first turn on the NMOS which then triggers the LNPN, when the pad voltage is approximately Vsp.

The PNP in the PDNMOS serves as a trigger element to trigger the protection NMOS during an ESD event. The capacitor should be large enough to enable the PNP to provide a suitable PNP collector current to raise the gate voltage of the protection NMOS. This would then turn on the protection NMOS. The capacitor can be realized by the parasitic capacitance of the power supply in the IC. Therefore, the base of the PNP is connected to a power supply for a PDNMOS protection for an I/O pad. Such configuration also ensures that the ESD circuit is off when the I/O pad voltage is within rail-to-rail range for normal circuit operation. During an ESD event, the charging of the parasitic capacitance of the power supply would provide the base current of PNP.

In a submicron CMOS process, the PNP is realized by a lateral PNP (LPNP) device. The LPNP device is built in an nwell in the same way as a PMOS device. A minimum poly gate length is used to enhance the LPNP action by minimizing the base width. Figure 4 is a simplified cross-section of the PDNMOS. Note that there is another parasitic vertical PNP (VPNP) device also shown.

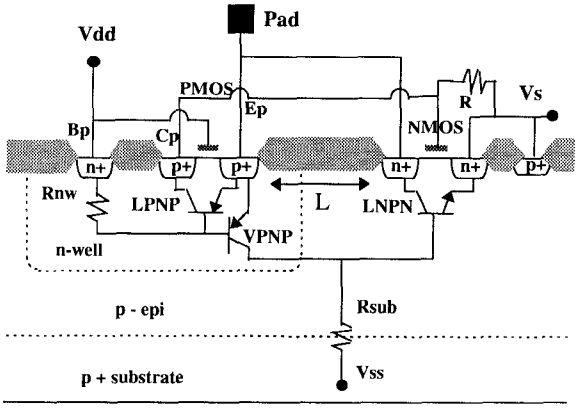

Figure 4. A simplified cross-section of a PDNMOS. Parasitic LPNP, VPNP, and LNPN devices are indicated in the picture. A large spacing L between PNPs and LNPN is used to prevent SCR trigger.

In the VPNP, the emitter and the base are the same as those of LPNP. But the collector of the VPNP is the p-epi layer. Under Vbe bias, both of the LPNP and the VPNP would turn on. The turn on of the vertical PNP during ESD would help to divert part of the ESD current into the p-substrate [13] and raise the local p-substrate potential thus enabling the trigger of the LNPN [10].

III. Development of the PDNMOS Protection Scheme

III-A. Trigger mechanisms of PDNMOS protection

An equivalent circuit of the simplified PDNMOS protection scheme is shown in figure 5. The total ESD current (*Iesd*) flow into PDNMOS can be expressed as

$$Iesd = Ielpnp + Ievpnp + Ic + Ids$$

where *Ielpnp* and *Ievpnp* are the emitter currents of LPNP and VPNP, *Ids* is the NMOS current, and the *Ic* is the LNPN collector current. The emitter currents of PNPs for a given pad voltage depend on PNP current gain, beta, nwell resistance Rnwell, and the base current. Since the base current is provided by the charge current of Vdd chip capacitance, a bigger Vdd capacitance results in a larger base current which, in turn, means larger emitter current. *Ic* is a function of *Ids* through the generation current, *Ig* given by [14]

$$Ig = (M\text{-}1)\,(Ids + Ic) = Ib + (Isub - Icvpnp)$$

where *M* is the multiplication factor dependent on the drain junction voltage Vd, *Ib* is the LNPN base current, *Isub* is the substrate current, and *Icvpnp* is the VPNP collector current. Before the LNPN turns on, *Ib*=*Ic*=0, and *Ids* will have an important role in the triggering. The trigger of the LNPN relies on the base potential Vsub = *Isub*·*Rsub*, where

$$Isub = (M\text{-}1)\,Ids + Icvpnp$$

and Rsub is the substrate resistance. For higher *Ids* and/or *Icvpnp*, it is easier to turn on the LNPN at a given *M*. Hence, it is important that, during an ESD event, a gate driven NMOS protection must have sufficient *Ids* and/or *Icvpnp* to obtain a low LNPN trigger voltage Vt1.

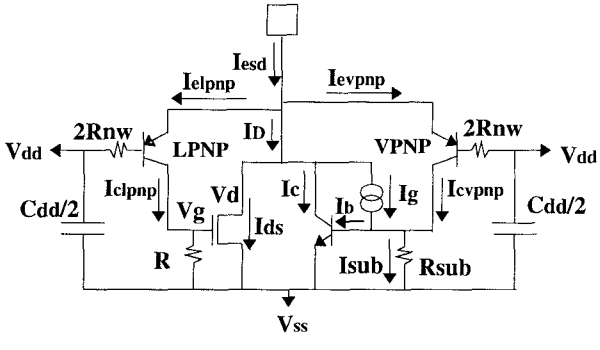

Figure 5. An equivalent circuit of figure 4.

Figure 6 shows values of Vt1 and Vt2 of a stand-alone 36/0.72 um NMOS in the 0.72 um non-silicided CMOS process. The measurements were carried out in a TLP system with the NMOS gate under different biases. In this case, *Icvpnp* = 0. *Isub* stems totally from *Ids*. As indicated in the figure, for gate voltage less than 1 V, Vt1 > Vt2, and Vt1 decreases as gate voltage increases. At around 1 V gate voltage, the Vt1 curve crosses the Vt2 curve. For gate voltage higher than 1 V, Vt1 < Vt2. The minimum Vt1 is around 8 V at gate voltage of about 3 V in this process. The largest margin of Vt2 - Vt1 is about 1V.

Without a gate driven effect or with the gate grounded, the NMOS is off and *Ids* = 0, which is a typical case of STNMOS [10]. All the *Isub* stems from *Icvpnp*. In order to obtain Vt1 < Vt2, a large *Icvpnp* is necessary. This, in turn, requires a large Ievpnp or large base current and results in a requirement of a large capacitance.

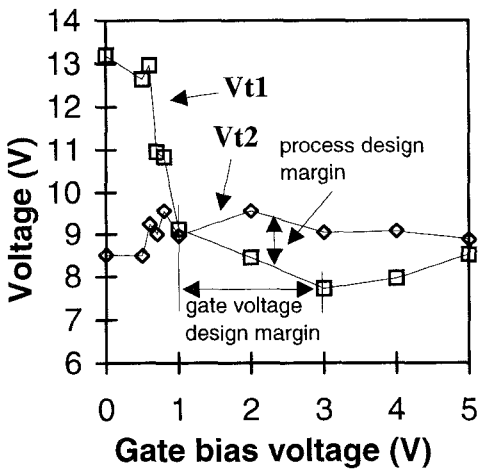

Figure 6. Values of Vt1 and Vt2 vs. gate bias voltage for a stand-alone 36/0.72 um NMOS in a 0.72 um non-silicided CMOS process.

As discussed previously, a PMOS is used to make the LPNP in such way that a minimum base width can be achieved. This results in a PMOS device in PDNMOS as shown in figure 4. The gate of the PMOS device in this work is connected to the base of LPNP or Vdd. The PMOS also provides an additional MOS current to bias the gate of the protection NMOS and thus enhance the gate driven effect to improve the PDNMOS performance.

III-B. Experimental Results

The PDNMOS structure was initially fabricated and tested in a 0.72 um non-silicided CMOS process. Based on the design methodology of the PDNMOS, there is no specific contact-to-gate spacing requirement in this design. The protection NMOS layout followed the process design rules and a minimum layout spacing is used in design. Figure 7 is the high current-voltage curves of a tested PDNMOS. The size of the protection NMOS is 520/0.72 um and the PNP is 144/0.72, the resistor R is 9 kΩ. The figure also shows Vt1 equal to the Vsp (= 8 V) of single NMOS as shown in figure 1. The 1V lower Vsp of the PDNMOS compared to that of a single NMOS could be due to the turn-on of multiple LNPNs which results in more *Isub* being generated at a given Vd. The lower Vsp of turn on of a multi-finger NMOS has also been reported previously [6].

Since PDNMOS operation relies mainly on the Vdd chip capacitance Cdd to provide the base current of PNPs, the ESD performance would be function of the

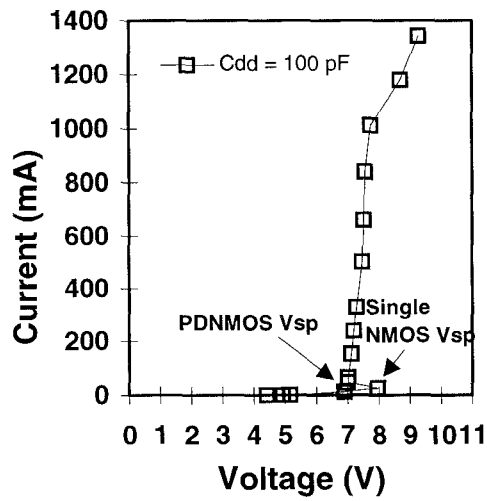

Figure 7. I-V curve of a PDNMOS in the 0.72 um CMOS process. The size of the protection NMOS is 520/0.72 um, The PNP is 144/0.72 um, the R is 9 kΩ. The PDNMOS was measured under a 100 pF Vdd capacitance, Cdd. The PDNMOS Vsp is shown and the single NMOS Vsp obtained from figure 2 is also indicated in the figure.

Cdd. Figure 8 shows the variation in HBM threshold (passed level) with Cdd for the PDNMOS. The peak ESD performance of the PDNMOS is about 6.5 kV HBM for a 100 ~ 200 pF Vdd capacitance, which is a typical Cdd range seen in most mixed-signal products.

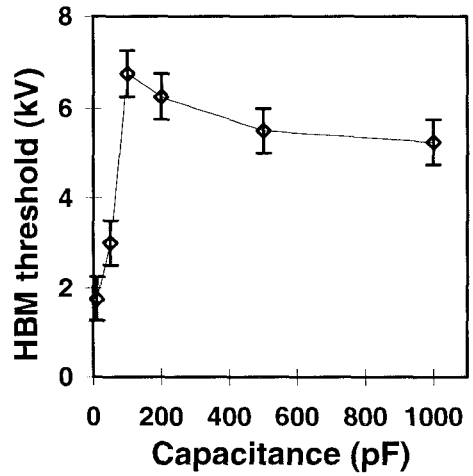

Figure 8. HBM ESD performance of the PDNMOS as function of Cdd for a 0.72 um non-silicided CMOS process. The size of the protection NMOS is 520/0.72 um and a minimum contact-to-gate spacing is used for the protection NMOS device.

The ESD performance at smaller values of Cdd is low because the gate voltage Vg of the NMOS was not high enough to generate sufficient *Ids* to trigger LNPN action in most NMOS fingers (also the *Icvpnp* current is low for a low Cdd because of the low base current). As the Vdd capacitance is increased, the higher base current of LPNP would result in a higher collector current of LPNP. The voltage of the gate of the NMOS would be increased. The reason for the small reduction in the ESD protection at large values of Vdd capacitance would be related to the NMOS gate voltage being too high, due to a large LPNP collector current (driven by a large base charging current) through the resistor R.

The degradation of LNPN high current handling capability for a high NMOS gate bias voltage has been observed in CMOS processes [1,2]. Figure 9 shows the measured second breakdown current It2 for different gate bias conditions in the 0.72 um

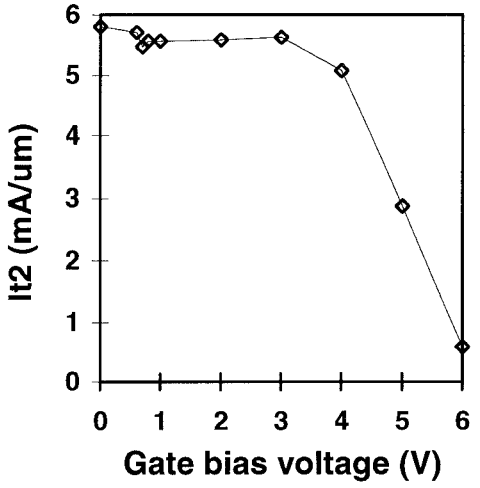

Figure 9. A 36/0.72 um NMOS It2 value vs. gate bias voltage in the 0.72 um CMOS process.

non-silicided process. The figure indicates that the It2 starts to drop when the gate voltage is higher than 3 V. This gate voltage roll off determines the gate voltage design margin (shown in figure 6) for a gate driven NMOS protection design.

III-C. Optimization of PDNMOS protection

As shown in the previous section, the ESD performance of PDNMOS varies with the Vdd chip capacitance, depending on the gate voltage of the protection NMOS during ESD events. For a given design, or a given Vdd chip capacitance, the size of the PNPs and the value of the resistor in the PDNMOS protection can be determined by a SPICE simulation so that the peak ESD performance is obtained for a specific Cdd window.

In practice, we would like to have a PDNMOS having a high ESD performance for a wide range Vdd chip capacitance. To that end, we can first increase the size of PNPs or the value of the resistor to improve the ESD performance for a very small Vdd chip capacitance (<10 pF), by significantly raising the protection NMOS gate voltage during ESD events. Secondly, it is necessary to use additional clamping diodes to clamp the protection NMOS gate voltage to ensure the NMOS gate voltage would not be pulled too high even for the case of a large Vdd chip capacitance.

The choice for the clamping diodes may be either p-n type diodes in nwell or diode-connected NMOSs (with gate and drain tied together), depending on technology and circuit application. In this study, a diode-connected NMOS is used in PDNMOS protection in order to minimize silicon area. Figure 10 is a full circuit schematic of the PDNMOS protection with a diode-connected NMOS clamping for design implementation and SPICE simulation.

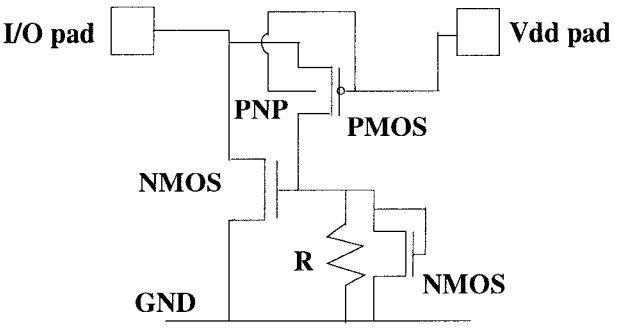

Figure 10. A completed schematic of the PDNMOS. The LNPN is not shown in the figure.

A SPICE simulation of a PDNMOS shown in figure 11 indicates that the Vg is 1.8 V with an NMOS clamp, and 4.5 V without the clamp, when the pad voltage develops to 8 V during an ESD event. Hence, the figure shows that the clamp limits the Vg. Note that, in this technology, whenever the pad voltage exceeds 8 V, LNPNs would turn on to conduct the ESD current and the pad voltage will be clamped at around 8-9 V, which is not shown in the simulation results since the parasitic LNPN action was not included in the simulation.

Figure 12 is the layout of an optimized PDNMOS, which is integrated with a 72 um x 72 um bond pad. In order to eliminate SCR action in PDNMOS, a large

space L (figure 4) between the PNPs and NMOSs was chosen in a PDNMOS layout, and a p+ guardring was employed to isolate the PNPs from the NMOS.

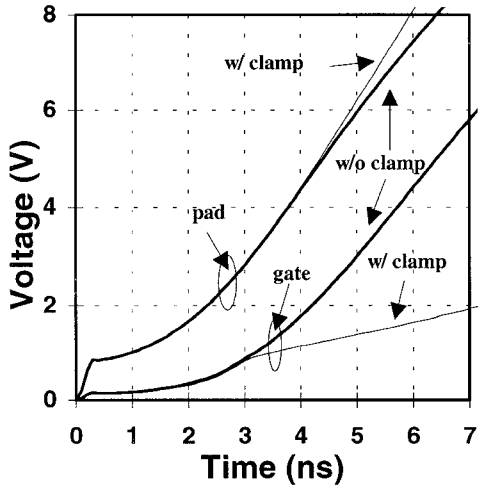

Figure 11. SPICE transient simulation of an I/O pad and gate voltage of a PDNMOS under a 2 kV ESD event for cases of with/without a NMOS clamp. A 200 pF Cdd value was used in simulation. The size of the protection NMOS is 720/0.72 um, The size of PMOS is 72/0.72 um, the size of NMOS clamp is 108/0.72 um, and the R is 15 kΩ.

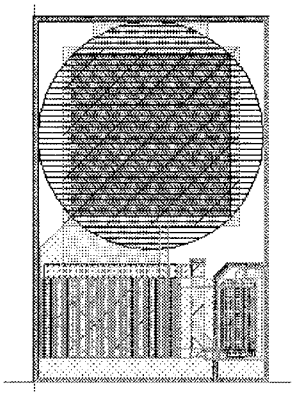

Figure 12. The layout of PDNMOS.

III-D. PDNMOS protection for power supply pins

The PDNMOS is a three terminal circuit. Operation of a PDNMOS protection requires the gate node (connection of the base of PNPs and the gate of PMOS), connected to a capacitor to provide the base current of PNPs. For input and output pin protection, a power supply Vdd parasitic capacitance is utilized in PDNMOS implementation. For the power supply pin protection, however, the PDNMOS requires at least two power supplies with the same voltage level in a chip design. For most of mixed signal and digital designs, they usually meet this requirement since mixed signal designs have analog and digital power supplies and digital designs have core and peripheral power supplies. Figure 13 is a block diagram for PDNMOS protections in I/O and two power supply pins (Vdd1 and Vdd2). The gate node of the Vdd1 PDNMOS protection needs to be connected to power supply Vdd2. Vice versa, the gate node of the Vdd2 PDNMOS protection can be connected to Vdd1.

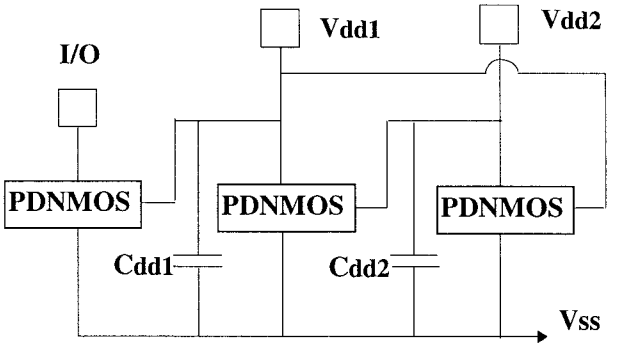

Figure 13. Block diagram of the PDNMOS implementation for a multiple power supply chip.

The implementation of PDNMOS in power supply would, together with the Vdd capacitance, provide additional base current for an I/O PDNMOS. The requirement of a power supply having some capacitance to provide base current for an I/O PDNMOS operation is thus relaxed. It is worth pointing out that, even though the Vdd1 and Vdd2 are connected together through PDNMOS devices as shown in figure 13, the base-emitter diodes of PNPs between two power supplies would suppress noise injection between two power supplies thus improve the noise immunity between power supplies.

IV. Experimental Results in a Silicided Process

PDNMOS protection scheme was initially developed and successfully implemented in submicron non-silicided CMOS processes. Minimum Contact to poly Gate Spacing (CGS) can be used in the design which makes the PDNMOS a good candidate for a submicron silicided CMOS process. The PDNMOS design methodology developed for non-silicided processes has been applied to a 0.8 um silicided process. The PDNMOS protection shown in figure 10 was adapted in the silicided process. The size of the protection NMOS is 1000/0.8 um, the PMOS is

100/0.8 um, the NMOS clamping diode is 150/0.8 um, and the value of the nwell resistor is 15 kΩ.

The TLP results of this PDNMOS are shown in figure 14. It is clearly seen that the LNPN turns on and conducts most current up to over 2.8 A at a 10V pad voltage. Thus the 1000/0.8 um protection NMOS of the PDNMOS results in an effective It2 of 2.8 mA/um ~ 3.2 mA/um. An I-V curve of a 50/0.8 um

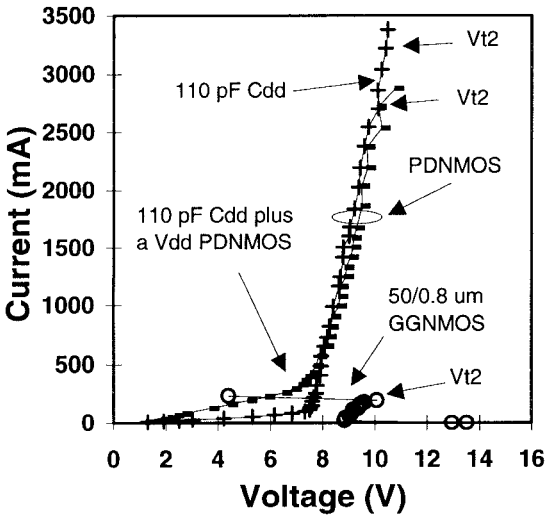

Figure 14. I-V curves of an I/O PDNMOS fabricated in a 0.8 um silicided CMOS process for a 110 pF Cdd power supply with/without a PDNMOS protection. The curves show that Vdd PDNMOS does provide a large base current to help the I/O PDNMOS. The I-V curve of a 50/0.8 um GGNMOS in this process is also shown in the figure for comparison. The size of the protection NMOS is 20 x 50/0.8 um, the PNP is 100/0.8 um, the R is 15 kΩ, the NMOS clamp is 150/0.8 um.

GGNMOS is also shown in the figure. The It2 of the 50/0.8 um NMOS is about 200 mA (4 mA/um). If each 50 um finger of the PDNMOS handles 200 mA, the measured effective It2 of the PDNMOS indicates that about 70 ~ 80% of fingers must be conducting. Figure 14 also shows that the PDNMOS protection circuit with a second PDNMOS connected between Vdd and Vss has a larger MOS current than that without the second PDNMOS before the LNPN triggering. Hence, a lower R and a smaller size of PNP can be used in an I/O PDNMOS design if the second PDNMOS is implemented into the power supply. This would reduce the loading effect on the I/O pad.

Similar to the I-V curve (figure 7) of the 0.72 um nonsilicided process, the dramatic increase in current in figure 14 after 7.5 V indicates the trigger of LNPN in PDNMOS. Before the LNPN being triggered, all the ESD current is conducted by a combination action of NMOS, VPNP, and LPNP (or a diode to Vcc) devices. However, the current level of the combination action is well below the current level conducted by LNPN as shown in the figure. The combination current would increase with the increase of the chip Vcc capacitance.

The HBM results for the PDNMOS for different chip capacitance are shown in figure 15. The PDNMOS design was optimized for a small Cdd. A high 9 kV ESD performance for a 10 ~ 50 pF chip capacitance is obtained in this process.

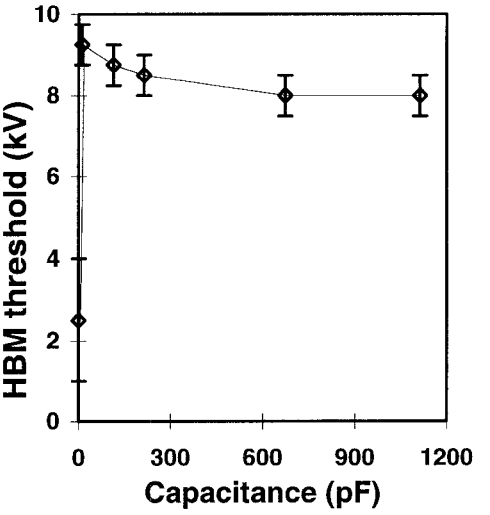

Figure 15. HBM ESD performance of the PDNMOS as function of Cdd for a 0.8 um silicided CMOS process. The size of the protection NMOS is 1000/0.8 um.

Figure 16 is a picture of a typical PDNMOS ESD failure. Damage locations were scattered at different NMOS fingers. This is a strong proof that most

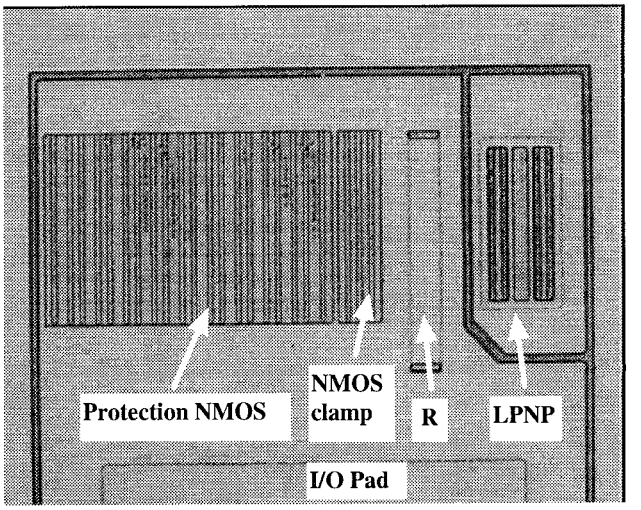

Figure 16. FA picture of a PDNMOS. ESD damages were seen in most fingers of the protection NMOS.

fingers turn on during an ESD event. Figure 17 is a SEM picture of some damage inside figure 16. A drain-source flash-over failure mode is clearly shown in the picture. The failures are due to the failures of parasitic LNPNs of NMOS fingers.

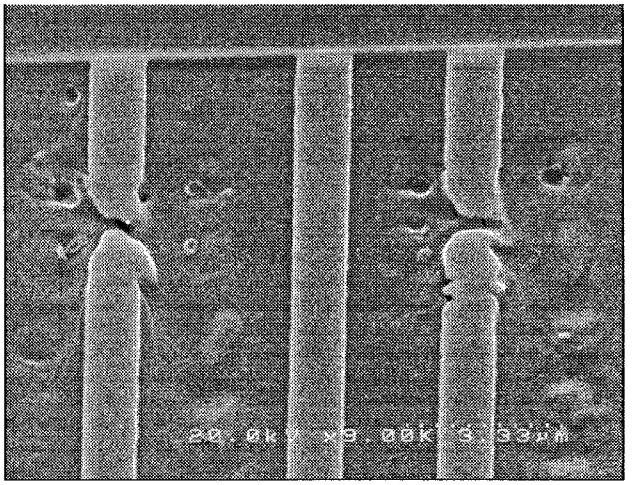

Figure 17. SEM picture of the PDNMOS of figure 16, showing the local drain-source damages in fingers.

V. Discussion

High ESD performance of PDNMOS protection scheme was demonstrated in both 0.72 um nonsilicided and 0.8 um silicided processes. Based on the methodology developed here, the ESD performance of PDNMOS scales with the size of the protection NMOS. For a given ESD protection level, the size of the protection NMOS would be determined by It2 value for a specific process. A low (or high) It2 in a process leads to a large (or small) required NMOS size. Worst case design, however, should assume that about 75% of the multi-finger device turns on.

The nature of relatively low NMOS It2 in CMOS processes, compared with that of BSCR and NPN BJT processes, leads to a relatively large size of a protection NMOS in a gate driven ESD protection scheme. Therefore, a relatively large parasitic loading effect on an I/O pad would resulted. In the PDNMOS protection scheme, the load is mainly contributed from the parasitic capacitance of the protection NMOS and the LPNP. For a given process It2 value, the size of the NMOS is then determined for a required ESD level. The small size of LPNP can be used to reduce the load, at the cost of increasing the value of gate resistor in PDNMOS. It should be noted that, in high speed applications, the value of the gate resistor should not be too large. Because of a gate coupling effect during fast transient, a large value of gate resistor would turn on the protection NMOS and result in the ESD protection distorting normal circuit operation. Thus caution should be applied in the design of the resistor value. For a given technology, the value of the resistor and the size of LPNP can be optimized by SPICE simulations for both cases of normal circuit operation and ESD event. SPICE would also simulate the leakage current caused by a fast transient signal in input and output pins.

Using a gate driven NMOS ESD protection scheme in submicron, it is necessary to characterize the process ESD parameters such as Vt1, Vt2, and It2, etc. The value of Vt2-Vt1 sets the "process design margin" (figure 6), determining the validation of the protection in a given process. The roll-off point of It2 vs gate bias curve (figure 9) sets the "gate voltage design margin" (figure 6) for the gate driven NMOS protection scheme. A small "design margin" (either process or gate voltage) limits the NMOS gate driven protection application in the process.

The new design of PDNMOS ESD protection scheme not only provides the necessary gate driven effect on the protection NMOS device, but also supplies a local substrate bias to the NMOS device through a parasitic VPNP action. The local substrate bias would lower the Vt1 value further, in addition to the low Vt1 value resulted from the NMOS gate driven effect. The local substrate bias would also improve the It2 value in a given process.

The PDNMOS protection circuit has been used for CMOS digital and analog pins such as input, output, and power supply in mixed-signal chips in production. ESD protection levels of > 4 kV HBM, > 350 V MM, and > 1.5 kV CDM have been obtained in production for a mixed-signal IC with a small chip size of 95 mil x 136 mil. In the production line tests, all pins are subjected to ESD stress with different pin combination, according to the ESD test standard. Functional tests are performed pre- and post-ESD stressing to ensure that the leakage current, parametric data, and functionality would meet design specifications in all operational voltage and temperature range.

VI. Conclusions

This paper has described the design methodology for optimizing gate driven NMOS ESD protection designs. A new gate driven NMOS scheme for submicron CMOS processes has been presented. SPICE simulation was used to optimize the design for

ESD performance. Experimental results of TLP, ESD test, and FA consistently indicate efficient finger turn-on of the protection NMOS. High ESD performance of this PDNMOS protection scheme has therefore been demonstrated in this work.

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