Driving a capacitive load without dissipating fCV^2

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Abstract

We describe a driver for capacitive loads that dissipates considerably less power than fCV^2. We give a design procedure for the driver that minimizes the dissipation. Measurements on an experimental chip support the theoretical results.

1 Introduction

Output pad drivers often contribute a large part of the total power dissipation of a chip, due to the large capacitive load they drive. Here, we describe a driver capable of significant reduction of this dissipation, for given values of voltage swing, load capacitance, and switching frequency, without performance loss. We accomplish this by *stepwise charging* [1], an inductor-free form of adiabatic charging [2,3,4].

2 Stepwise charging

Figure 1 (a) shows a capacitance being charged from a bank of voltage supplies with uniformly distributed voltages. To charge the load, each supply is switched in briefly in ascending order, until the load has reached the corresponding voltage. Each supply then injects a charge packet of size q_{inj}:

$$q_{\text{inj}} = C_L(V_i - V_{i-1}) = C_L(V/N) \qquad (1)$$

During discharging (when supplies are switched in in opposite order), each supply except V_N receives one charge packet, and one packet is dumped to ground. The net effect over one complete cycle is to inject one packet at voltage V_N, and remove one packet at voltage 0. Since the initial and final states are identical, the total dissipated energy is equal to the net injected energy:

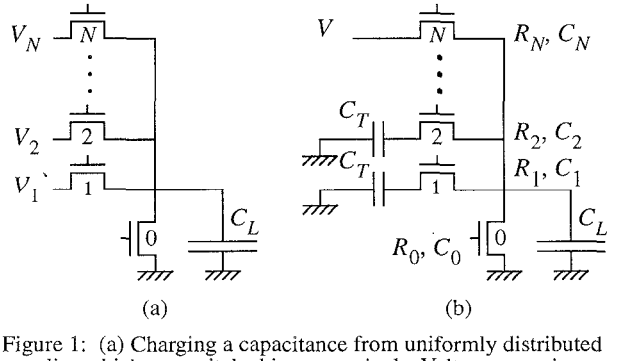

Figure 1: (a) Charging a capacitance from uniformly distributed supplies which are switched in successively. Voltages are given by $V_i = iV/N$. Switches may be n- or p-channel devices. (b) All supplies but one are replaced with large "tank" capacitors, C_T. The C_i, R_i pairs are the gate capacitance and channel resistance of each switch device.

$$E_{\text{diss}} = E_{\text{inj}} = q_{\text{inj}} V = (C_L V^2)/N \qquad (2)$$

Thus, charging through N steps instead of a single step reduces the energy dissipation by a factor of N, and $N = 1$ corresponds to the conventional case.

The use of multiple supply voltages for a chip is undesirable for practical reasons. Fortunately, simple capacitors may be substituted for all but one of the supplies in Figure 1 (a): during a switching cycle, no supply except V_N provides any net charge to the circuit. The circuit shown in Figure 1 (b) will behave identically. No additional circuitry is needed to maintain the desired voltages on the tank capacitors; the circuit is *self-stabilizing* [1].

3 Design of a driver using stepwise charging

Equation (2) indicates that dissipation decreases monotonically with increasing N. N cannot, however, usefully be made very large, because all the switches need to be operated, which itself causes dissipation. The energy required to drive each switch depends on the width of the device, which should be just enough to allow the charging to "complete" before the next step commences. For a given total charging time T, there is an optimal number of steps and a set of optimal device sizes which lead to minimal total dissipation.

Consider the circuit in Figure 1 (b). Assume the gates of the switch devices are driven conventionally. The load is charged and discharged once. The energy needed to drive the gates of the switch devices is:

$$E_{\text{sw}} = \left(\sum_{i=1}^{N} C_i + \sum_{i=0}^{N-1} C_i\right) V^2 \qquad (3)$$

Allot each step one Nth of the total charging time T. Then:

$$T/N = mR_iC_L \qquad (4)$$

Here, m is the number of RC time constants spent waiting for each charging step to "complete." Suitable values range from 2 to 4. We see from (4) that all the switch devices should have equal on-resistance. Selecting the on-resistance of device i by tuning the width affects the gate capacitance:

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$$\rho_i = R_i C_i \tag{5}$$

ρ_i is a quality measure of the switch. It varies with i, since the bulk-to-channel and gate-to-channel voltages are different for different switches. Combine (3), (4), and (5):

$$E_{sw} = \frac{Nm}{T}\left(\sum_{i=1}^{N}\rho_i + \sum_{i=0}^{N-1}\rho_i\right)C_L V^2 \tag{6}$$

Introduce $\bar{\rho}$, a weighted average of ρ_i for all switches:

$$\bar{\rho} = \frac{1}{2N}\left(\sum_{i=1}^{N}\rho_i + \sum_{i=0}^{N-1}\rho_i\right) \tag{7}$$

If N is large, $\bar{\rho}$ is close to the unweighted average of ρ over the entire voltage range. Combine (2), (6), and (7):

$$E_{tot} = \left(\frac{1}{N} + 2N^2 m\frac{\bar{\rho}}{T}\right) C_L V^2 \tag{8}$$

The N that minimizes E_{tot} is given by:

$$N_{opt} = \sqrt[3]{\frac{T}{4m\bar{\rho}}} \tag{9}$$

The corresponding energy dissipation is:

$$E_{opt} = \frac{3}{2}\sqrt[3]{\frac{4m\bar{\rho}}{T}} C_L V^2 \tag{10}$$

By using the number of stages given by (9), the designer can minimize the power dissipation of the driver. A lower N will still give a considerable improvement over the conventional case; $N = 2$ already gives almost 50% reduction. The on-resistance of each switch is then given by (4). The corresponding gate capacitance, and thereby the device width, is given by (5). The values of ρ for a certain technology can be found by circuit simulation or by measuring the on-resistances of test devices of known widths.

4 Experimental chip

We have designed, fabricated, and tested a simple stepwise driver that charges a load capacitance of 880 pF from 0 to 5 volts in 500 ns. We used the MOSIS 2μ CMOS process with a $\bar{\rho}$ of approximately 40 ps. A conservative choice for m resulted in the selection of $N = 6$.

The experimental driver is shown in Figure 2. When the input is stable, the load is held high (low) by switch 6 (0). When the input changes, a finite state machine (FSM) turns on the switches in succession. The V_4 switch is actually two devices: a p-channel device used to discharge the load from V_5 and an n-channel device for charging up from V_3 (a switch of either type would have to be very wide to cover the entire voltage range from V_3 to V_5 adequately). An additional input, Fast/Slow, is used in the output logic of the FSM to select between using the stepwise mode of the driver and just turning on the top (bottom) device immediately when the input goes high (low).

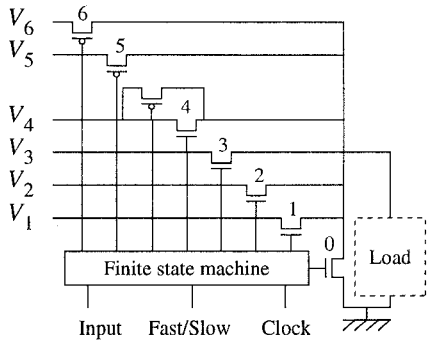

Figure 2: Implementation of experimental driver. V_6 is the "real" supply voltage; $V_1 - V_5$ are provided by tank capacitors.

The energy dissipation per charge-discharge cycle given by the equations is 4.44 nJ, an improvement by 80% over the 22 nJ of the conventional case. Hspice simulation of the extracted layout comes out slightly worse, at 5.1 nJ and 77%. For the actual circuit, the measured supply current reduction when the stepwise mode is selected with the Fast/Slow signal corresponds to a dissipation decrease of 16.1 nJ per charge-discharge cycle, or 73% of 22nJ.

5 Acknowledgments

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6 References

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