

Analysis and Modeling of On-Chip High-Voltage Generator Circuits for Use in EEPROM Circuits

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Abstract—Most of the presently available EEPROM circuits feature 5-V-only operation and therefore incorporate on-chip high-voltage generators. In spite of the importance of these latter circuits, a thorough analysis of the circuit has not been presented. In this paper the characteristics of the voltage multiplier circuit are thoroughly analyzed and modeled. The results obtained from this analysis are fully confirmed by experiments. The degradation characteristics of the circuit are discussed and its capability to compensate for nonvolatile memory degradation is shown.

I. INTRODUCTION

SINCE the introduction of the first floating-gate type EPROM devices, the number and diversity of non-volatile memory circuits, EPROM and EEPROM, has been steadily growing. One of the objectives of this evolution has been to make the nonvolatile memory circuits as easy to use as the static RAM memories. It was quickly recognized that the use of a second voltage supply, required for the programming of the devices, is unacceptable. Therefore, on-chip high-voltage generators are increasingly incorporated on the memory chip and most of the presently available EEPROM devices exhibit a 5-V-only operation (except for some very high-speed products) [1], [2]. Most high-voltage multiplier circuits used are based on the circuit proposed by Dickson in 1976 [3]. This circuit makes use of capacitors which are interconnected by diodes and coupled in parallel with two noninterleaving clock signals. The circuit is rather insensitive to parasitic capacitances. A practical implementation of the circuit uses MOS transistors to accomplish the diode function [2], [3]. This implies, however, some deviations from the simple model as proposed by Dickson.

Although the voltage multiplier circuit is widely used, the description of the circuit in literature has been restricted to the basic operating principle of the diode-capacitor chain proposed by Dickson [3] and a thorough and systematic treatment has not been presented. In this paper the voltage multiplier circuit realized with transistors

is thoroughly analyzed and a complete model is proposed. Also the degradation features of the circuit and its implication on EEPROM endurance are studied. Experimental results confirm the validity of the proposed model.

II. MODEL FOR THE VOLTAGE MULTIPLIER

A. Dickson Voltage Multiplier Circuit with Diodes

The basic electrical circuit of the high-voltage generator is shown in Fig. 1. The voltage multiplier as presented by Dickson [3] uses diodes to separate the different capacitors by which the clock pulses are coupled to the nodes of the chain. The output voltage of the circuit is calculated in [3]; the results are resumed below. The output voltage is calculated as

$$V_{\text{out}} = V_{\text{in}} - V_d + n \cdot [V_{\phi}' - V_d - V_l] \quad (1)$$

where

- V_{in} input voltage of the circuit,
- V_{ϕ}' voltage swing of node i due to capacitive coupling with the clock signal,
- V_d voltage drop over a diode, and
- V_l voltage drop due to the output current I_{out} which is delivered by the multiplier.

Introducing

$$\begin{cases} V_{\phi}' = V_{\phi} \frac{C}{C + C_s} \\ I_{\text{out}} = f \cdot (C + C_s) \cdot V_l \end{cases} \quad (2)$$

with C the clock coupling capacitance, C_s the stray capacitance at each node, V_{ϕ} the clock signal amplitude (see Fig. 1), and f the clock frequency, results in

$$V_{\text{out}} = V_{\text{in}} - V_d + n \cdot \left[V_{\phi}' - V_d - \frac{I_{\text{out}}}{f \cdot (C + C_s)} \right] \quad (3)$$

There will be a voltage ripple at the multiplier output due to the discharging of the output capacitance C_{out} by the

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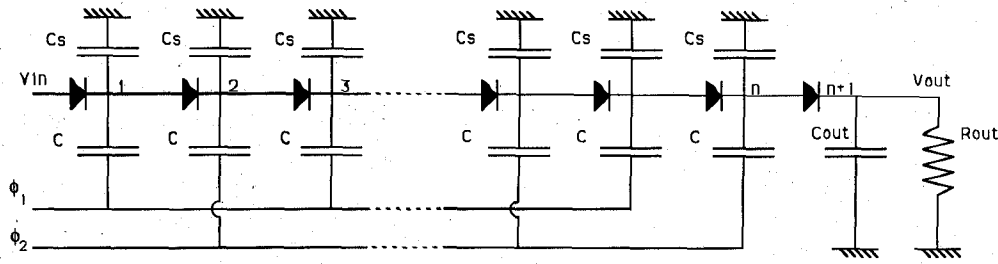


Fig. 1. High-voltage generator with capacitors in parallel with diodes [3]. ϕ_1 and ϕ_2 are two noninterleaving clock signals. C_s is the stray capacitance at each node.

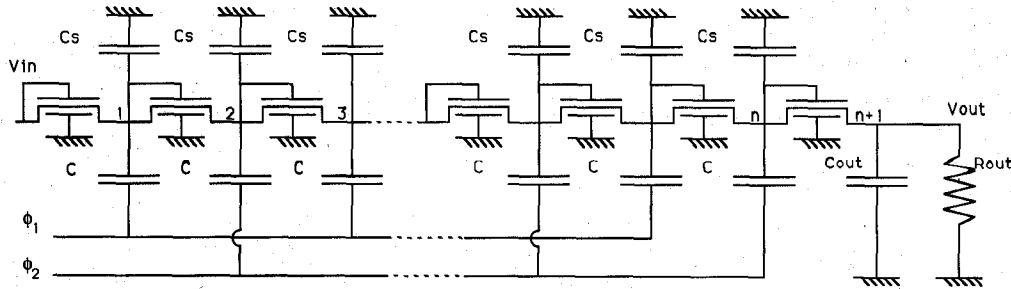


Fig. 2. High-voltage generator with capacitors in parallel with transistors.

load resistor R_{out} (see Fig. 1). Besides this voltage ripple due to the load resistor, there will be an additional ripple component due to the capacitive coupling from the clocks through the diodes.

Based on (3), an equivalent circuit for the voltage multiplier can be derived. Indeed, (3) can be written as

$$V_{out} = V_{eq} - R_{eq} \cdot I_{out} \quad (4)$$

with

$$V_{eq} = V_{in} - V_d + n \cdot [V'_\phi - V_d] \quad (5)$$

$$R_{eq} = \frac{n}{f \cdot (C + C_s)} \quad (6)$$

In this implementation of the multiplier circuit the output voltage keeps increasing with increasing number of stages and theoretically any output voltage can be generated.

In practical implementations the capacitors are formed by two polysilicon layers. In most VLSI processes, however, it is difficult to implement isolated diodes, although polysilicon diodes using both n^+ and p^+ doped polysilicon have been proposed and used before [4]. In the past, some nonvolatile memory products were developed in a p-well process in which the whole substrate could be brought to the high programming voltage [5] such that the drain-p-well junction of the nMOS transistor could be used as diode. However, this is unacceptable if the high voltage is generated on chip. The most common approach is to substitute the diodes in the multiplier circuit by MOS transistors with a drain-gate contact as shown in Fig. 2. An important difference with a voltage multiplier that uses diodes is that now the voltage drop over the "diode" is no longer a constant. Indeed, in this case, V_d equals the threshold voltage of the transistor, which is influenced by

the source-substrate voltage through the so-called body effect. Dickson [3] already pointed to this problem, and in order to account for it he assumed a mean value for the threshold voltage over the whole range of voltages that occur in the multiplier circuit. This mean value was chosen somewhat arbitrarily. In the next section another, more accurate approach is proposed.

B. The Body Effect

The body effect occurs when a source-substrate voltage is applied. The voltage across the reverse-biased source-substrate junction will increase the threshold voltage of the transistor. The dependence of the threshold voltage on the source-substrate voltage is expressed as [6]

$$V_t = V_{t0} + K_2 \cdot [\sqrt{V_{bs} + 2\phi_f} - \sqrt{2\phi_f}] \quad (7)$$

where V_{t0} is the threshold voltage if no substrate bias is applied, $2\phi_f$ is the band bending in the substrate needed to invert the silicon surface, and

$$K_2 = \frac{\sqrt{2q\epsilon_{Si}}}{\epsilon_{SiO_2}} \cdot \sqrt{N_b} \cdot t_{ox} \quad (8)$$

These formulas are for the case of a uniformly doped substrate.

Most VLSI processes make use of ion implantations to adjust the threshold voltage of the transistor to the desired value and to improve the punchthrough features of the transistors. Consequently, the gate area of a transistor is certainly not uniformly doped.

It has been shown that the transistor characteristics can be modeled by making use of two different K_2 and V_{t0} values [7]. The surface doping concentration is determining

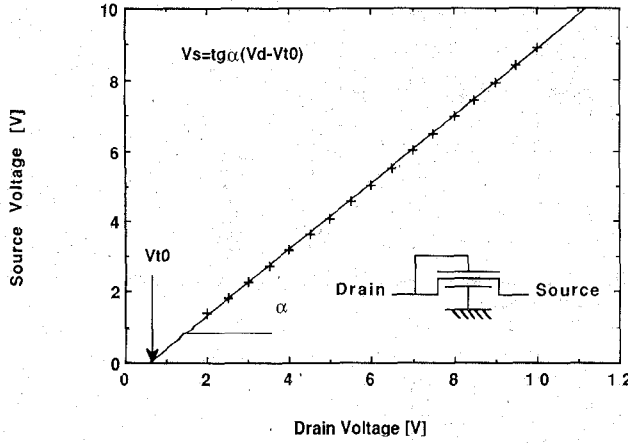


Fig. 3. Source voltage versus drain voltage of a transistor used as diode in the circuit. + : measured values; - : interpolating line.

the values for K_2 and V_{t0} for the low-substrate-bias range. A second pair of K_2 and V_{t0} values corresponds to the substrate doping concentration which is assumed to be constant. These values can be used in the high-substrate-bias range. As the transistors in a voltage multiplier circuit will normally operate with a substrate bias voltage larger than 3 V, the second pair of K_2 and V_{t0} values should be used. This will be the case for most VLSI processes, where the implantations are aimed at influencing the surface doping level only.

The threshold voltage, as expressed by (7), is not very practical for use in calculations. Therefore an approximation that is easier to handle is needed. Fig. 3 shows the voltage measured at the source of a transistor, used as a diode (see inset of Fig. 3) as a function of the drain voltage, when the source of the transistor is connected to a very high impedance. For transistors with a small body effect, this dependence can be approximated by a straight line. If there were no substrate bias influence, the source voltage would follow a straight line with slope 1. For a transistor with a small K_2 value, the relationship can be approximated by a line with a slope somewhat less than 1:

$$V_s = tg\alpha \cdot (V_d - V_{t0}). \quad (9)$$

This approximation is fairly good if the considered substrate bias range is small and the value of K_2 is small.

When considering the transistors in a voltage multiplier circuit, the substrate bias is limited to the output voltage of the circuit (≈ 20 V). The K_2 value will be rather small in view of the fact that the advanced memory technologies make use of a decreasing gate oxide thickness and that n-well processes, in which the nMOS transistors are formed in a lightly doped substrate (and not in a highly doped well), are preferred. This justifies the use of the approximation proposed above.

C. Dickson Voltage Multiplier Circuit with Transistors

Based on the approximation for the body effect, the behavior of the Dickson voltage multiplier circuit with transistors can be described. The output voltage as a

function of the input voltage, the clock amplitude, and the output current will be derived starting from Fig. 4. This figure again shows the source voltage as a function of the drain voltage for a transistor that operates as a diode (solid line A). It is assumed that the multiplier circuit is in steady state, i.e., that the delivered output current is constant. The symbol V_{il} refers to the voltage at node i when the corresponding clock pulse is at its low level, whereas V_{ih} refers to the voltage at node i when the corresponding clock pulse is at its high level.

The voltages on the successive nodes are now derived as follows: in Fig. 4, a line B is added parallel to the line representing the source-drain voltage relationship, but shifted upwards by an amount

$$V'_\phi - \frac{I_{out}}{f \cdot (C + C_s)} = V'_\phi - V_l. \quad (10)$$

On this line, the V_{ih} voltages can be found. V_{in} is the input voltage of the first transistor. The output voltage V_{il} of this transistor (at node 1) can be found as the ordinate of line A where its abscissa is V_{in} . When the clock at node 1 goes up, node 1 is pushed toward V_{ih} , which can be found on line B. V_{ih} is again the input voltage of the transistor between nodes 1 and 2. Therefore, V_{ih} can be projected on the x-axis by making use of the bisector of the $V_s - V_d$ axes (dotted line C). Now the procedure can restart, with V_{2l} on line A and V_{2h} on line B, which is again the input voltage of the third stage and so on.

This procedure can be expressed in formulas. For example, for V_{2l} one finds

$$V_{il} = tg\alpha \cdot (V_{in} - V_{t0}) \quad (11)$$

$$V_{ih} = V_{il} + V'_\phi - \frac{I_{out}}{f \cdot (C + C_s)} \quad (12)$$

$$V_{2l} = tg\alpha \cdot (V_{ih} - V_{t0}) \\ = tg\alpha \cdot \left(V_{il} + V'_\phi - \frac{I_{out}}{f \cdot (C + C_s)} \right) - tg\alpha \cdot V_{t0}. \quad (13)$$

One can find the difference between V_{ih} and V_{in} in Fig. 4 as the distance labeled a between the dotted line D, parallel to the bisector C at a distance $V'_\phi - V_l$, and the solid line A. Therefore the relation between V_{il} and V_{2l} can be written as

$$V_{2l} = V_{il} + a \cdot tg\alpha. \quad (14)$$

The threshold voltage of each transistor can be found as the difference between the bisector (dotted line C), which gives the input voltage of each transistor, and the solid line A, which gives the corresponding output voltage. As an example, V_{il} is given by

$$V_{il} = V_{in} - V_{il}. \quad (15)$$

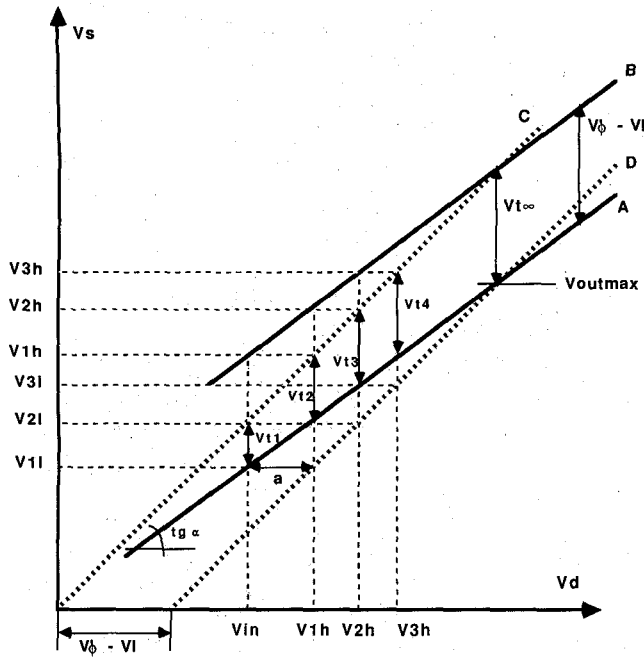


Fig. 4. Correlation between the voltages at the nodes of the voltage multiplier circuit with capacitors in parallel using transistors.

From Fig. 4 it can be found that

$$a = V_{\phi}' - \frac{I_{out}}{f \cdot (C + C_s)} - V_{t0} \quad (16)$$

This, of course, can also be calculated using (11), (13), and (15). In the same way, V_{3l} can be calculated out of V_{2l} and so on. In general, one finds

$$V_{il} = V_{t0} + \sum_{j=1}^{i-1} a \cdot tg^j \alpha = V_{t0} + a \cdot tg \alpha \cdot \frac{1 - tg^{i-1} \alpha}{1 - tg \alpha} \quad (17)$$

As V_{out} can be considered as $V_{(n+1)l}$, it is found that

$$V_{out} = V_{t0} + \left(V_{\phi}' - \frac{I_{out}}{f \cdot (C + C_s)} - V_{t0} \right) \cdot tg \alpha \cdot \frac{1 - tg^n \alpha}{1 - tg \alpha} \quad (18)$$

If the threshold voltage of the first transistor is substituted by

$$V_{t1} = V_{in} - V_{t0} = (1 - tg \alpha) \cdot V_{in} + tg \alpha \cdot V_{t0} \quad (19)$$

the output voltage V_{out} becomes

$$V_{out} = tg^{n+1} \alpha \cdot V_{in} - tg \alpha \cdot \frac{1 - tg^{n+1} \alpha}{1 - tg \alpha} \cdot V_{t0} + \left(V_{\phi}' - \frac{I_{out}}{f \cdot (C + C_s)} \right) \cdot tg \alpha \cdot \frac{1 - tg^n \alpha}{1 - tg \alpha} \quad (20)$$

As $tg \alpha < 1$, (18) clearly indicates that due to the body effect, the output voltage is lower than if diodes were used in the circuit. The output voltage remains linearly dependent on the input voltage V_{in} , the clock signal V_{ϕ}' , and the delivered output current I_{out} . Therefore the equivalent

circuit is the same as for the multiplier built up with diodes, but the value of the equivalent elements is somewhat different. Not only the output voltage, but also the equivalent resistance of the chain will be lower than that for a chain constructed with genuine diodes. Equation (18) shows that the equivalent resistance of the voltage multiplier is

$$R_{eq} = \frac{1}{f \cdot (C + C_s)} \cdot tg \alpha \cdot \frac{1 - tg^n \alpha}{1 - tg \alpha} \quad (21)$$

In contrast to the ideal circuit, the output voltage of the multiplier circuit is also limited, irrespective of the number of stages and the input voltage used. It follows indeed from (18) that the maximum output voltage that can be reached ($n = \infty$) is given by

$$V_{outmax} < V_{t0} + (V_{\phi}' - V_{t0} - V_{t0}) \cdot \frac{tg \alpha}{1 - tg \alpha} \quad (22)$$

$$= (V_{\phi}' - V_{t0} - V_{t0}) \cdot \frac{tg \alpha}{1 - tg \alpha} \quad (23)$$

This voltage can be found in Fig. 4 as the intersection of lines A and D. As can be seen in Fig. 4, at this output voltage the threshold voltage of the last, isolating transistor, indicated by V_{t0} , becomes equal to the voltage swing of each node, i.e., $V_{\phi}' = V_{t0}$.

If the transistors do not suffer from the body effect, i.e., $tg \alpha = 1$, the formulas reduce to those derived by Dickson for a voltage multiplier with diodes (see previous section). Indeed, using de L'Hôpital's rule for limits, one finds

$$\lim_{tg \alpha \rightarrow 1} tg \alpha \cdot \frac{1 - tg^n \alpha}{1 - tg \alpha} = \lim_{tg \alpha \rightarrow 1} \frac{1 - (n+1) \cdot tg^n \alpha}{-1} = n \quad (24)$$

The influence of the body effect becomes more important the more stages the voltage multiplier contains.

There will be a voltage ripple V_r at the output of the high-voltage generator with transistors due to the discharging of the output capacitor C_{out} by the load resistor R_{out} . In a voltage multiplier circuit with transistors, there will be a capacitive coupling from the clocks:

$$V_{bt} = \frac{C_{gs}}{C_{gs} + C_{out}} \cdot V_{\phi}' \quad (25)$$

with C_{gs} being the gate-source capacitance. Also for multiplier circuits with transistors, this ripple voltage is normally small. In the derivation of the formulas, it has been assumed that the capacitors of the chain are completely charged and discharged by the transistors.

D. Limitations of the Model

The model is based on the approximation of the threshold voltage substrate bias relationship by a straight line. The error, introduced by this approximation, will of course

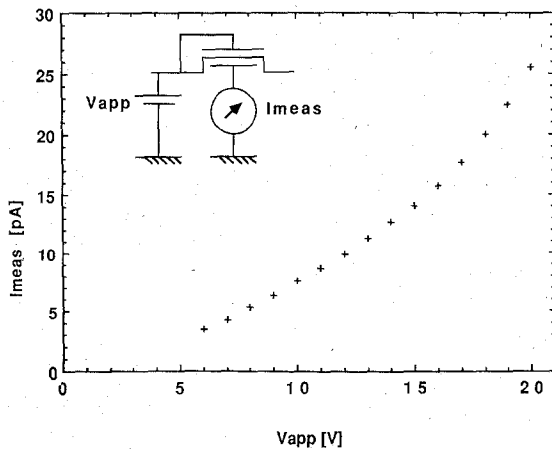


Fig. 5. Measured leakage current (substrate current) as function of drain voltage for a transistor used in the voltage multiplier circuit; the measurement setup is shown in the inset.

be smaller if a smaller range of output voltages is considered.

A first limitation stems from the assumption made in Section II-B that all transistors in the multiplier circuit will operate with a substrate bias of at least 3 V. This assumption implies that the input voltage V_{in} of the charge pump should be larger than $(3 V + V_{d1})$. For most practical realizations of the circuit, 3 V is a fairly safe limit. In the experimental data further on, no input voltages smaller than 2 V will be used.

Leakage currents of any nature will also cause deviations from the proposed model. Junction leakage currents from the drain and source of the transistors are possible. Fig. 5 shows the leakage current for a measurement setup as shown in the inset, obtained for the process to be discussed in the next section. The leakage current remains small: at 20 V a substrate current less than 30 pA is measured. This rather low value is explained by the special conditions under which the transistors are operating. Source and drain junctions are at a high voltage, but at the same time the gate is at a high voltage, thus preventing any gate-induced junction breakdown: the whole channel area of each transistor in the multiplier circuit will always be depleted (or inverted). Junction breakdown will therefore occur at the drain-substrate or source-substrate junction edges not covered by the gate. It is concluded that for output voltages up to 20 V, these junction leakage currents can still be neglected.

Another source of leakage is formed by the capacitors. In this voltage multiplier circuit, the capacitors have to withstand the voltages developed along the chain. As the capacitors are formed by two poly layers, the choice of the function of each poly layer is important. Indeed, oxides grown on polysilicon are known to conduct current more easily in one direction. Due to the asperities on the lower polysilicon layer, electron injection from this layer to the top electrode will be strongly enhanced [8]. If one wants to limit the leakage current through the capacitors (for a constant output voltage with time, see Section III-D), the

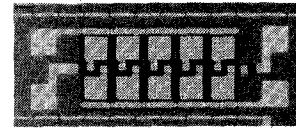


Fig. 6. Photograph of the voltage multiplier circuit with capacitors in parallel with ten stages.

top electrode of the capacitor must therefore be connected to the clock signal, in order to inhibit the enhanced electron injection. On the other hand, the leakage currents through the capacitors can be used to modulate the output voltage of the circuit (see Section III-D); in this case, the proposed model is of course no longer valid.

The range of output currents that the circuit delivers must also be limited. The model implicitly assumes that two successive transistors are never conducting at the same time. In order to fulfill this condition, the voltage drop due to the output current should be smaller than the voltage swing due to capacitive coupling with the clock signal, i.e.

$$\frac{I_{out}}{f \cdot (C + C_s)} < V_{\phi}' \quad (26)$$

This has to be kept in mind when the output voltage is measured as a function of output current. At larger output currents the behavior of the circuit can no longer be described by the proposed model. In fact, if a circuit with only a few stages is measured, and the input voltage V_{in} is sufficiently large ($V_{in} >$ the sum of the threshold voltages of the transistors of the chain), at large output currents I_{out} all transistors of the chain will conduct at the same time and the output voltage will only slightly decrease when the output current is further increased.

III. EXPERIMENTAL RESULTS ON THE MULTIPLIER USING TRANSISTORS

A. Devices

The multiplier circuit is realized in a 3- μ m n-well CMOS process. The gate oxide thickness of nMOS and pMOS transistors is 45 nm, and the polyoxide thickness is 67 nm. The capacitors in the multiplier circuit are formed between two polysilicon layers and the area of the capacitors is $10^4 \mu\text{m}^2$, which corresponds to a capacitance of 5.15 pF. Fig. 6 shows a photograph of the test circuit. The realized circuit contains ten capacitors. The top polysilicon plate of each capacitor is covered by aluminium such that this top plate can also be contacted. As this top plate is also connected to the gate of the nMOS transistors, this offers the possibility of applying the input voltage of the multiplier at any point, thus reducing the number of stages between the input voltage and the output voltage. Therefore, in this design it is possible to measure voltage multipliers with from one up to ten stages.

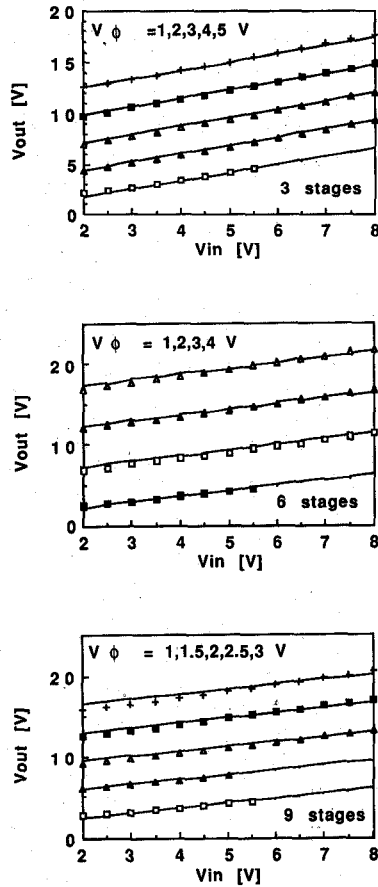


Fig. 7. Measured output voltage of three different voltage multiplier circuits, for different clock signal amplitudes. The clock signal frequency is 100 kHz. The lines indicate the output voltage as predicted by the proposed model.

B. Output Voltage of the Multiplier Circuit Delivering No Output Current I_{out}

The equivalent circuit of the voltage multiplier consists of a voltage source V_{eq} with a (high) internal resistance R_{eq} . If the circuit does not deliver an output current, the value of V_{eq} can be measured. In order to avoid any leakage current through the capacitors, the operating conditions were somewhat modified during this measurement. When carefully analyzing the circuit of Fig. 2, one observes that the output voltage does not depend on the absolute values of the pulse base and top levels of the clock signal, but only on its amplitude. This feature is used to avoid leakage currents by increasing the input voltage of the circuit and simultaneously increasing the pulse base level of the clock signal while keeping the clock amplitude constant. The pulse base level must, however, always remain smaller than $V_{in} - V_{nl}$ for the first transistor of the chain to remain in its normal operating mode. By this adjustment of the clock signal, the voltages across the capacitors can be considerably reduced, such that the capacitors no longer have to withstand such high voltages developed along the chain. This adjustment is only possible when the clock signal is externally applied and thus any pulse base level can be used; in real on-chip high-voltage generators this is, of course, no longer possible.

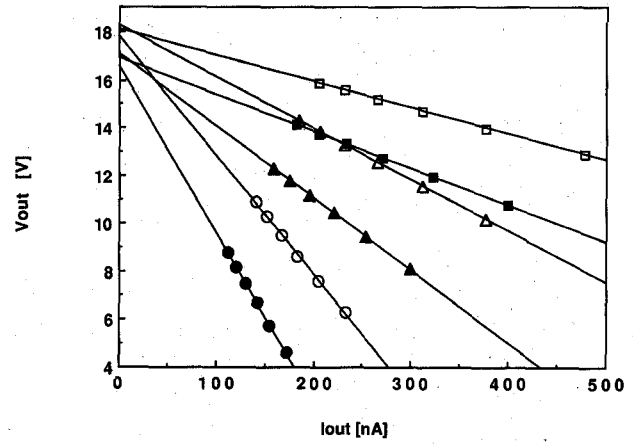


Fig. 8. Measured output voltage of six- and nine-stage voltage multiplier circuits as a function of the output current I_{out} , delivered to a load resistor for different clock signal frequencies. Characteristic numbers are given in Table I. (Six-stage multiplier: $V_{in} = 4$ V, $V_{\phi} = 4$ V: $\square$ 10 kHz, $\triangle$ 50 kHz, $\circ$ 100 kHz. Nine-stage multiplier: $V_{in} = 4$ V, $V_{\phi} = 3$ V: $\blacksquare$ 10 kHz, $\blacktriangle$ 50 kHz, $\bullet$ 100 kHz.)

Fig. 7 shows the measured output voltage V_{out} as a function of the input voltage V_{in} , for several clock amplitudes, for three high-voltage generation circuits with different numbers of stages. Also shown are the model predictions for the output voltage using (20), when a single value of V_{i0} ($= 0.77$ V) and $tg\alpha$ ($= 0.951$) is used. The figure clearly shows that the model predictions are very accurate, considering the fact that circuits with from three up to nine stages were used and thus a very wide range of output voltages is obtained.

C. Equivalent Resistance of the Circuit

The equivalent resistance of the circuit can be measured by monitoring the output voltage of the circuit, if the multiplier is loaded and thus has to deliver an output current I_{out} . Fig. 8 shows this output voltage as a function of the output current I_{out} for two different multiplier circuits and three clock signal frequencies. The slopes of the curves provide the equivalent resistance of the circuit. The extracted values for V_{eq} and R_{eq} together with the values calculated using $tg\alpha = 0.951$ and $V_{i0} = 0.77$ V are listed in Table I. The difference between the measured and the calculated values is caused by the resistance of the transistors of the chain. The resistance of these transistors has no influence if the chain is not delivering any current (as for the measurement results of Fig. 6); if the circuit is conducting current, there will be an additional voltage drop over the transistors that will reduce the output voltage (and thus V_{eq}) and the resistance of the transistors will add to the equivalent resistance of the circuit. This effect is larger for higher clock signal frequencies, since for higher frequencies less time is available for the transistors to conduct the current.

From (21) it follows that the equivalent resistance is inversely proportional to the clock signal frequency. If a voltage multiplier with a constant load resistance R_{out} is

TABLE I
EQUIVALENT CIRCUIT ELEMENTS FOR THE RESULTS OF FIG. 7

n	f [kHz]	Measured		Calculated	
		V _{eq} [V]	R _{eq} [MΩ]	V _{eq} [V]	R _{eq} [MΩ]
9	20	16.60	69.75	17.72	68.55
9	50	17.12	30.31	17.72	27.42
9	100	16.92	15.43	17.72	13.71
6	20	17.80	49.81	18.60	49.05
6	50	18.26	21.49	18.60	19.62
6	100	18.09	10.87	18.60	9.81

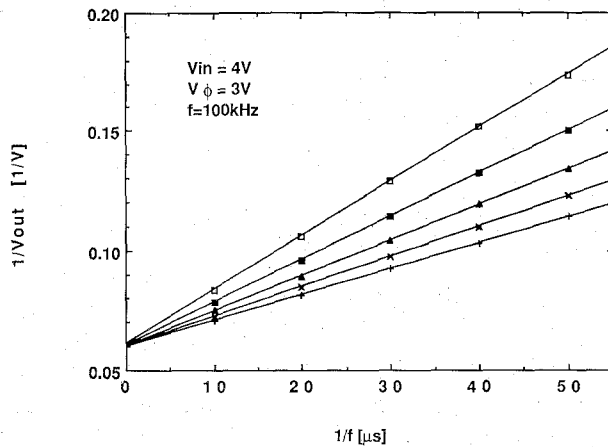


Fig. 9. Measured influence of the clock signal frequency on the output voltage of a nine-stage voltage multiplier circuit for the five different load resistance values given in Table II. Characteristic numbers are also given in Table II.

considered, the following equation can be derived:

$$\frac{1}{V_{out}} = \frac{R_{eq}}{R_{out} \cdot V_{eq}} + \frac{1}{V_{eq}} \quad (27)$$

or

$$\frac{1}{V_{out}} = \frac{\text{slope}}{f} + \text{intcp} \quad (28)$$

and

$$R_{eq} = \frac{R_{out} \cdot \text{slope}}{\text{intcp} \cdot f} \quad (29)$$

Fig. 9 depicts $1/V_{out}$ versus $1/f$ for a nine-stage voltage multiplier chain for five different output resistances R_{out} . The values for V_{eq} and R_{eq} , derived from slope and intcp in (28), are indicated in Table II. The resistance of the transistors of the chain will influence the measurement results as explained above. However, another effect is also causing part of the difference between calculation and measurement: a loaded multiplier circuit has a small output voltage ($V_{out} < 10$ V) and all transistors will be operating with substrate bias conditions that imply a small $tg\alpha$ value. The values for V_{eq} , indicated in Table II, are the ones influenced by this small $tg\alpha$ value (see (18)). An

TABLE II
EXTRACTED VALUES OF V_{eq} AND R_{eq} FROM FIG. 8

Rout [MΩ]	Slope [Hz/V]	Intcp [1/V]	Veq [V]	Req at 100kHz [MΩ]
37.06	2261	.06121	16.33	13.69
47.07	1792	.06047	16.54	13.95
57.27	1474	.06016	16.62	14.03
67.33	1252	.05994	16.68	14.06
77.46	1085	.05980	16.72	14.06
Calculated with $tg\alpha = .951$ and $V_{t0} = .77$			17.72	13.71

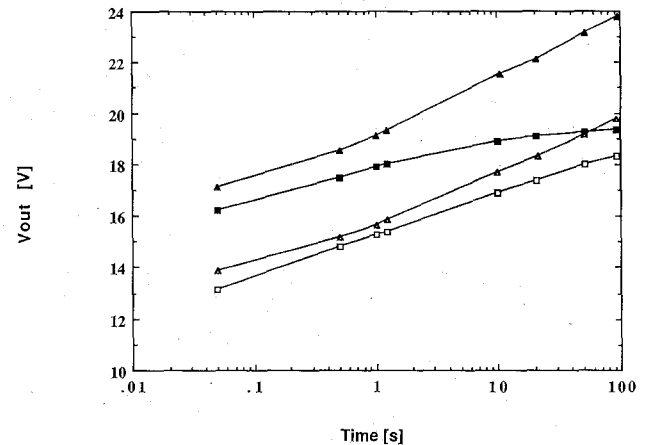


Fig. 10. Measured increase in output voltage with time for six- and nine-stage voltage multiplier circuits under different operating conditions. (Six-stage multiplier: $V_{in} = 5$ V, $V_{\phi} = 4$ V; $\square$ 10 kHz, $\blacksquare$ 100 kHz. Nine-stage multiplier: $V_{in} = 5$ V, $V_{\phi} = 3$ V; $\triangle$ 10 kHz, $\blacktriangle$ 100 kHz.)

increase in load resistance R_{out} will cause the output voltage to increase and the transistors will operate with a substrate bias that implies a larger $tg\alpha$. This increase in $tg\alpha$ will cause an increase in output voltage. This explains the increase in output voltage with increasing R_{out} in Table II. The small increase in equivalent resistance R_{eq} with increasing R_{out} , shown in Table II, is due to the same effect. The deviations, however, remain small, and the proposed model is able to explain all measurement results.

D. Degradation of the Voltage Multiplier

Any leakage current within the voltage multiplier circuit will cause the output voltage to decrease. Important leakage currents can be conducted by the capacitors along the chain. But as these currents change with time, the output voltage will also change with time.

We now consider a voltage multiplier circuit using interpoly capacitors. The first poly layer, on which the oxide is thermally grown, is connected to the clock signal; the polyoxide will draw a large leakage current even at moderate voltages at the top poly layer (electric field values of 2 MV/cm across the oxide). Although the polyoxide is rather thick (67 nm), these field values are easily reached in the voltage multiplier circuit. The large current injection

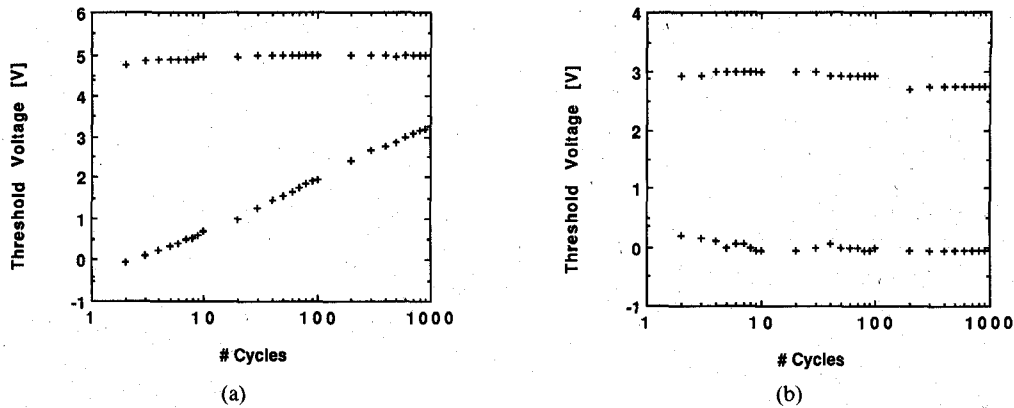


Fig. 11. Measured threshold-voltage window degradation of a memory cell. Programming conditions: (a) write $V_g = 18$ V, $V_d = 11$ V during 0.1 s; erase $V_g = 21$ V during 0.2 s (pulse generators); (b) write $V_g = 16$ V, $V_d = 12$ V during 1 s (pulse generators); erase V_g is supplied by a voltage multiplier circuit with nine stages ($V_\phi = 4$ V, $V_{in} = 4.5$ V, clock frequency = 100 kHz during 0.2 s).

in polysilicon oxide layers is known to be caused by the field enhancement at the asperities on the surface of the bottom polysilicon layer [8]. It is also known that this field enhancement results in a nonuniform distribution of the current over the total area, and an increased charge trapping at the injection sites [8]. Therefore, the leakage current will rapidly decrease with time. This phenomenon has a considerable effect on the output voltage of the voltage multiplier circuit. Indeed, leakage currents through the capacitors will initially limit the output voltage of the circuit. When the leakage currents through the polyoxide decrease rapidly with time, the output voltage of the multiplier circuit will start to increase. Because the voltage multiplier is based on a diode-capacitor chain, the circuit inherently has a very high internal resistance. Only a small decrease in capacitor leakage current is therefore needed for the output voltage to increase by several volts. Consequently, in this circuit, degradation of the current conduction capability of the polyoxide (due to charge trapping) will cause the output voltage to increase.

Fig. 10 shows the output voltage of two multiplier circuits under various frequencies, as a function of time. The maximum output voltage (i.e., the output voltage at $t = \infty$) will be equal to the one obtained in the total absence of leakage currents, which can be predicted by the model of Section II. The output voltage at the start of the measurement is determined by the leakage current flowing at that moment. If the capacitor-transistor chain is sufficiently long, several capacitors can be drawing a considerable current. This means that the simple model of the voltage multiplier circuit (a voltage source with a high internal resistance) can no longer be used to determine the output voltage. Nevertheless some features can be indicated: the lower the clock frequency, the smaller the output voltage at $t = 0$, but the larger the possible increase with time. If the transistor-capacitor chain is very long, the maximum output voltage is high but so will be the leakage current. Therefore, the output voltage at $t = 0$ will be much smaller than the maximum output voltage. This means that a circuit with only few stages operating at a low clock frequency and a very long chain operating at a

high frequency will behave similarly (output voltage at $t = 0$ much smaller than the maximum output voltage; large increase in output voltage is possible), although the absolute output voltage value of the latter can of course be different. This is also illustrated by Fig. 10.

If, however, a stable output voltage is required, this could be achieved by interchanging the function of the two polysilicon layers so as to avoid the leakage currents due to field enhancement at asperities.

The "degradation" effect can be used to control the output voltage of the circuit in time. This control capability is very interesting when nonvolatile memory circuits are considered, for which obtaining a constant memory threshold voltage window in gradually degraded memory cells can only be achieved by a corresponding increase of the programming voltage [9]. The ideal case would be the one in which the increase of the output voltage of the multiplier circuit matches the increase in programming voltage needed to obtain a constant memory threshold voltage window. Therefore it is important to understand the mechanisms that control the increase in output voltage of the multiplier circuit.

Fig. 11 shows the degradation characteristics of a nonvolatile memory cell that is programmed to a high threshold voltage by means of hot-electron injection and erased (towards a low threshold voltage) by means of Fowler-Nordheim conduction through the polyoxide between the floating gate and the control gate [8], [10], which could be a possible solution for flash EEPROM. In the case of Fig. 11(a), the programming and erase voltages are supplied by external pulse generators (constant amplitudes). A very significant and fast threshold-voltage window closure is observed, which is due to the trapping of negative charges in the polyoxide [8]. Fig. 11(b) shows the endurance characteristic of an identical nonvolatile memory transistor, where this time the erase voltage is supplied by a voltage multiplier circuit. Although this particular multiplier circuit was not designed to generate the erase voltage of this memory device, the figure clearly shows that the degradation of the voltage multiplier (i.e., an increase in output voltage) matches the memory degradation fairly well: the

threshold voltage window indeed does not show any closure up to 1000 cycles.

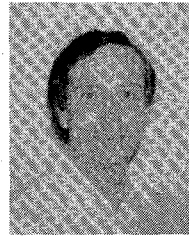
IV. CONCLUSIONS

The practical implementation of the voltage multiplier circuit uses transistors intended to operate as diodes. The features of the circuit change slightly with respect to the circuit consisting of genuine diodes: due to the body effect that influences the threshold voltage of the transistors in the chain, the output voltage of the circuit lowers with respect to the circuit with diodes, and at the same time the internal resistance of the circuit is reduced. The difference between the implementation with diodes and the one with transistors becomes more pronounced for circuits with more stages. The output voltage of the multiplier circuit is also limited, irrespective of the number of stages used. A model for the multiplier circuit is proposed and experimentally verified. This model allows the prediction of the characteristics of a wide range of voltage multipliers.

An important characteristic of the voltage multiplier circuit is its degradation behavior. In this case, a degradation means an increase in output voltage with time. By controlling the number of stages, the characteristics of the capacitors used, and the clock signal frequency, the change in output voltage with time can be modulated. It is demonstrated that this offers interesting possibilities when used in nonvolatile memory applications to compensate for the intrinsic degradation mechanism of nonvolatile memory cells caused by electron trapping in polyoxides.

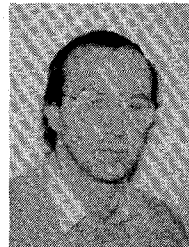
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