An Efficient Charge Recovery Logic Circuit

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Abstract—**Efficient charge recovery logic (ECRL) is proposed as a candidate for low-energy adiabatic logic circuit. Power comparison with other logic circuits is performed on an inverter chain and a carry lookahead adder (CLA). ECRL CLA is designed as a pipelined structure for obtaining the same throughput as a conventional static CMOS CLA. Proposed logic shows four to six times power reduction with a practical loading and operation frequency range. An inductor-based supply clock generation circuit is proposed. Circuits are designed using 1.0-μm CMOS technology with a reduced threshold voltage of 0.2 V.**

I. Introduction

INTEREST in low energy computing is growing as the cost of power dissipation becomes preposterous. Low energy is of utmost importance in, for example, a hand held computer, where its performance is not critical, but a battery life is of primary concern. Adiabatic computing is an attractive approach in this viewpoint. A method based on adiabatic technique uses an ac power supply rather than dc for the recovery of energy. Although adiabatic circuits consume zero power theoretically, they show energy loss due to nonzero resistance in the switches. Previous works on adiabatic circuit show their potential for real applications [1]–[4]. The previous adiabatic circuits deliver energy in the precharge phase, and recover their energy during the evaluation phase. Most of the proposed adiabatic circuits use diodes or diode-like devices for precharge. This causes unavoidable energy loss due to the voltage drop across the diodes. However, energy dissipation as a whole is still smaller than that of static logic.

Efficient charge recovery logic (ECRL) adopts a new method that performs precharge and evaluation simultaneously. ECRL eliminates the precharge diode and dissipates less energy than other adiabatic circuits. An ECRL inverter chain and a pipelined carry lookahead adder (CLA) are constructed to show the effectiveness of this approach.

In Section II, the concept and operation of ECRL are discussed. In Section III, practical design considerations of implementing the adder are described. Energy comparison and some simulation results are shown in Section IV. Section V shows the supply clock generation circuit, and Section VI is dedicated to the conclusion.

II. Basic Operations of ECRL

The schematic of the ECRL inverter that we propose is illustrated in Fig. 1. This logic has the same circuit structure as cascode voltage switch logic (CVSL) with differential signaling [5].

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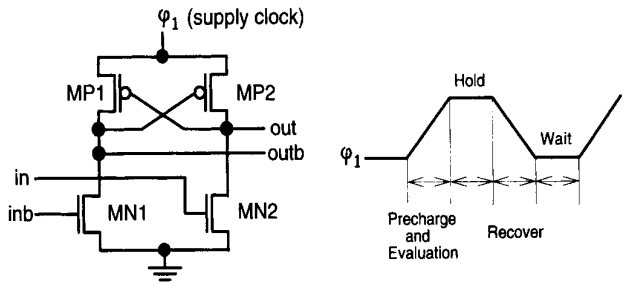

Fig. 1. ECRL inverter and supply clock.

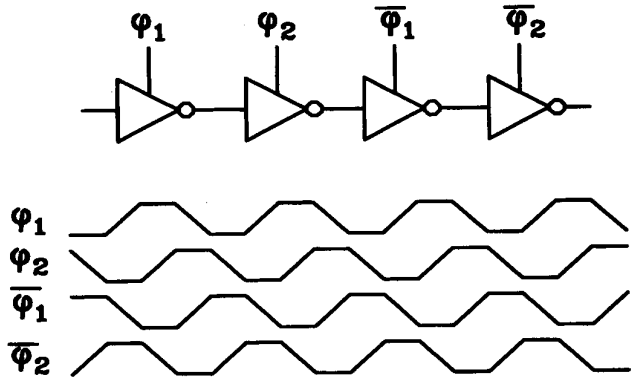

Fig. 2. Inverter chain and four-phase supply clock.

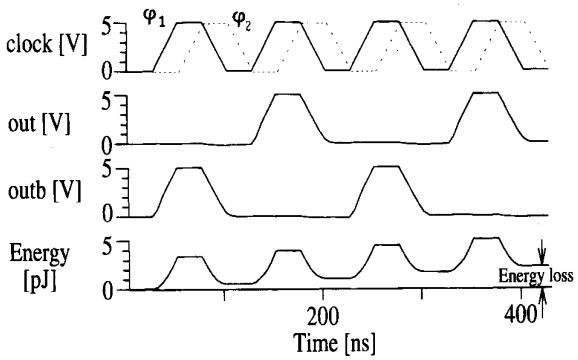

Fig. 3. Nodes waveforms of inverter chain.

For the purpose of initial discussion, let us assume in is at high and inb is at low. At the beginning of a cycle, when the supply clock φ_1 rises from zero to V_{dd}, out remains at a ground level, because in signal turns on MN2. Outb follows φ_1 through MP1. When φ_1 reaches V_{dd}, the outputs hold valid logic levels. These values are maintained during the *hold* phase and used as inputs for evaluation of the next stage. After the *hold* phase, φ_1 falls down to a ground level, outb node returns

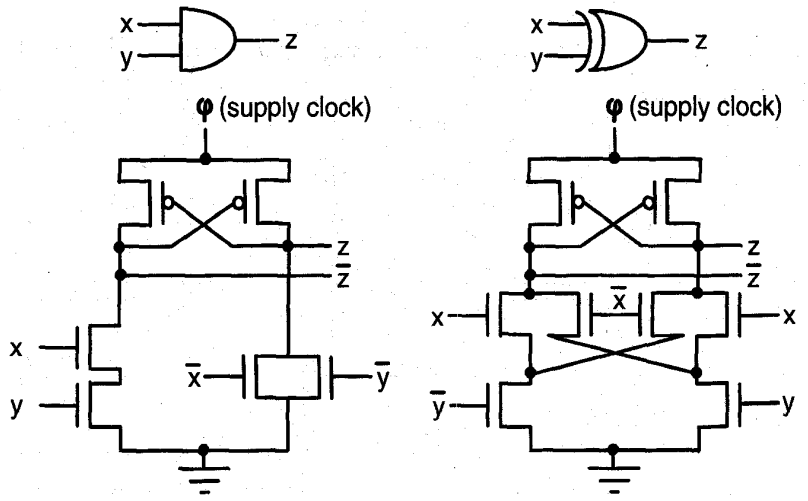

Fig. 4. ECRL AND gate and exclusive-OR gate.

its energy to φ_1 so that the delivered charge is recovered. Thus, the clock φ_1 acts as both a clock and power supply. *Wait* phase is inserted for clock symmetry. In this phase, valid inputs are being prepared in the previous stage.

There is a clocking rule to form a chain of logic circuits. Fig. 2 shows phase relationship among supply clocks. ECRL uses four-phase clocking to efficiently recover the charge delivered by the supply clock. Each clock is followed by the next clock with a 90° phase lag. So when the previous stage is in the *hold* phase, the next stage must evaluate logic values in the *precharge and evaluation* phase.

Output and clock waveforms of a inverter chain and energy dissipation are shown in Fig. 3. In the first cycle from 0 ns to 100 ns, node out stays at low and outb follows the supply clock. In the next cycle from 100 ns to 200 ns, outputs are reversed, because the input values are changed. The energy graph shows that energy is recovered as the supply clock goes down but not completely. This energy loss is very small compared to other logic families.

ECRL would consume unnecessary power with two-phase clocking because the transition of logic value in the previous stage can affect the next stage. So four-phase clocking is recommended for the effective energy saving.

III. Circuit Designs

A. Gate Design

ECRL gate consists of PMOS loads and NMOS pull-down transistors. This structure needs differential inputs and is the same structure as CVSL except that all the gates need specific clocks depending on their stages. The ECRL inverter is already shown in Fig. 1 and Fig. 4 shows the schematics of two basic gates, an AND gate and an exclusive-OR gate. The complex gate could be constructed by the conventional MOS gate design method. Some CVSL design techniques are used to minimize transistor count, especially in the exclusive-OR gate shown here [6]. A three-input exclusive-OR gate is constructed easily using this technique by adding four NMOS pull down transistors. Although a static CMOS can be used for the same purpose, a differential structure is more adequate since the loading capacitance seen by clocks remain constant regardless of their input combinations, which is important for the design of clock circuits.

B. Adder Design

An adder is an essential element in a digital system, so the design of the adder is chosen to show the usefulness of the new logic family. Adiabatic logic computes only one logic level per phase, so it is difficult to implement a complex logic with a long chain of stages. In this respect, a ripple carry adder (RCA) is not practical with the adiabatic method, since it needs many phases to obtain a result. 32-b RCA would need at least 32-phases to execute one addition.

A CLA not only reduces logic depth, but also offers a pipelined structure if buffers are added in the circuit. So CLA structure is adopted in the design of the ECRL adder to overcome the drawback of an adiabatic circuit.

The schematic of 16-b pipelined ECRL CLA is shown in Fig. 5. The triangles are buffers. These are the same as the inverter except that output nodes are swapped. Many buffers are used for maintaining a pipeline. These buffers propagate the correct logic values for addition like latch in the general pipeline structure. Pipelined structure uses all the blocks of a digital system, so it gives high throughput. The rectangular block is the basic cell and it is composed of three gates. We merged two gates—AND and OR gates—in the basic cell into one ECRL gate to reduce latency. The implementation of merged gate and basic cell is shown in Fig. 6.

This adder can execute 16-b addition per phase and six stages are needed to compute the result as shown in Fig. 5.

The difference between static CLA and ECRL CLA is the use of buffers for maintaining a pipeline in ECRL CLA. Using buffers increases the transistor count, but helps to ease layout due to regularity. To obtain the first result of the addition, a few cycles of latency are needed. The latency is only 1.5 cycles

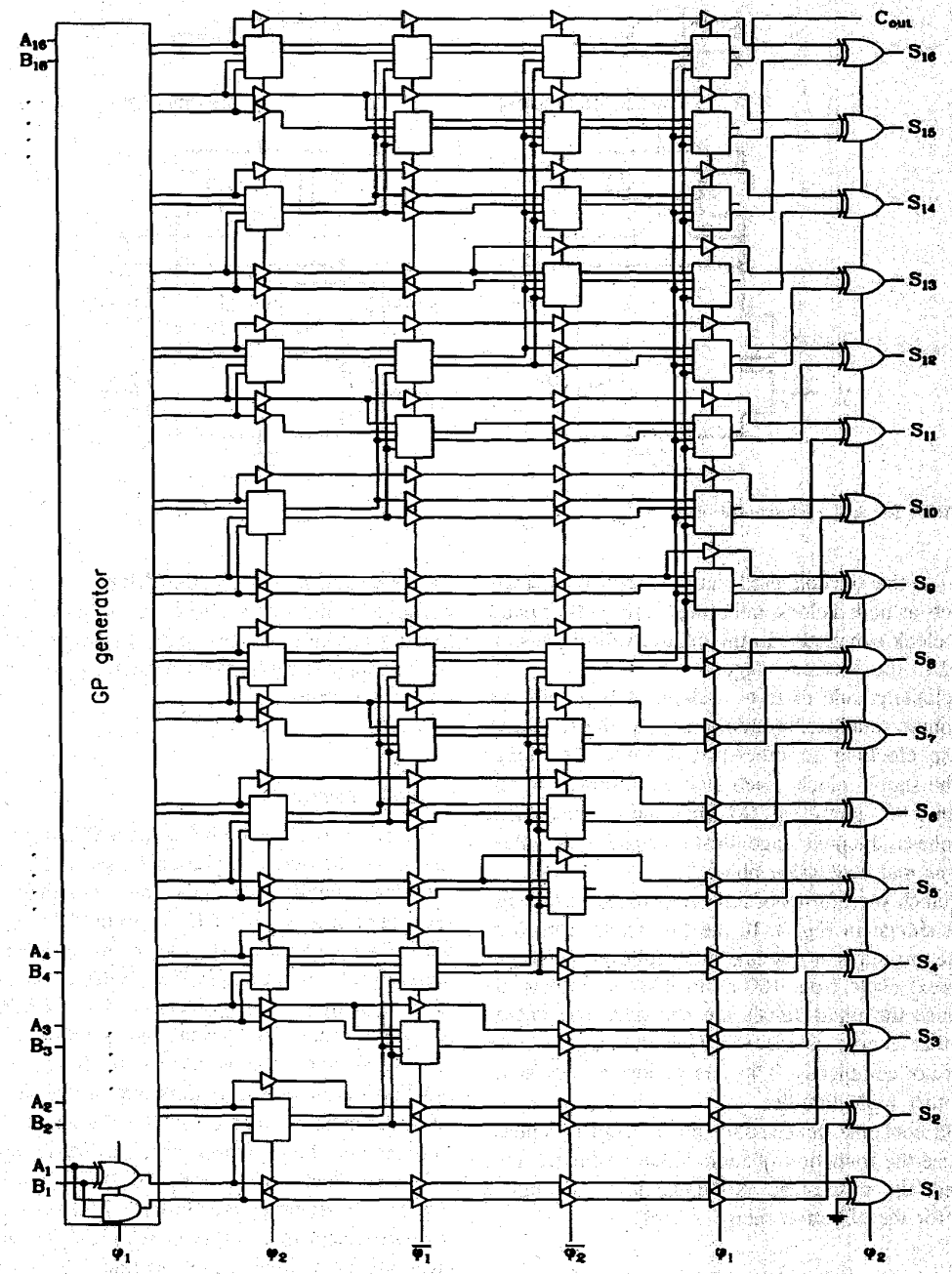

Fig. 5. Schematic of 16-b CLA.

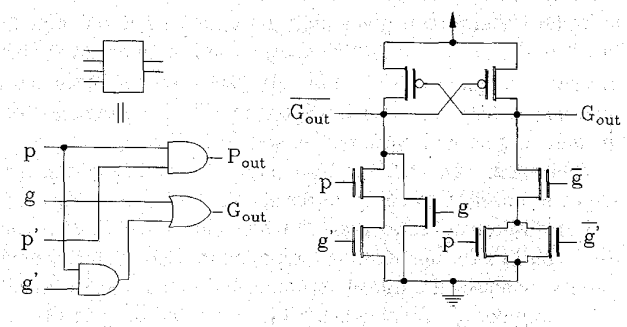

Fig. 6. Implementation of basic cell.

for the 16-b adder. Only two stages (0.5 cycle) are added for a 64-b adder and the latency is two cycles.

IV. Energy Comparison

Energy comparison is an interesting concern in adiabatic logic design. The energy loss of a conventional fully static CMOS including the discharge power-dissipation term is

$$E_{\text{conv}} = CV_{dd}^2 \tag{1}$$

and this equation is the basis of the analysis of simulation results. Operating frequency term is excluded in this expression, so the energy loss equation represents energy loss per cycle.

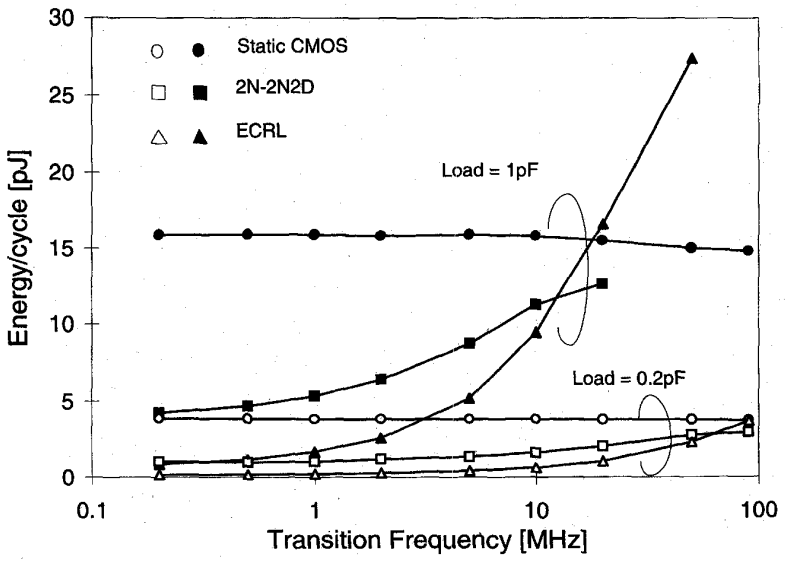

Fig. 7. Energy versus transition frequency for inverter chain.

Previous adiabatic circuits need diodes for precharging output nodes [2]–[4]. Using a diode for precharge leads to an unavoidable energy loss due to a voltage drop across the diode when turned on. But adiabatic circuits which have a *precharge* phase need the diode or diode like device inevitably. Thus energy loss is given as

$$E_{\text{prev}} \approx CV_{dd}V_{d,on} \tag{2}$$

$V_{d,on}$ is the diode turn-on voltage and a threshold voltage of 0.2 V is used for simulation assuming it is made of an NMOS. 2N-2N2D logic family [4] is used as a previous adiabatic circuit in this comparison.

ECRL always pumps charge on the output with a full swing. However, as the voltage on the supply clock approaches to $|V_{tp}|$, the PMOS gets turned off. So the recovery path to the supply clock is disconnected, thus, resulting in incomplete recovery. V_{tp} is the threshold voltage of PMOS and -0.2 V is assumed. The amount of loss is given as

$$E_{ECRL} = C|\ V_{tp}\ |^2/2. \tag{3}$$

Although nonzero, it is still more than ten times smaller than the energy loss of the previously mentioned adiabatic circuits with supply voltages greater than 1 V.

A. The Energy Comparison of Inverter Chain

Fig. 7 shows the comparison of energy dissipation with static CMOS and 2N-2N2D with varying data rate. 1.0-μm CMOS technology with the threshold voltage of 0.2 V is used in simulation. An inverter chain in Fig. 2 is used for simulation, and the channel width of NMOS is 5 μm and PMOS 10 μm. A set of trapezoidal supply clocks with equal rise, hold, fall, and wait times is used.

The energy is calculated per transition with the same input pattern and rectangular waveform is used as input signal for ECRL and static inverter chain. The load means output loading capacitance. Energy dissipation in the static inverter chain does not vary over transition frequency. But as the transition frequency increases, adiabatic circuits dissipate more energy due to power dissipation in the increased resistance of the devices. Some points not drawn on the graph at high frequency represent malfunction due to incomplete transition.

When the load is 0.2 pF, ECRL shows the best energy performance. At higher load capacitance, the trend is similar but energy gain is not as large, even though ECRL still shows the least energy consumption. Loss of energy due to resistive MOS switches is greater when the transition frequency is high and load capacitance is large. But ECRL shows good energy efficiency in wide operating conditions, especially with a small load capacitance at low frequency operation.

As shown in Fig. 8, computing energy is reduced for all types of logic as the supply voltage decreases. The energy consumption of the static CMOS is independent of its operation frequency and is dependent only on its supply voltage. As the supply voltage decreases, the gap between static CMOS and ECRL is reduced. But ECRL still shows large energy savings over wide range of supply voltage. In this comparison of energy consumption, only the energy of the ECRL core is considered. For a fairer comparison, energy loss due to supply clock generator must be included. Including this loss, ECRL dissipates two to three times larger energy. This topic will be treated in detail separately in Section V.

At 5 V supply and 10 MHz clock input, 2N-2N2D dissipates 42% of the energy of the conventional CMOS. ECRL dissipates only 16%. At 500 KHz, 2N-2N2D dissipates 26% and ECRL dissipates 5% of the energy of the conventional CMOS. ECRL shows 20 times power gain in this case.

Energy dissipation varies as the threshold voltage changes. The simulation result of the inverter chain which indicates the effect of different threshold voltages is shown in Fig. 9. Lowering the threshold voltage helps the adiabatic circuits save energy as is already shown in the energy loss equations

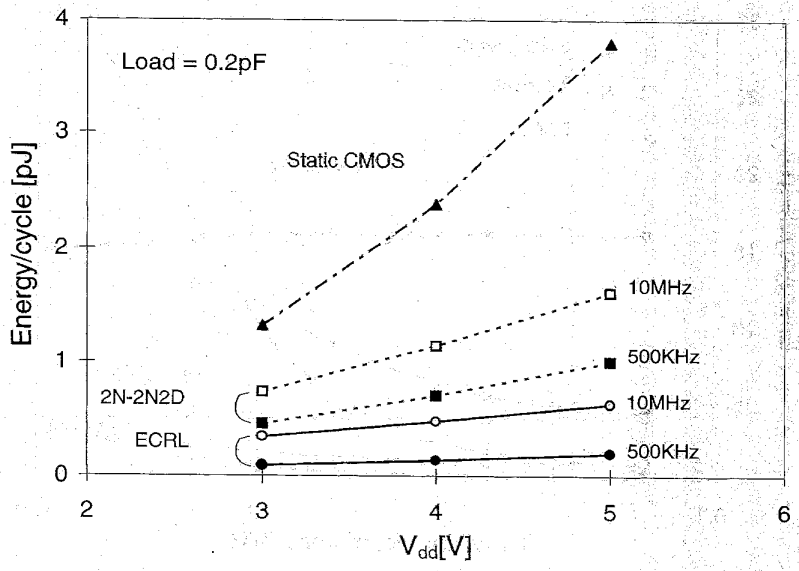

Fig. 8. Energy versus supply voltage for inverter chain.

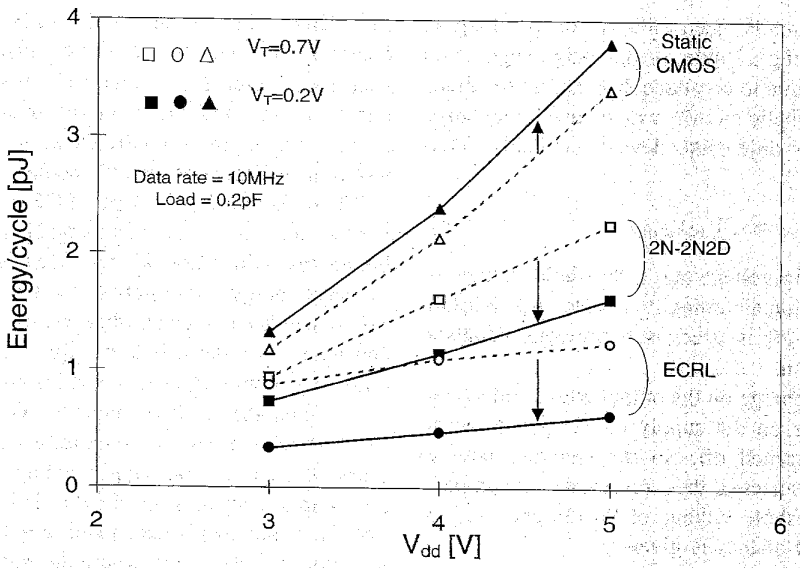

Fig. 9. Effect of threshold voltage on energy consumption for inverter chain.

(2) and (3). In 2N-2N2D, energy is reduced due to reduced voltage drop across the diode-connected NMOS. In ECRL, energy loss is decreased even more, since the PMOS pull-ups become cut-off at a lower voltage with the stored energy being returned to the supply clock with less loss.

In contrast to adiabatic circuits, a static circuit consumes slightly more energy because of the increased crowbar current.

B. The Energy Comparison of Carry Lookahead Adder

A plot of energy per addition for conventional CLA and ECRL CLA as a function of operation frequency is drawn in Fig. 10. The relative energy gain is significant with the same throughput as a static CMOS. This result shows the beneficial use of ECRL in real applications. ECRL reduces the power dissipation of the 16-b CLA by about four to six times over a static CLA in various supply voltages although the ECRL adder has more transistors. Large transistor count is due to the fact that ECRL CLA has many buffers for pipelining. The transistor count of ECRL CLA is approximately 60% larger than that of the conventional CLA. Since ECRL CLA provides differential signals, additional gates are not needed where inverted signals are required. The ECRL CLA shows small energy increase at low frequency because of the static power dissipation caused by subthreshold current due to low V_T devices. The amount of static power is the same for both low and high frequency, but the energy, being the accumulation of power, is proportional to a time period. The effect of

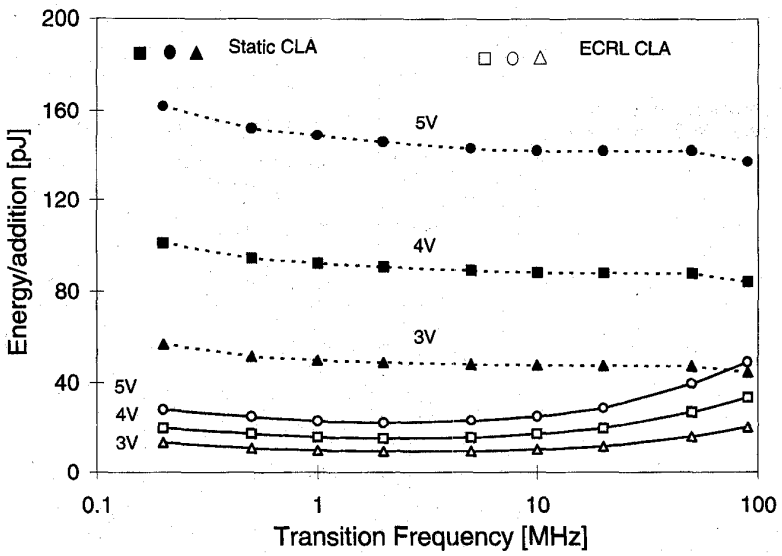

Fig. 10. Energy consumption of 16-b CLA's.

this portion is negligible for higher threshold voltage and high clock frequency. At a high frequency region, the energy consumption of a static CLA decreases due to the reduced logic swing.

V. Supply Clock Generation

ECRL saves energy by returning delivered energy back to the supply. The ac power supply is needed to efficiently restore the charge, so an efficient clock circuit which converts dc power to ac should be designed. The LC resonant circuit which performs like a Colpitts-type oscillator is suitable for a supply clock generator. It consists of one inductor and two capacitors with MOS switches.

The supply clock generation circuit based on this idea is shown in Fig. 11. The clock nodes of ECRL are represented by C_1, R_1 and C_2, R_2 and an external inductor is needed to move the charge from C_1 to C_2 or vice versa. NMOS and PMOS operate as switches to dc supply and ground to maintain the amplitude of supply clock nodes by supplying loss of charge. It is not necessary to turn on MOS switches when the amplitude of supply clock nodes is maintained in the desired range. This superfluous energy could be eliminated by turning the MOS switches off. The peak detector monitors the amplitude of supply clock nodes, and provides *disable* signal for gating the signals for MOS switches. φ_1 and φ_2 are signals for MOS switches, which are supplied externally and used with *disable* signal through NOR gate. This supply clock circuit generates a sinewave, substituting the trapezoidal supply waveform. We verified that the ECRL system operates from sinewave sources with a minimal increase in energy loss. Although multiphase clocking for submicron VLSI chips could cause interconnection complexity, ECRL substitutes supply clocks for clock and power lines, so area overhead due to interconnection is not severe. While interconnection capacitance does not cause any energy loss, interconnection resistance does result in energy loss and clock skew.

Fig. 12 shows a simple peak detector and comparator circuit which follows the peak voltage of the clock nodes and generates a *disable* signal. The comparator used in Fig. 12 is designed to have a threshold of 4 V. Hence, the detector and comparator generate a *disable* signal when the peak value does not fall down below 4.5 V, assuming the V_T of NMOS to be 0.5 V due to body effect. The response time of peak detector could be controlled by the current source and the capacitor. The schmitt trigger inverter is used to prevent the ripple of peak detector output.

The supply clock generator shown in Fig. 11 produces two supply clocks which have 180° phase difference. But ECRL needs four-phase clocking, so two supply clock generators which have 90° phase difference are needed. Such a scheme is shown in Fig. 13. The supply clock generator is initiated by external switch signals as φ_1 and φ_2. To generate four supply clocks with 90° phase difference, the external switch signals, $\varphi_1 - \varphi_4$, of the shape as shown in Fig. 13, are needed. It is not difficult to provide signals like $\varphi_1 - \varphi_4$ and the synchronization of supply clocks is realized by these switch signals.

The energy efficiency of the clock generation circuit is calculated by monitoring the delivered power from the external dc supply and dissipated energy in supply clock nodes. The efficiency depends on the values of R_n and C_n which represent a node of an ECRL supply clock. The efficiency ranges from 15% to 60% depending on R_n and C_n values. The large portion of delivered energy is dissipated in the MOS switches because of the resistance of the MOS switches.

Four-phase supply clocks which are generated by the circuit mentioned are shown in Fig. 14. The clock waveform is obtained by substituting the node modeled with R_n and C_n to ECRL CLA supply node. Small capacitors are added to nodes to balance capacitance and the added capacitance is about 2 pF. At the beginning of power-up, the amplitude of the supply clock is small. The amplitude of the supply clock grows as the MOS switches provide energy from dc supply.

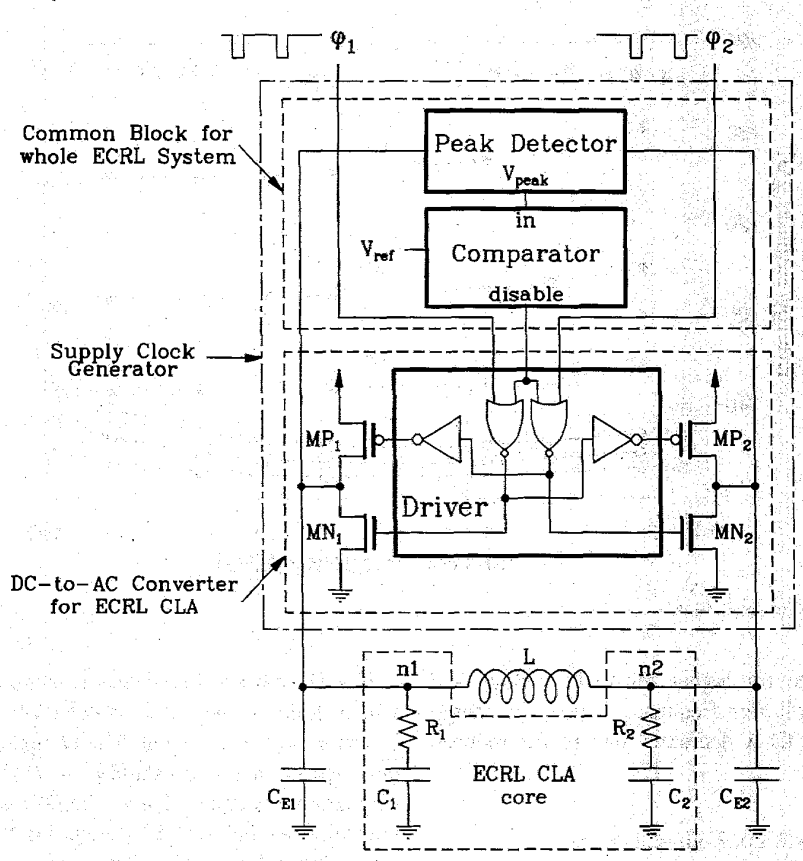

Fig. 11. Inductor-based supply clock generator with external capacitor for capacitance balance.

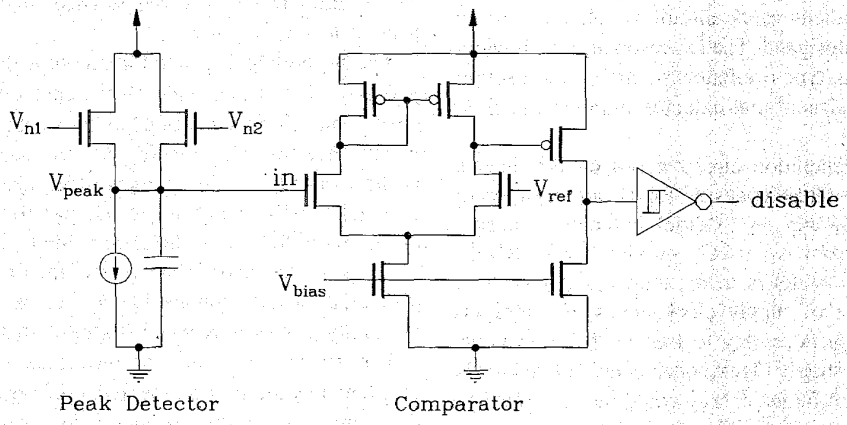

Fig. 12. Peak detector and comparator.

The difference of clock amplitude is due to the mismatch in capacitance of supply clock nodes. The amplitudes are matched by trimming the added external capacitor. An input test vector was arranged so that the least significant bit (LSB) of ECRL outputs is changed on every clock. The differential output nodes—*s1p*, *s1b*—of ECRL CLA LSB are shown in Fig. 15. The output waveform of LSB shows the correct operation of ECRL CLA under the designed supply clock circuit.

The capacitance of the ECRL supply node is dependent on the complexity of the ECRL system. The 16-b CLA which uses 1.0-μm double-metal CMOS technology shows about 10 pF on each supply node. The capacitance is obtained in simulation by forcing a sinusoidal wave to the supply nodes and measuring the current level. The capacitance shows 10%–30% differences between supply nodes, but the balance of capacitance is obtained by adding a small external capacitor to the supply nodes with low capacitance.

Table I shows the power dissipation of each functional block of the ECRL CLA. The ECRL core dissipates slightly more power than the amount shown in Fig. 10 due to the distortion of the supply clock waveforms from an ideal waveform. The

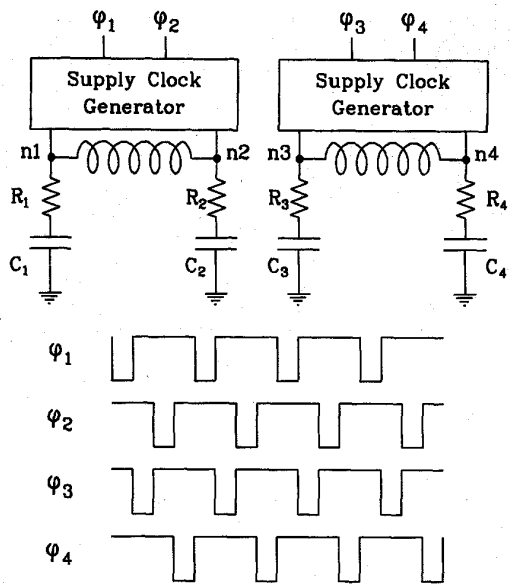

Fig. 13. Four-phase clock generation circuit.

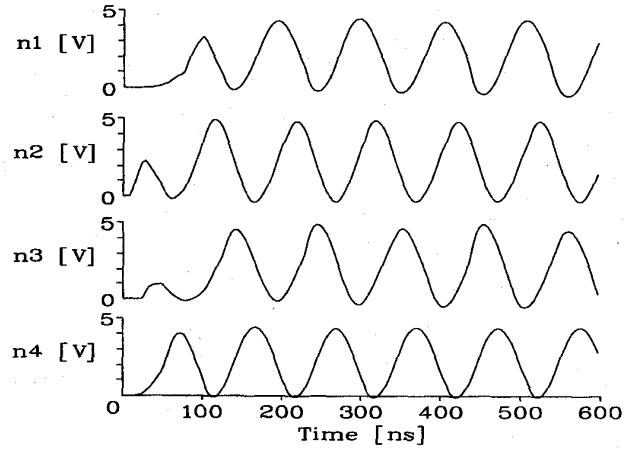

Fig. 14. Generated four-phase supply clocks for 16-b ECRL CLA.

supply clock generator consists of a peak detector, a comparator, a driver, and MOS switches. The MOS switches dissipate additional power due to their resistance while providing energy to the LC resonator. Also, the driver for MOS switches consumes dynamic power from the dc supply. Other blocks such as the peak detector and the comparator are common to all adiabatic system, which makes their power consumption amortized into a negligible portion. As such, in Table I, only the power dissipation of the dc-to-ac converter which comprises the MOS switches and the driver is considered as a loss of power. The MOS switches and the driver scales as the size and complexity of the ECRL core grows.

The conversion efficiency is defined as the ratio of dissipated energy in ECRL core and total delivered energy from the dc supply. Although the conversion efficiency is near 40% in this case, a larger efficiency could be obtained by selecting an optimum operation frequency other than 10 MHz. Including

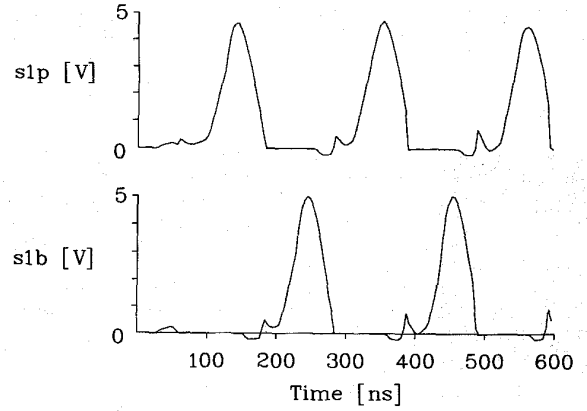

Fig. 15. Adder outputs of ECRL CLA (least significant bit).

TABLE I
SUMMARY OF POWER DISSIPATION OF 16-b ECRL CLA OPERATING AT 10 MHz

Power Dissipation of ECRL core	258uW
Power Dissipation of DC-to-AC converter	365uW
Total Delivered Power	623uW
Conversion Efficiency	41%
Power Dissipation of Conventional CMOS	1430uW
Power Gain of ECRL over Conventional CMOS	56%

the energy dissipated in the supply, an ECRL still shows 56% of energy saving compared with a conventional CMOS logic.

VI. CONCLUSION

ECRL is a low-energy, adiabatic logic. ECRL has CVSL structure and needs four-phase clocking for the efficient energy recovery. Simulation indicates power saving over static and other adiabatic logic families. The ECRL inverter chain shows 10–20 times power gain over a conventional inverter chain. Simulation studies with a 16-b pipelined CLA show four to six times power gain with the same throughput compared with a conventional CLA. A method to generate four-phase supply clocks is suggested and an incorporation of this with ECRL CLA is shown to be effective. ECRL shows large power saving and pipelined CLA shows the promising usage of ECRL in a low power system.

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