Substrate Triggering and Salicide Effects on ESD Performance and Protection Circuit Design in Deep Submicron CMOS Processes

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Abstract

The effect of salicides and the influence of the local substrate potential on ESD performance of deep submicron nMOS transistors have been studied. It is shown that salicidation causes a strong dependence of ESD performance on effective channel length in these devices. Salicides also impact the behavior of the lateral *npn* parasitic bipolar transistor by affecting the emitter efficiency. A higher local substrate potential has been shown to have a positive impact on ESD performance. Based on these results we have designed and demonstrated a substrate triggered nMOS protection circuit which provides > 2 kV ESD performance in a fully salicided process.

Introduction

As technologies scale towards sub-0.25 μm, design challenges for effective Electrostatic Discharge (ESD) protection circuits include operation to > 2 kV, area efficiency, and compatibility with mixed voltage interfacing (e.g. 2.5 V/3.3 V) [1][2]. Figure 1 shows a typical protection circuit using a lateral *npn* (LNPN) formed by a nMOS between the I/O pad and ground bus V_{ss} [2], and a *pn*-diode to the supply bus V_{dd} [1][3]. Such a protection circuit is most effective if the LNPN has a low trigger voltage V_{trig} and a high ESD capability. The main objectives for LNPN design are, therefore, to reduce V_{trig} and increase the second breakdown trigger current, I_{t2}, which is the ESD monitor parameter. The target for $I_{t2} \sim 5$ mA/μm. A cross-section of an nMOS transistor indicating the LNPN is shown in Figure 2. The operation of the LNPN depends on the substrate current I_{sub} to forward bias the source-substrate (emitter) junction. Hence the substrate resistance R_{sub} and *local* substrate potential V_{sub} are important parameters [2][4].

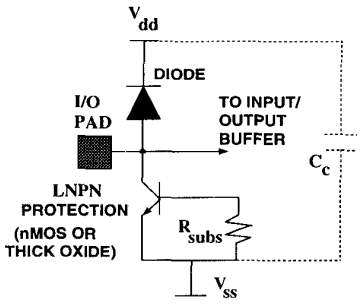

Figure 1: *Typical ESD protection circuit using a lateral* npn *to* V_{ss} *and a* pn *diode to* V_{dd}. *The* npn *can be formed using an nMOS device or a field oxide device.* C_C *is the effective chip capacitance.*

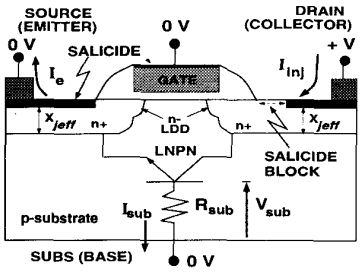

Figure 2: *Cross-section of an nMOS transistor showing the parasitic* npn *transistor.* $V_{sub} = I_{sub} \times R_{sub}$ *is the local substrate potential at the source-substrate junction. The effective junction depth* X_{jeff} *is the distance between the bottom of the salicide and the junction. In a field oxide* npn *the two n regions are seperated by field oxide.*

In this paper we show that, in addition to the expected adverse effect of the salicided drain on I_{t2} in a 0.35 μm process [6], the salicided source also has an effect. Higher I_{t2} was observed by increasing the spacing between the edge of the source salicide and the gate. This is an important result which relates I_{t2} to the properties of the LNPN emitter. It is observed experimentally that a higher V_{sub} improves the LNPN I_{t2} and reduces the negative effect of salicidation by aiding the LNPN action. Hence, circuit designs which raise the local substrate potential can increase ESD performance in fully-salicided processes. Since the lateral *pn* diode forms a vertical *pnp* (VPNP) between the pad and V_{ss} with the base tied to V_{dd} as shown in Figure 3 [3][5], the collector current I_C can be used to raise V_{sub}. We demonstrate a VPNP-triggered LNPN circuit design with > 2 kV ESD performance in an SRAM IC,

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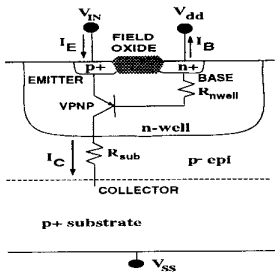

Figure 3: *Cross-section of a lateral n-well* pn *diode showing the parasitic vertical* pnp. *The emitter is connected to V_{IN}, and the base to V_{dd}. The collector is the p^+ substrate.*

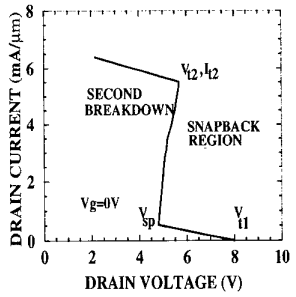

Figure 4: *The high current I-V curve for a nMOS transistor in lateral* npn *mode for L_{gate}=0.35 μm. The gate, source and substrate are at 0 V. The* npn *triggers at V_{t1} and V_{sp} is the holding voltage. I_{t2} is the onset of second breakdown and is the ESD monitor parameter.*

and verify the device operation using device simulations.

High current effects in nMOS

The high current $I-V$ curve for nMOS transistors shown in Figure 4 [2], can be directly related to Human Body Model (HBM) ESD levels through I_{t2}. Figure 5 shows that I_{t2} in a 0.35 μm process depends on the drive current I_{drive}, which is inversely proportional to the effective channel length L_{eff}. Typically, output transistors have longer L_{eff} with $I_{drive} \sim 350\ \mu A/\mu m$, where the nominal $I_{drive} \sim 550\ \mu A/\mu m$. I_{t2} for the long L_{eff} transistors is approximately 1.5 mA/μm which is much lower than the ~5 mA/μm obtained for the nominal 0.35 μm devices (Figure 5).

It was observed that by selectively blocking salicide and increasing the spacing between the drain salicide edge and gate (Figure 2), I_{t2} is significantly increased for the long L_{eff}. Figure 5 shows that by increasing the spacing between the drain salicide edge and the gate from 0.7 μm to 2.1 μm, the I_{t2} can be restored to that of the nominal L_{eff}. Thus the reduction in I_{t2} for longer L_{eff} is due to

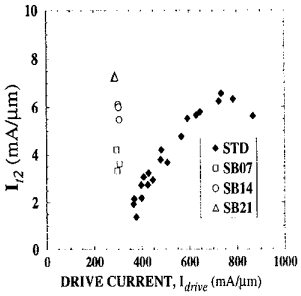

Figure 5: *I_{t2} versus drive current I_{drive} in a 0.35 μm process. $I_{drive} \propto 1/L_{eff}$. The data is shown for fully-salicided devices (STD), and with salicide blocked in the drain only (see Figure 2). The distance between the edge of the salicide and the gate is 0.7 μm (SB07), 1.4 μm (SB14), and 2.1 μm (SB21).*

the presence of salicide.

An external substrate bias was applied to fully salicided nMOS and field oxide (FOX) LNPN devices. Figure 6 shows that I_{t2} increases for both structures as a function of V_{sub}. The nMOS devices were more responsive to V_{sub} than the FOX devices, though both show significant increase in I_{t2} beyond $V_{sub} = 0.8$ V. It was also observed that V_{trig} was reduced from the avalanche breakdown voltage $V_{t1} \approx 8$ V for $V_{sub} = 0$ V (see Figure 4) to the snapback holding voltage $V_{sp} \approx 4.5$ V for $V_{sub} > 0.8$ V.

Protection circuit design

We can now consider protection circuit designs for a fully salicided process, where circuit techniques are used to raise V_{sub}. A simple example of such a technique is to place a VPNP in close proximity to a LNPN as shown in Figure 7. During an ESD event, VPNP turns on, driving current through R_{subs} (Figure 7 inset) which increases

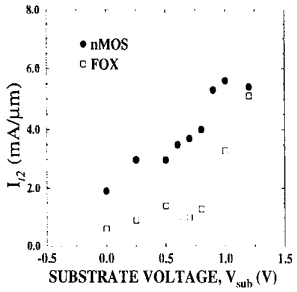

Figure 6: *I_{t2} as a function of an external substrate voltage V_{sub} for nMOS and field oxide (FOX) lateral* npn *transistors.*

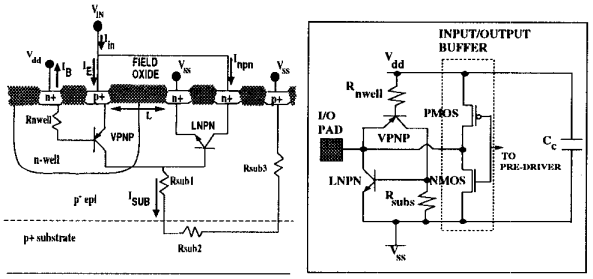

Figure 7: *Cross-section of a VPNP triggered LNPN ESD protection circuit. The p^+-n^+ spacing L is $\approx 10\mu m$ and the SCR cannot trigger. R_{sub1}, R_{sub2} and R_{sub3} form the total substrate resistance. Inset: the schematic circuit with the input/output buffer and the V_{dd} to V_{ss} chip capacitance C_c. Typically $C_c \geq 1nF$.*

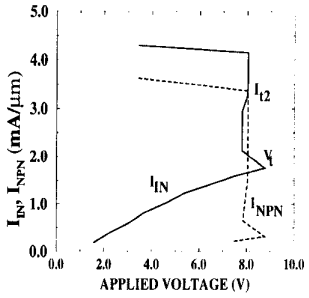

Figure 9: *$I-V$ curve for a VPNP triggered protection circuit showing the input current I_{IN} and the LNPN current I_{NPN} as a function of the applied voltage. I_{IN} is applied to the emitter of the VPNP and the collector of the LNPN. The other terminals are at 0 V.*

V_{sub}. When V_{sub} reaches 0.8 V, the twin objectives of a reduced LNPN V_{trig} and a higher I_{t2} can be achieved.

The high current behavior of VPNP is important in designing this circuit. Figure 8 shows the high current $I-V$ curve of a VPNP, and also the variation of the gain β with the emitter current I_E and the collector current I_C. β is $\ll 1$ at high currents and e.g. $I_C \approx 3$ mA/μm for $I_E \approx 30$ mA/μm at $V_{IN} = 5$ V, but this I_C is well above the ≈ 0.5 mA/μm required to trigger the LNPN in this process. The stand-alone field-oxide LNPN had a $V_{trig} \approx 12$ V and $I_{t2} \approx 1$ mA/μm. The $I-V$ curve for a VPNP-triggered field-oxide LNPN is shown in Figure 9. The current in the lateral *pn*-diode (emitter-base of VPNP) dominates until $V_{trig} \approx 9$ V, at which point the LNPN is triggered by the V_{sub} due to the VPNP I_C. The current through the LNPN is indicated by I_{NPN} and now $I_{t2} \approx 4$ mA/μm compared to 1 mA/μm for the stand-alone device.

The ESD performance of a VPNP-triggered LNPN protection circuit for SRAM Input/Output (I/O) pins was evaluated. The stand-alone LNPN failed at 500 V HBM ESD stress. Connecting a VPNP as shown in Figure 7 increased the ESD level to > 2 kV. The LNPN V_{trig} and the trigger current are functions of the n-well resistance, R_{nwell} and R_{sub}, respectively, and together with the chip capacitance C_c will have a strong influence on the ESD capability of this circuit. The I/O pad voltage and V_{dd} voltage as a function of peak ESD current in Figure 10 shows the LNPN triggering. C_c was $\sim$4 nF for this IC.

Figure 11 shows device simulations of a substrate-triggered circuit subjected to a 1.5 kV HBM ESD pulse. The current flowlines before and after the LNPN is triggered are shown in (a) and (b). The main current path is seen to move from the *pn*-diode to the LNPN after triggering. C_c was taken to be 10 nF. For mixed voltage circuits, measurements showed that 4-diode ($I_C \approx 12$ mA/μm) and 6-diode ($I_C \approx 14$ mA/μm) strings have larger I_C for a given $I_E \approx 30$ mA/μm and $V_{IN} \approx 5$ V, and will enable

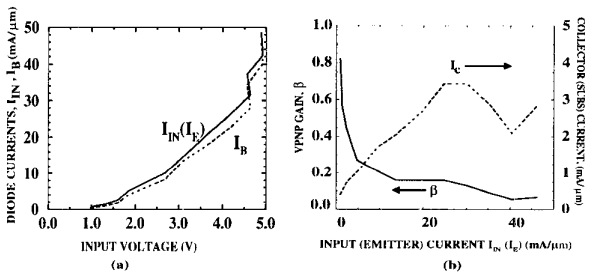

Figure 8: *(a) The input (emitter) current I_{IN} and the base current I_B of a vertical* pnp *device. (b) The current gain β and collector current I_C of the VPNP as a function of the input (emitter) current I_E.*

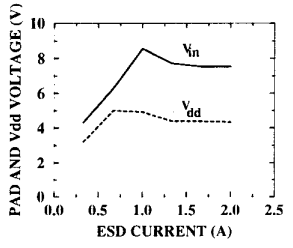

Figure 10: *The input voltage V_{IN} and the V_{dd} voltage as a function of the peak ESD current for a VPNP triggered ESD protection in a 0.35 μm SRAM circuit. The ESD pulse is applied between the input/output pad and V_{ss}; the other pins are floating.*

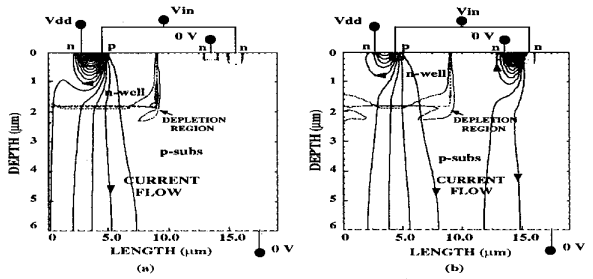

Figure 11: *TMA MEDICI device simulations showing current flowlines (a) before and (b) after LNPN triggering, for a VPNP triggering circuit. The device is subjected to a simulated 1.5kV HBM ESD pulse and V_{dd} is connected through a 10 nF capacitor to ground. $V_{in} \approx 5$ V after triggering, with input current of 8 mA/μm.*

better LNPN triggering.

The Effect of Salicides

It has been suggested [7] that one of the reasons for the reduction in ESD performance caused by salicides is the shallower effective junction depth X_{jeff} (see Figure 2). A shallower LNPN emitter has a lower emitter efficiency and requires more avalanche generated hole current to sustain the bipolar action. Salicidation also causes the current in the drain to be restricted to the region close to the salicide [6], which increases the effective current density in the drain. These two effects combine to increase the junction heating at the drain and lowers I_{t2}. Experimentally, we observed that thinner salicides *or* deeper junctions, both of which increase X_{jeff}, resulted in a higher I_{t2} in accordance with this analysis.

The increase of I_{t2} with V_{sub} indicates that when LNPN is externally biased a lower avalanche current will sustain the LNPN thereby compensating the negative effect of the salicide. To verify the effect of the source (emitter) salicidation, devices with salicide blocked in the source only (maintaining fully salicided drains) were tested. The results in Figure 12 show that I_{t2} increases with salicide-edge to diffusion-edge spacing in the source. The effect on I_{t2} is less than with drain salicide blocking shown in the same figure, but is still significant. Hence, the negative impact of salicide on ESD can also be related to its effect on the emitter efficiency of the LNPN. Some of the improvement with salicide blocking may be attributed to the ballasting effect of the higher emitter resistance after the device begins to enter thermal runaway. However, the emitter resistance in non-salicided processes, as defined by the source contact to gate spacing, has not been observed to be significant [8] and should not be the dominant effect resulting in the higher I_{t2}.

These results are the first demonstration that salicidation of the LNPN emitter impacts ESD performance in these deep submicron nMOS devices. The data supports the analysis that the emitter efficiency γ is an important parameter in the high current operation of the LNPN. MEDICI device simulations confirmed that γ given by $I_{nE}/(I_{nE}+I_{pE})$, where I_{nE} and I_{pE} are the electron and hole currents at the emitter contact, decreases from $\approx$0.98 to $\approx$0.88 if X_{jeff} is reduced from 0.2 μm to 0.15 μm.

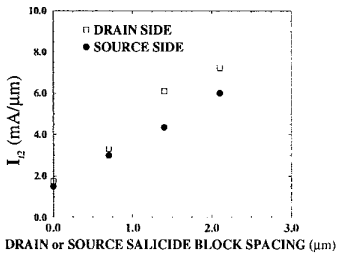

Figure 12: *I_{t2} as a function of the salicide block spacing (Figure 2) on the drain side or the source side. Typical I_{drive} for these devices was 350 μA/μm with L_{gate} = 0.49 μm.*

Conclusion

We have shown that salicides and the local substrate potential impact ESD performance by influencing the lateral *npn* behavior. A protection circuit design with ESD levels > 2kV in a 0.35 μm process is presented, which uses a vertical *pnp* to utilize the benefits of increased local substrate potential on the fully-salicided lateral *npn* behavior. This approach allows the design of area-efficient, high performance ESD protection, which can be compatible with mixed-voltage requirements, in fully-salicided deep submicron technologies.

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