An Experimental 256-Mb DRAM with Boosted Sense-Ground Scheme

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Abstract—**In developing the 256-Mb DRAM, the data retention characteristics must inevitably be improved. In order for DRAM's to remain the semiconductor device with the largest production volume in the 256-Mb era, we must develop a cost effective device with a small chip size and a large process tolerance. In this paper, we propose the BSG (Boosted Sense-Ground) scheme for data retention and FOGOS (FOlded Global and Open Segment bit-line) structure for chip size reduction. We have fabricated an experimental 256-Mb DRAM with these technologies and obtained a chip size of 304 mm^2 and a performance of 34 ns access time.**

I. Introduction

DRAM's are the semiconductor device with the largest production volume because of their superiority of bit cost over other semiconductor memories. This superiority has been achieved by steady progress represented by a capacity increase of four times every three years while keeping compatible with the previous generation. Now experimental 256-Mb DRAM's have been reported [1]–[3], but to realize mass-produced 256-Mb DRAM's with the above mentioned compatibility, two big problems exist. One is the data retention characteristics and the other is the cost [4].

Fig. 1 shows the specified value of data retention time of 4-Mb to 256-Mb DRAM's. To keep the same refresh cycle interval as the previous generation (16 μs) while not increasing the power consumption, these values double every generation. In 16-Mb, two standardized data retention times have evolved, one as an extension from 4-Mb DRAM (32 ms/2 k refresh cycles), and the other to reduce power consumption (64 ms/4 k refresh cycles). But the real ability of each generation of DRAM's at most maintains that of the previous generation, generally becomes worse. This is because the stored charge in the memory cell decreases and the probability of mask-misalignment, which increases the leakage current, becomes large because of the reduction of the alignment margin and by a more complicated fabrication process. For 256-Mb DRAM's, a 256-ms data retention time will be required. It is a concern that there will be almost no margin between this value and the real ability. Therefore, the development of not the process but the design technology to improve the data retention characteristics is desired. In this paper, we propose the Boosted Sense-Ground (BSG) scheme to extend the data retention time from the viewpoint of circuit design for high density DRAM's [5].

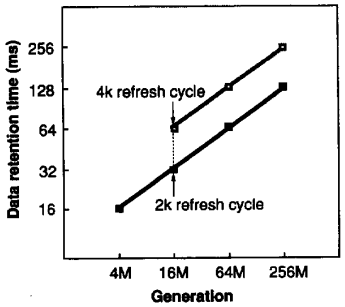

Fig. 1. Specified value of data retention time for standard DRAM's.

For low-cost, mass-produced devices are required to have a small die size with a simple memory cell structure and a large process tolerance. Hierarchical bit-line architecture is very useful in reducing the die size [6], [7]. In this paper, we propose a simple memory cell structure using the planar stacked capacitor with high dielectric constant film suitable for hierarchical bit-line architecture. We call this architecture the FOlded Global and Open Segment bit-line (FOGOS) structure [8].

In Section II, the BSG scheme is explained. The FOGOS structure is described in Section III. We have fabricated an experimental 256-Mb DRAM implementing these technologies, and the experimental results are shown in Section IV.

II. Boosted Sense-Ground (BSG) Scheme

A. Memory Cell Access Transistor

In this subsection, we discuss the requirements for the memory cell access transistor.

To restore the full V_{cc} level (bit-line "H" level) to a memory cell, the boosted word-line level (V_{WLH}) must be higher than $V_{cc}+V_{th}(V_{cc})+\alpha$, where α is the voltage margin and $V_{th}(V_{cc})$ is the threshold voltage of the memory cell transistor when the source voltage is V_{cc}. For transistor reliability, V_{WLH} should be as small as possible. This means that $V_{th}(V_{cc})$ is required to be small. In a long cycle operation, the "H" data stored in an unselected memory cell connected to the "L" sensed bit-line is exposed to worst case leakage conditions. In this situation, the signal charge stored in the memory cell leaks away more rapidly due to the subthreshold leakage current of

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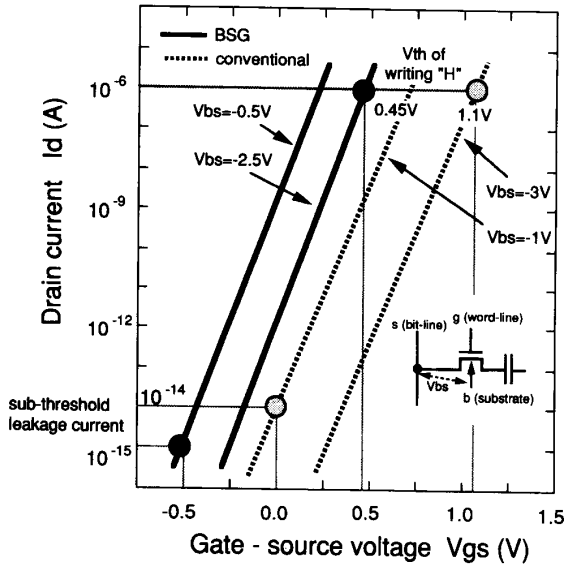


Fig. 2. I_d (drain current) $-V_{gs}$ (gate-source voltage) characteristics of memory cell access transistors.

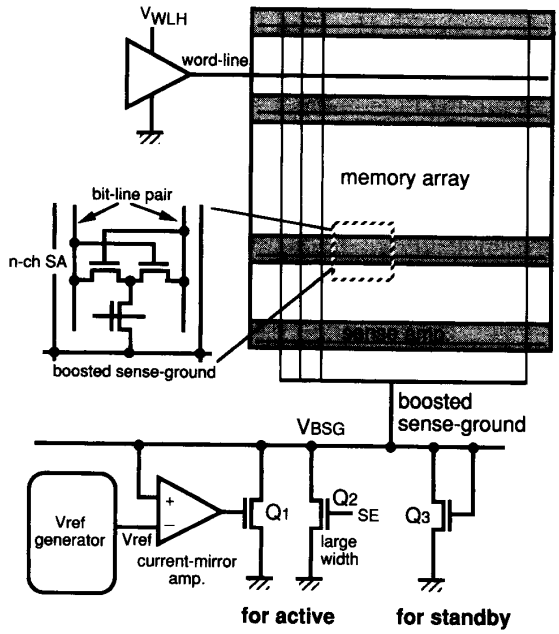


Fig. 3. The BSG circuits.

the memory cell transistors being in its maximum state from a biasing perspective. This results in degraded data retention characteristics. There are many factors which degrade the data retention characteristics such as the subthreshold leakage current, the leakage current through isolation regions, and that through the capacitor dielectric film, etc. In general, the cell structure is primarily designed and developed in order to suppress these kinds of leakage currents sufficiently when compared to the junction leakage current mentioned later. Therefore, the subthreshold leakage current must be low enough that it determines the minimum value of $V_{\rm th}(0)$ [9]. To meet with these two requirements of threshold voltage, the substrate generally has a back bias voltage, $V_{\rm bb}$, applied to suppress the body effect.

The dotted lines in Fig. 2 show the characteristics of a memory cell access transistor optimized for the conventional scheme. The bit-line swing is assumed to be 2 V, which is determined by the reliability of the high dielectric constant film of the memory cell capacitor mentioned below in section III and by a low power dissipation requirement. The $V_{\rm bb}$ is set at -1 V. The $V_{\rm th}$(2 V) becomes 1.1 V, therefore, the $V_{\rm WLH}$ must be no less than 3.1 V. In this case, the p-n junction's reverse voltage between the substrate and the storage node of the "H" data stored memory cell becomes -3 V. The larger this reverse voltage is, the larger the junction leakage current becomes. To extend the data retention time we must suppress the junction leakage current while keeping a low subthreshold leakage current. As for junction leakage current, it is desirable to make the $V_{\rm bb}$ small, but this doesn't meet the requirement of suppressing the sub-threshold leakage current.

B. The Concept of BSG Scheme

To reduce the junction leakage current and obtain a low subthreshold leakage current and a low boosted word-line voltage level, we propose the Boosted Sense-Ground (BSG) scheme. This scheme has the feature that the "L" level of the bit-line swing is slightly boosted. This level is called the BSG level, and is set at 0.5 V in the discussions in this paper. In a long cycle operation, the sub-threshold leakage current is drastically reduced for the negative gate-source voltage, $V_{\rm gs}$. When the sub-threshold swing [10] is 80 mV/decade, the subthreshold leakage current will be reduced by 6 orders of magnitude. So, by sacrificing a part of this excessive improvement, we can both make the $V_{\rm bb}$ small and lower the threshold voltage.

The solid lines in Fig. 2 show the characteristics of a memory cell access transistor optimized for the BSG scheme by reducing the channel impurity concentration. The $V_{\rm bb}$ is 0 V, and the bit-line swing is 2 V, which is the same as conventional schemes. Therefore, the bit-line "H" level is 2.5 V and the $V_{\rm th}$(2.5 V) becomes 0.45 V. Thus, the $V_{\rm WLH}$ must be no less than 2.95 V, which is lower than that of conventional schemes in spite of the higher bit-line "H" level. The subthreshold leakage current is one order of magnitude smaller, too. And the p-n junction voltage between the substrate and the storage node of "H" data stored memory cell becomes -2.5 V, which is smaller than is conventional, and therefore the junction leakage current decreases and the data retention time is expected to become longer.

C. The BSG Circuit and Simulated Results

Fig. 3 shows the BSG circuits. The BSG line is connected to n-channel sense amplifiers through the sense amplifier drive transistors and placed over the memory array like a mesh pattern [11]. The BSG level is generated by the reference level generator, which is the same circuit used in the internal power

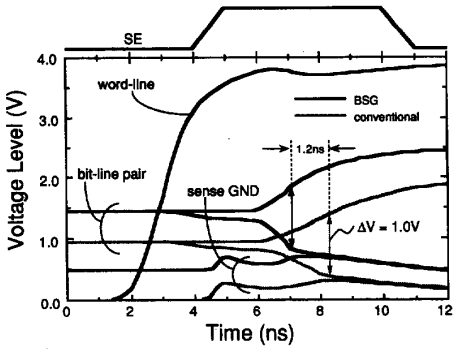


Fig. 4. The simulated wave forms in sensing period.

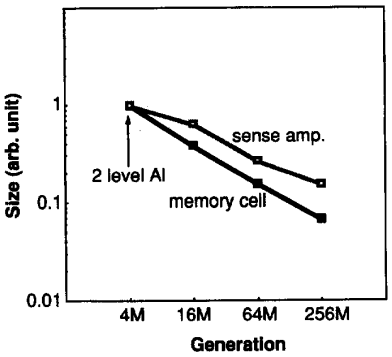


Fig. 6. The size reduction trend of memory cells and sense amplifiers.

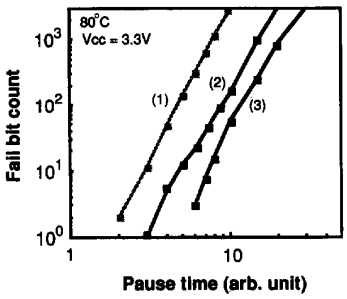


Fig. 5. Pause refresh characteristics measured by the test device. (1) Conventional scheme with $V_{bb} = -1.5$ V, (2) BSG scheme with the same threshold voltage of memory cell access transistor as conventional scheme, (3) BSG scheme with low threshold voltage transistor.

supply voltage generator [12]. The differential amplifier, which is the current mirror type, is made inactive in the standby state so as not to increase the standby current. The BSG level is clamped to the threshold voltage of the n-channel transistor by $Q3$. The large width n-channel transistor, $Q2$, which is controlled by the signal SE, is made to be on at the beginning of sensing period to suppress an unnecessary rise in the BSG level by the sensing current. The ground line for supplying the charge to the BSG line is fully separated from other ground lines, therefore the current flow from the ground line to the BSG line does not affect other circuit operation.

Fig. 4 shows the simulated wave forms of the sensing period. Solid lines indicate the BSG scheme and shadow lines indicate the conventional. Compared to the conventional case, the data read-out speed on the bit-line is not delayed in spite of the higher bit-line precharging level for the sake of a lower threshold voltage of the memory cell transistor. The sensing speed of a 1–V bit-line swing becomes 1.2 ns faster owing to the large n-channel transistor controlled by the SE and the higher bit-line precharge level. Thus an unnecessary rise in the BSG line is suppressed.

D. The Data Retention Characteristics

We applied the BSG scheme to a test device with a 0.5-μm design rule and measured the data retention characteristics. Fig. 5 shows the data retention characteristics with no disturbance, which were the number of fail bits counted by varying the pause time. In this figure three conditions of data are shown. These are: (1) the conventional scheme with $V_{bb} = -1.5$ V, (2) the BSG scheme with the same threshold voltage of memory cell access transistor as the conventional scheme, and (3) the BSG scheme with the low threshold voltage transistor. In all conditions the bit-line "H" level is set at 3.3 V, thus in the BSG scheme, the bit-line swing is 2.8 V, which is 0.5 V smaller than that of (1). The time to the first bit failure of (2) is 1.5 times longer than (1) in spite of the smaller signal charge, which is due to the effect of the smaller p-n junction voltage. Furthermore, in case (3), the time to the first bit failure is an additional two times longer compared to condition (2) because of the reduction in the channel impurity concentration which lowers the threshold voltage. Therefore, using the BSG scheme, the data retention time is three times longer than the conventional scheme.

In the 256-Mb DRAM, the same order of improvement will be expected for the BSG scheme by optimizing the memory cell transistor.

III. FOGOS (Folded Global and Open Segment Bit-Line) Architecture

A. The Hierarchical Bit-line Architecture

Fig. 6 shows the size reduction trends of memory cells and sense amplifiers for 4-Mb to 256-Mb DRAM's. The sense amplifier region includes the I/O gates, bit-line precharging and equalizing transistors, and bit-line isolation transistors. Memory cell size has been reduced to 40% of the previous generation by both the design rule reduction and the three-dimensional structure. On the other hand, the sense amplifier size has been reduced only 55% of the previous generation. Therefore, the size ratio of sense amplifiers to memory cells of 256-Mb DRAM's will be about 2.5 times larger than that of 4-Mb DRAM's. It is therefore very difficult to maintain the trend of chip size reduction for 256-Mb DRAM's. A simple solution for this problem is to reduce the number of sense amplifiers in order to increase the number of memory cells connected to each sense amplifier. However, this makes the bit-line capacitance large, which brings about an access

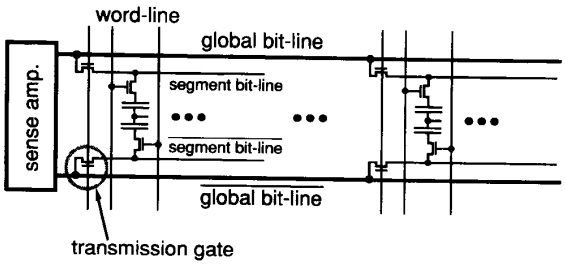


Fig. 7. The concept of hierarchical bit-line architecture.

time delay, a reduction of sensing margin, and a larger power dissipation.

Hierarchical bit-line architecture achieves a chip size reduction with no performance penalty. Fig. 7 shows the concept of hierarchical bit-line architecture. The bit-line is divided into two portions. One is the segment bit-line to which the memory cells are connected, and the other is a global bit-line which is connected to the sense amplifier. Each segment bit-line is connected to each global bit-line by a transmission gate. And for low total bit-line capacitance and resistance, the global bit-line must be made of a thin, low resistivity metal such as tungsten. The number of cells per segment bit-line and the number of segment bit-lines per global bit-line are decided by the memory cell structure.

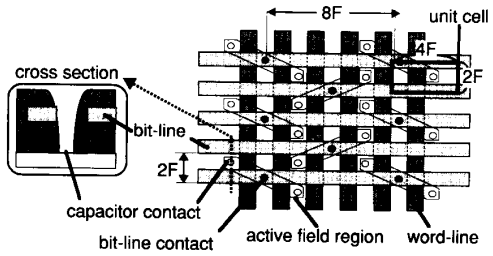
B. Memory Cell Structure

We have developed a planar stacked capacitor with a high dielectric constant film for 256-Mb DRAM's. This high dielectric film is $(Ba_{0.75}Sr_{0.25})TiO_2$ with a cell size of 0.72 μm^2 utilizing 0.25-μm process technology.

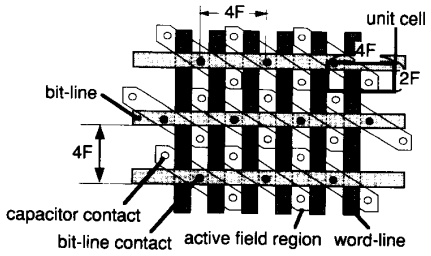
Fig. 8 shows the two types of memory cell pattern layout. One is the open-type where the memory cells are placed on every cross point of the word-line and segment bit-line. The other is the folded-type where the cells are placed alternately on the cross points. These two types of cells are both $8F^2$ cells where F is the feature size, which is the minimum design rule (0.25 μm) + alignment tolerance (0.05 μm). Compared to the folded type, the open type has two major advantages for process tolerance concerning the memory cell arrangement. These are: (1) the large lithographic alignment tolerance of storage-node contact hole openings for the segment bit-lines, and (2) a large space tolerance of more than $2F$ between the contact holes of cells. This type also has another major advantage: the reduction of the parasitic capacitance of the segment bit-line per unit cell. This is because the length is half and the pitch is two times larger than that of the folded type. The wide pitch of the segment bit-line also reduces the bit-line coupling noise.

C. FOGOS Structure

Using this type of memory cell, we have developed the new FOGOS array architecture which is shown in Fig. 9. The pair of global bit-lines is arranged in the same direction, and the pitch is $2F$, which is the same as the bit-line pitch of



(a)



(b)

Fig. 8. Layout pattern of memory cell. (a) folded type. (b) Open type.

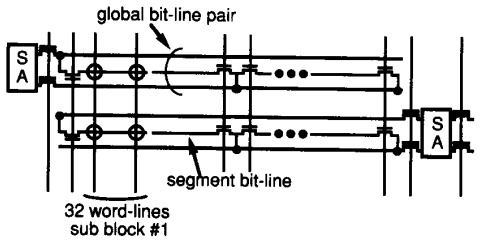


Fig. 9. FOGOS structure.

conventional folded bit-line architecture. The global bit-line is composed of pure tungsten 50 nm thick and fabricated after the memory cell fabrication process.

Thirty-two memory cells are connected to each segment bit-line, and 32 segment bit-lines plus two spare segment bit-lines for the X-line and block replacement are connected to each global bit-line pair. For a further reduction in chip size, we adopted the shared sense amplifier scheme, in which each sense amplifier is shared by both sides of the global bit-line pairs. The total bit-line capacitance is suppressed to 150 fF, and the chip size is reduced by over 10% compared to the conventional folded bit-line architecture with 128 cells per bit-line.

This FOGOS structure has a large potential for cost reduction in spite of adding one extra layer for the global bit-line. There are three major reasons, which are: (1) the reduction in die size without using a smaller design rule, (2) the decrease in process steps for fabricating the memory cells by adopting

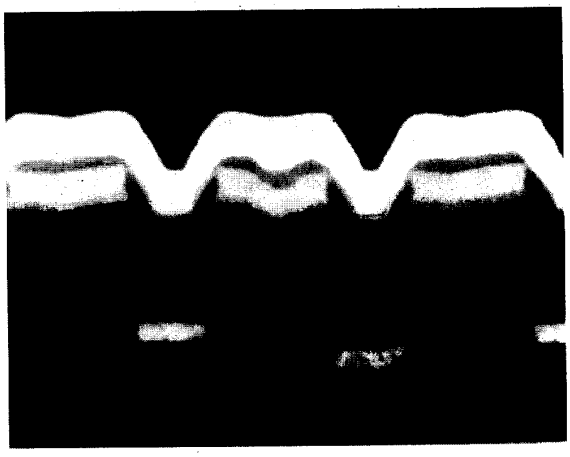


Fig. 10. Cross-sectional SEM photograph of the memory cell.

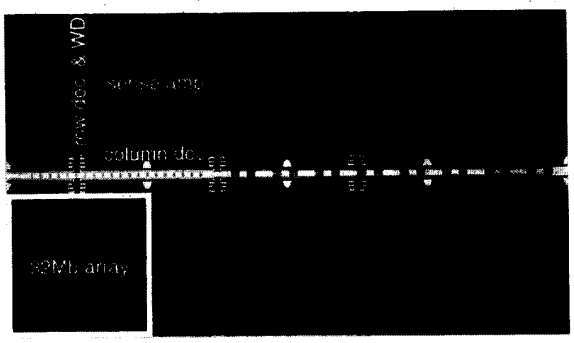


Fig. 11. Photomicrograph of the 256-Mb DRAM.

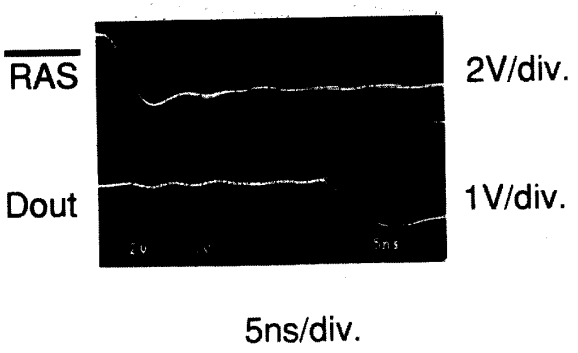


Fig. 12. Operating waveforms.

TABLE I
CHIP FEATURES

Organization	32 MW x 8b
Technology	KrF excimer 0.25 μm CMOS triple level metalization (1W 2Al)
Memory cell	Planar Stacked with BSTO film 0.6 x 1.2 = 0.72 μm^2
Chip size	13.32 x 22.84 = 304 mm^2
Supply voltage	3.3 V
Access time	34 ns
Active current	62 mA (tc = 90ns)
Standby current	60 μA
Refresh cycle	16384

a simple cell structure using high dielectric film, and (3) the increase in yield for the large alignment margin in the memory cell arrangement.

IV. THE EXPERIMENTAL 256-Mb DRAM

We fabricated an experimental 256-Mb DRAM incorporating both the BSG scheme and a FOGOS structure with high-dielectric constant film cells using 0.25-μm CMOS technology. Fig. 10 shows a cross-sectional SEM photograph of the memory cell capacitor. The equivalent SiO_2 thickness of high dielectric film is 0.47 nm, and the memory cell capacitance is 25 fF. The die photograph is shown in Fig. 11. The chip size is $13.32 \times 22.84 = 304$ mm^2. Fig. 12 shows the operating wave forms measured under typical conditions. We obtained a 34-ns RAS access time.

Table I summarizes the features of the device. KrF excimer laser lithography is used. The power supply voltage is 3.3 V, which is regulated to 2.5 V internally.

V. CONCLUSION

Improving the data retention characteristics are very important in developing the 256-Mb DRAM, and, to make it a cost effective mass-produced device, we have reduced the chip size while maintaining a large process margin. To achieve this, we developed the BSG scheme for data retention, and the FOGOS structure for chip size reduction.

We have fabricated an experimental 256-Mb DRAM with these technologies and have obtained good results. We can confirm that these technologies are very effective for not only the 256-Mb era but also beyond. Furthermore, the BSG scheme is also an effective technology in obtaining the low power DRAM's of smaller capacity.

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