DYNAMIC GATE COUPLING OF NMOS FOR EFFICIENT OUTPUT ESD PROTECTION

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Abstract

A dynamic gate coupling effect to increase the electrostatic discharge (ESD) protection efficiency of NMOS output devices is reported. As this paper shows, if the gate is dynamically held above threshold, the brief NMOS turn-on elevates the substrate potential to uniformly trigger all the parallel *npn*s of the MOSFET. Using this effect, good ESD protection for the grounded substrate logic chip outputs can be obtained even with silicided diffusions.

I. Introduction

During the last few years, the effective design of ESD protection circuits has become particularly challenging. This is mainly because the rapid advances in process technologies have had an adverse impact on protection circuit efficiency. For example, compared with devices using conventional source/drain junctions, the use of lightly doped drain (LDD) structures has been proven responsible for the degradation of ESD failure threshold levels in thin oxide and thick oxide devices.[1-3] Compounding this, silicided diffusions increase the surface heating in MOS devices under ESD conditions and further degrade ESD performance.[2-4]

CMOS SCR protection devices[5] can overcome these negative effects on ESD for input pins but are not reliable for outputs. For example, a low-voltage SCR for output protection was recently reported in Reference 6, but its effective trigger requires an isolation n-well resistor, which can degrade the output buffer circuit performance. Also, with the advent of 0.5-μm technologies, the CMOS SCR may not trigger reliably due to the use of thinner epi layer substrates.

As described in this paper, a dynamic gate coupling effect can be used for the output NMOS itself to make it robust for ESD protection. This technique is effective for both LDD and silicided technologies.

Section II presents the output NMOS ESD background information. This includes device behavior under advanced process options and protection phenomena for grounded substrate (used in logic chip design) versus floating substrate (used in DRAMs).

Section III discusses the gate coupling phenomenon for NMOS transistors and its effect under ESD transient conditions. A dynamic gate-coupled device is studied to understand and use the gate coupling effect. This paper presents the complete phenomena and results for nonsilicided devices (with both LDD and conventional source/drain), as well as for silicided structures. The measured ESD stress results are given in Section IV. Section V explains the gate coupling effect and device operation under ESD using modeling and simulation results. The design issues for optimum output ESD protection are also briefly discussed. Finally, Section VI summarizes the conclusions of this work.

II. Output ESD Background

In VLSI chips, the large NMOS output buffer transistor itself can be used as the protection device. The device operates as a parasitic bipolar *npn* with the drain as the collector, the substrate as the base, and the grounded source as the emitter. The basic I-V characteristics of a grounded gate device are shown in Figure 1. Here V_{t1} is the collector-base breakdown voltage of the *npn* with the emitter open-circuit or BV_{bo}. During the ESD event, the device operates mostly in the snapback mode where V_{sp} is the clamping voltage. At higher stress levels, the device could go into the second breakdown region where filament formation is encouraged and device failure eventually occurs. Since, under reverse bias, the heat generated at the drain junction could elevate the temperature at the contact metalization, moving the contact away from the drain diffusion edge can minimize the drain-to-source melt filament failures and improve the ESD protection level.[7] Also, to provide uniform current density and maximize the protection level, ladder structures are used where the MOSFET gates are laid as parallel fingers. For example, the ladder structure layout and the critical contact-to-gate spacing ("A") are shown in the inset of Figure 4. When these techniques are used, more than 10 V/μm of protection has been reported for outputs with conventional source/drain structures.

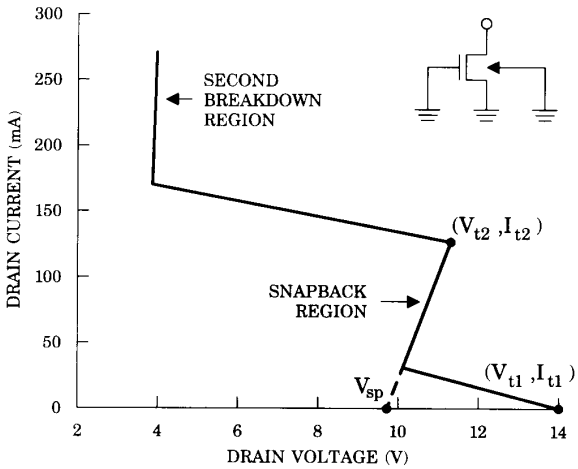
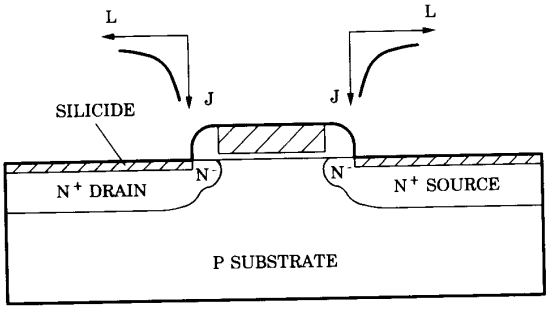


Figure 1. Typical I-V curves for an NMOS device showing snapback and second breakdown.

For advanced processes involving LDD junctions, output device ESD performance degradation has been widely reported. It is believed that the relatively shallow LDD junctions increase current density and, even with reduced electric fields (a feature of these devices), still result in a higher $\bar{J} \cdot \bar{E}$ product and, hence, a lower failure threshold level.[8] Typically, with the LDD junctions, the NMOS protection level could be about 8 V/μm. Various process modifications have been recently reported to overcome the "LDD effect" and restore the output ESD levels.[9-11]

The "silicide effect" appears to be more disastrous. Here, the use of silicided drain and source diffusions, implemented for



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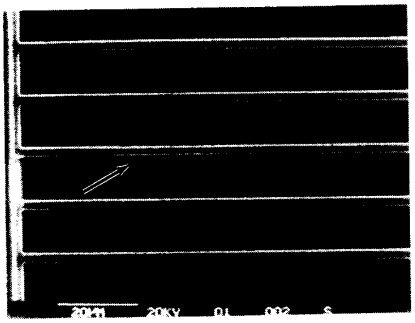

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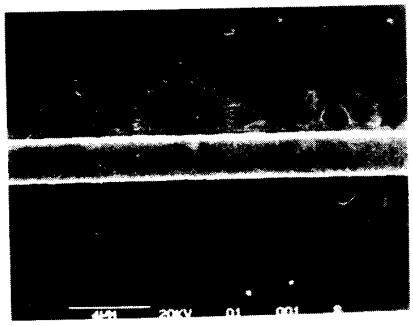

(C)

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Figure 2. The current density in a silicided device (A), the failure mode in a grounded gate silicided NMOS (B), and the symmetrical source/drain melt filament (C).

reduced source and drain contact resistances, caused the ESD levels to degrade below the acceptable 2-kV level for the human body model (HBM). The clad diffusions modify source/drain resistance owing to the effect of silicide/silicon interface[12] and result in nonuniform current density.[4] Figure 2 shows that the peak current density occurring at the drain and source sidewall edges (Figure 2a) leads to the well-known symmetric melt filament at both drain and source (Figures 2b and 2c). For the silicided devices, the NMOS device performance could be about 5 to 6 volts/μm.[13] To overcome the "silicide effect," process changes have been tried but with only minimal effect. Blocking the silicide formation with a mask at the ESD protection device is an expensive option.

As noted above, process advances reduce the NMOS device protection capability per micron. Even then, this figure of merit is still high enough to obtain greater than 4-kV protection with about an 800-μm-wide device. However, the ESD failure distribution is broader, usually having a 2-kV low-end failure threshold even for large output devices. For IC chips with CMOS or NMOS buffers, the ESD performance is generally limited by the NMOS pull-down device. In these large NMOS output devices with multiple parallel fingers, uniform conduction of all parasitic bipolar devices is difficult to achieve.[13] For the case of grounded substrate logic chips, this can lead to low ESD performance as described in the following paragraphs.

For DRAM chips with floating substrates, only small amounts of substrate current can raise the substrate potential during an ESD event turning on all lateral bipolar devices for uniform conduction. Effective ESD performance of floating substrate DRAM outputs has been reported.[14] For grounded-substrate logic chips, the source of the NMOS is closely tied to the substrate potential, making it difficult for uniform turn-on of all fingers. As will be shown in this paper, if the substrate potential can be locally increased during ESD by incorporating momentary MOS action, better parasitic bipolar trigger levels can also be achieved for grounded substrate logic chips.

Figure 3 shows the NMOS characteristics for a 1.6-μm device as measured with constant current pulses. Here, the gate is grounded for both grounded and floating substrates. As noted, the breakdown voltage is high at about 16 volts with an 8-volt snapback. In a multifinger MOSFET device, if one parallel *npn* turns on first and clamps at 8 volts, all current would have to be conducted by this device before the pad voltage builds up enough to turn on the next parallel finger. These two would then conduct the current, followed by the third device turn-on, etc. It is possible that the failure current might be reached before all of the fingers have had a chance to participate, thus reducing the protection level. In actuality, one or two fingers turning on into snapback would probably provide enough trigger current for subsequent finger turn-on. But this can be a random event and especially difficult for grounded substrate chips. For example, Figure 4 shows the ESD failure distribution for a 20-finger grounded gate device with 50-μm-wide fingers. The estimated number of fingers turning on to provide the measured protection level is also indicated. As shown, the random nature of multifinger turn-on gives unreliable ESD performance with a broad distribution. For silicided devices, the multifinger turn-on is much less effective and most failures occur between 800 and 1,200 volts.

For the above reasons, a grounded gate MOSFET is not a desirable protection structure. As shown in the next section, a dynamic gate coupling effect can be used to achieve uniform conduction and, hence, improved ESD performance for grounded substrate logic outputs. The effectiveness of this technique is clearly demonstrated for both silicided and nonsilicided processes.

III. Gate Coupling Effect

The effect of gate bias on the ESD performance of NMOS devices has been reported in a limited manner.[13,15,16] Reference 15 claimed that with large gate bias (5 to 8 volts) the increase of

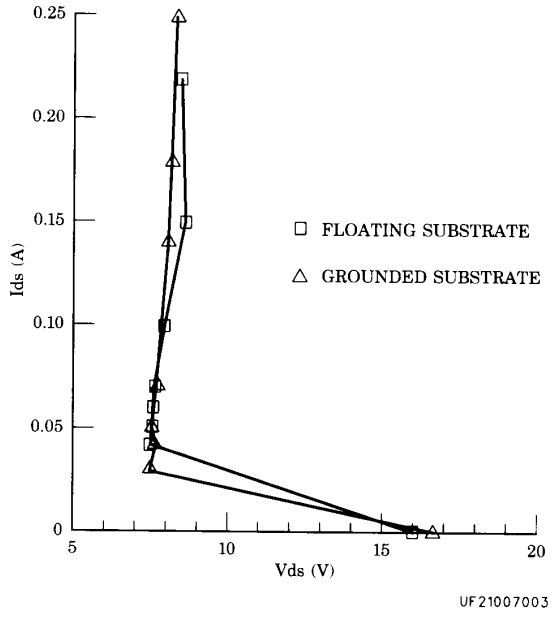


Figure 3. The I-V breakdown curves of a 500/1.6-μm grounded gate NMOS.

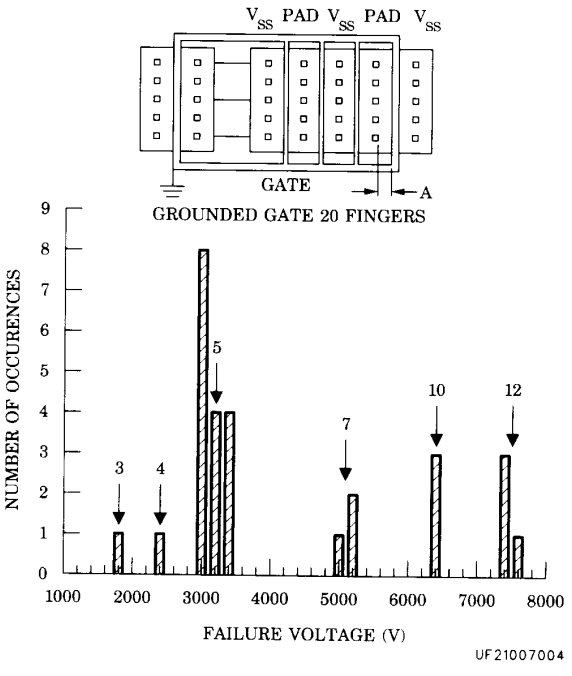


Figure 4. ESD-HBM failure threshold distribution for a 1,000/2-μm grounded gate NMOS with 20 fingers. The number of fingers turning on is also indicated.

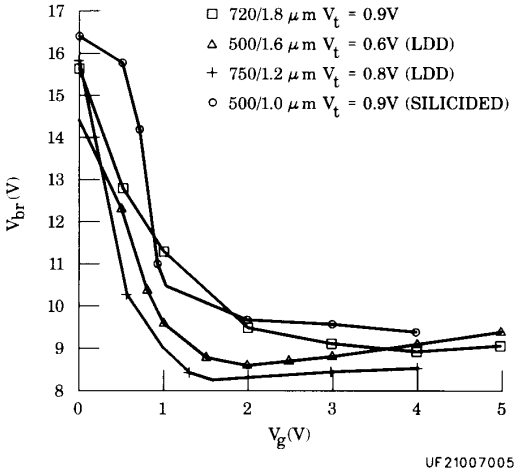


Figure 5. NMOS breakdown with gate bias for four different technologies.

snapback voltage results in increased power dissipation and, hence, reduced failure threshold level. The work of Reference 13 showed that with a gate bias of about 1 volt the NMOS trigger is lowered to less than the onset voltage for second breakdown (i.e., V_{t1} to be less than V_{t2} in Figure 1) and is therefore ideal for improved ESD performance. The authors also noted that if the gate voltage goes above 5 volts, the parameter I_{t2} in Figure 1 decreases, which could mean a reduced failure threshold level. Finally, Reference 16 investigated the gate bias dependence of ESD failure threshold for a single-finger NMOS and an optimum gate bias was noted. For the present work, we investigated in detail a multifinger NMOS device to show that an ideal dynamic gate coupling can effectively maximize the ESD performance of an output buffer transistor.

Figure 5 shows the well-known behavior of gate bias on the NMOS breakdown.[17-19] This figure plots the NMOS breakdown (with the substrate grounded) as a function of the gate bias for four different technologies. The zero bias breakdown value is commonly referred to as BV_{dss}. It is obvious that with a gate bias slightly above the transistor threshold voltage (V_t) the breakdown voltage is minimized. The substrate current generated by the MOS action helps to forward bias the source-substrate junction, thus lowering the trigger breakdown. The maximum substrate current condition will typically occur at around 2 to 4 volts on the gate. (Note that the current level at which we measure the breakdown more or less determines the actual shape of the curves in Figure 5.) However, as the gate bias increases, the substrate current is reduced and the breakdown voltage begins to increase slightly as noted in the figure.

For all of the technologies shown here, a similar approximate reduction of 6 volts in the breakdown occurs with a gate bias of 1 to 2 volts. This lowering should increase the efficiency of the multifinger turn-on of the NMOS device. This contrasts the grounded gate case because, even if only one finger turns on first, a smaller voltage buildup will quickly trigger subsequent fingers. Thus, all the fingers will rapidly participate before the device reaches failure current levels.

Figure 6 shows a structure fabricated to study the gate coupling effect, where a field oxide device (FOD) is added to the thin oxide device gate. The metal gate of the FOD directly connects to the pad so that when it reaches its threshold, it can discharge the

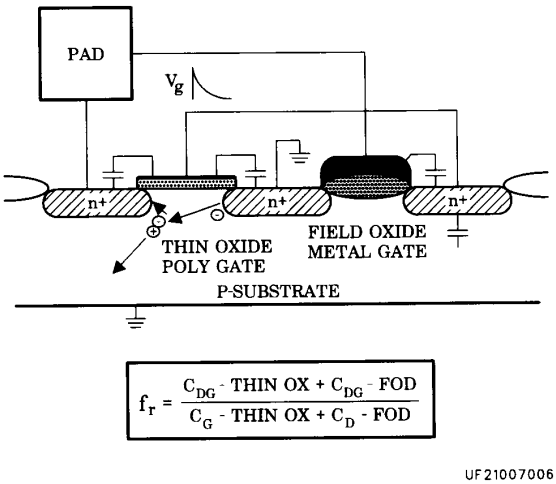


Figure 6. Cross section of a dynamic gate-coupled device. The feedthrough capacitance ratio is given as f_r.

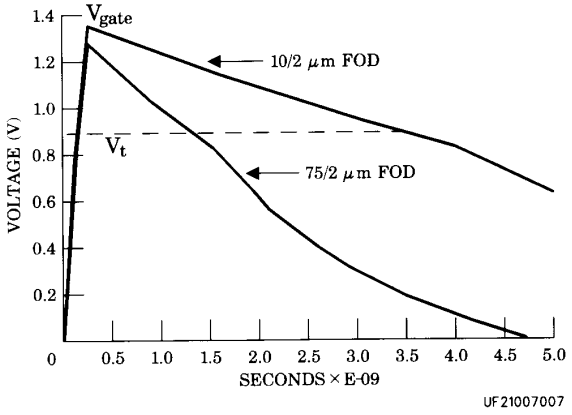


Figure 7. Simulated gate-coupling effects for a 500/1.0-μm NMOS.

thin oxide gate to ground. With the ESD transient, the thin oxide device gate is capacitively coupled upward and, as soon as the MOS device goes through its snapback, the gate is capacitively pulled down again, resulting in a transient pulse. Under this transient of the gate, the drain is at a high potential and the gate is above V_t, which is adequate for impact ionization and the subsequent generation of electron-hole pairs.

The holes collected by the substrate would elevate the local substrate potential to facilitate the uniform turn-on of all MOSFET fingers. Figure 7 shows a typical SPICE simulation of the transient pulse on the gate for two different sized FODs. Section V presents more detailed simulations to further explain the full device operation. The actual amount of gate coupling is determined by the feedthrough ratio of the capacitances (f_r) as indicated in Figure 6. For the devices studied, this ratio is about 0.1, giving 1 volt on the gate for every 10 volts on the drain. As seen from the simulation curves in Figure 7, with a larger FOD the feed-through ratio is reduced and results in a slightly lower gate coupling. Nevertheless, what is critical is the time during which the gate bias stays above the transistor V_t.

The effectiveness of the device performance at high ESD levels seems to depend on how well the gate is dynamically controlled, as will be discussed later. At higher stress levels, high voltage spikes at the pad (about 25 to 30 volts as indicated in Figure 17) will turn on the field oxide gate to control the thin oxide NMOS gate transient. If the gate is turned off too fast, the ineffective mode of grounded gate behavior is reached before all of the fingers of the NMOS have a chance to turn on. On the other hand, if the NMOS gate stays on too long after the *npn* snapback, the surface conduction could result in premature failure. This latter phenomenon seems to be more prevalent in silicided devices.

Figure 8 shows the I-V breakdown characteristics for two dynamic gate-coupled devices. The breakdown curves, measured with 150-ns current pulses,[20] are given for a transistor with 1.0-μm silicided/LDD process. The breakdown occurs at about 8.5 volts, which is 7 volts lower than the BV_{dss} breakdown voltage in Figure 5. Referring to the silicided process curve in Figure 5, this corresponds to more than 1 volt for the gate bias. From the simulations in Figure 7, this gate coupling should be higher with a smaller FOD. In the case of the smaller FOD in Figure 8, the minimal transition from trigger to snapback indicates that the coupling indeed is higher. Note that after snapback, the on resistance is low

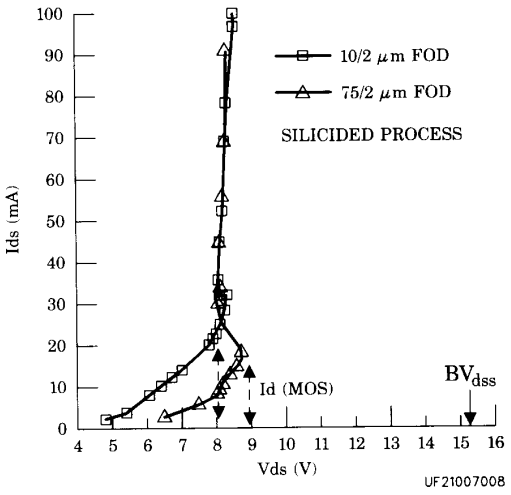


Figure 8. I-V breakdown curves for a dynamic gate-coupled device with the 1-μm silicide process. The NMOS is 500/1 μm.

and is less than 10 ohms. Before snapback, the MOS drain conduction can be seen as indicated by I_d (MOS). In this condition, the drain is near 8 volts and the gate is above V_t, leading to substrate current, which helps to a uniform turn-on of all fingers as noted above.

Similar gate coupling results were obtained for nonsilicided devices. As mentioned earlier, the amount of gate coupling depends on the overlap capacitance and the oxide capacitance for a given technology. For a 1.2-μm technology, the gate coupling appears higher than for 1.6-μm technology. Figure 9 shows the I-V breakdown curves for 1.2-μm technology. The inferred gate coupling is about 1.4 volts. For the 1.6-μm technology, Figure 10 compares the I-V breakdown curves for grounded gate devices with a gate-coupled device. The trigger voltage reduced from 15 V for the grounded gate case to 9.5 volts for the dynamic gate-coupled case, corresponding to only about 1.1 volts on the gate (refer to Figure 5). This is still adequate for effective ESD protection as will later be shown.

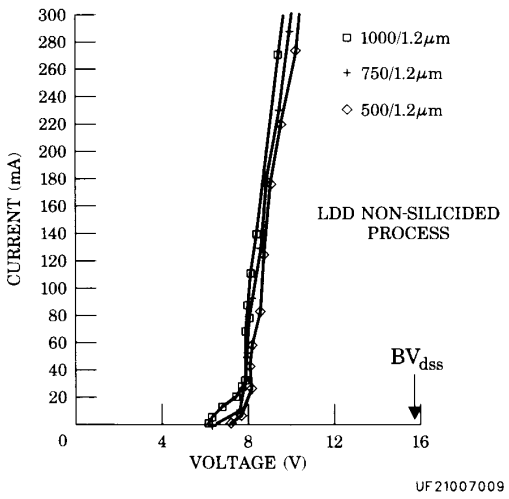


Figure 9. I-V breakdown curves for dynamic gate-coupled devices with the 1.2-μm LDD process.

Considering Figure 10 in detail, it is more interesting to note that, for the grounded gate cases, the on-resistance is larger, indicating that only a few fingers have turned on. This is further evidenced by the fact that second breakdown and device failure occur when a critical current level reaches around 600 to 700 mA. A translation to the HBM gives a failure level of less than 2 kV. However, for the gate-coupled case, the current level could be increased to more than 3 A without a failure because almost all fingers participate in the ESD current conduction. In fact, the multiple finger turn-on can be seen by closely observing the local voltage maxima (as indicated by the arrows) in the expanded view of the gate-coupled device curve as shown in the inset of Figure 10.

As described in this section, dynamic gate coupling to slightly above the transistor V_t is enough to facilitate uniform turn-on of most MOSFET fingers. The following section presents the actual ESD data to confirm this statement.

IV. ESD Results

The ESD stress data on all devices were taken for the HBM with positive stress with respect to V_{ss}. The data presented here apply to both silicided and nonsilicide devices to illustrate that the same concept will work.

A. Silicided Devices

Figure 11 shows the ESD data for silicided MOSFETs with the gate grounded and gate dynamically coupled. For the grounded-gate case, only 1 or 2 of the total fingers (10) turned on. For the gate-coupled devices, most of the fingers seem to successfully turn on, therefore giving the best protection. When the device width doubles from 500 to 1,000 μm, the ESD level also nearly doubles, thus demonstrating that the number of on-fingers increases. For gate-coupled devices, the size of the FOD controls how long the gate stays on above V_t. This, in turn, can determine how many fingers uniformly participate in the ESD event.

Once an optimum design is obtained, the failure distributions can be tighter than shown for the 1,000-μm-wide case in Figure 11. In general, the gate should stay above V_t for 5 to 10 ns or equal to about the rise time of the ESD event. Experiments have shown that on-times shorter than 2 ns gave rise to low-end failure distributions and longer than 20 ns gave erratic failure distributions. This was especially true for silicided devices. Possibly, for silicided transistors, if the gate stays on too long after bipolar

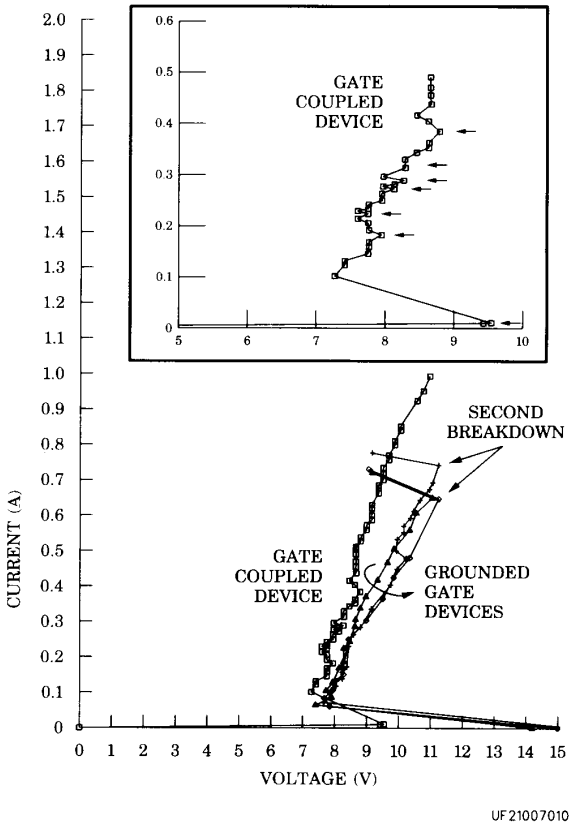


Figure 10. Comparison of a dynamic gate-coupled device with grounded gate devices for the 1.6-μm LDD process. All devices are of the same width. The multifinger turn-on for the gate-coupled device is indicated in the inset.

turn-on, the combination of the MOS and bipolar conductions would increase the localized $\bar{J} \cdot \bar{E}$ product at a point close to the silicide layer (see Figure 2). This occurrence would increase the probability for device failure to occur at lower than expected stress levels. However, if the gate is effectively turned off after uniform conduction is reached, the ESD current conduction is confined only to the bulk, reducing this effect.

As described above, uniform finger turn-on yielded good ESD levels for the silicided devices. Further study verified that a local increase of the substrate injection level produces uniform finger turn-on. We obtained verification by floating the substrate and obtaining failure distributions similar to those of Figure 11. Furthermore, uniform finger turn-on is dramatically illustrated for silicided devices through failure analysis. Figure 12 shows the fail mode with 5.2-kV failure stress level for the 1,000-μm device. The figure clearly shows that the silicide damage occurs on most of the fingers, in contrast to the grounded gate device in Figure 2b, where the failure site appears on only one finger. Further, Figure 12 shows the expected symmetrical damage site patterns on the multifingers.

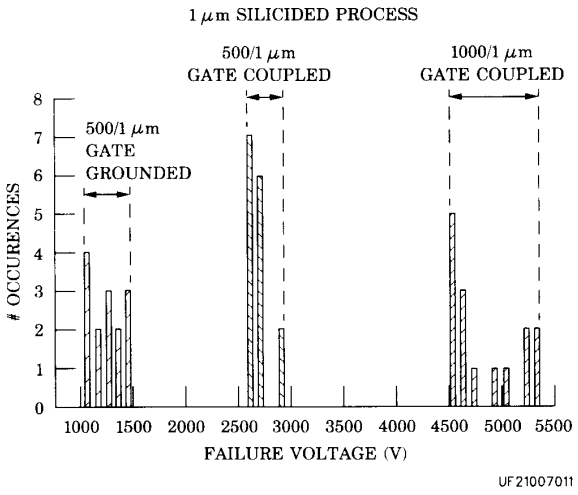


Figure 11. ESD-HBM performance of dynamic gate-coupled devices with grounded substrate for a 1-μm silicided technology.

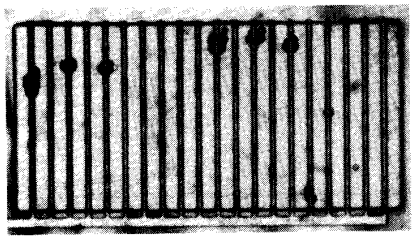


Figure 12. Failure sites for 1,000/1-μm dynamic gate-coupled device with silicided diffusions after 5.2-kV stress.

B. Nonsilicided Devices

Figures 13 and 14 demonstrate the effectiveness of this gate coupling on ESD for 1.2- and 1.8-μm nonsilicided processes, respectively. For the 1.2-μm devices in Figure 13, failure distributions improve with increased device width. However, the finger turn-on efficiency seems to be only about 60 to 80 percent. Note that, for the 1,000-μm device, the high end of the distribution is somewhat truncated due to the ESD tester limit. Figure 14 shows similar results for the 1.8-μm devices. Here, for all device widths, the same number of fingers (6) was used. For the grounded gate case, only 1 or 2 fingers turned on, whereas nearly 5 to 6 fingers turned on for the 480-μm gate-coupled device.

Figure 14 shows that the efficiency again slightly drops off for the wider devices, indicating that further device optimization is needed by adjusting the FOD size. Nevertheless, it is interesting to note that both of the LDD/nonsilicided devices of Figures 13 and 14 achieve a minimum of 10 volts/μm ESD performance. In contrast, for the silicided devices, about 5 to 6 volts/μm was obtained, as seen from Figure 11. Thus, the results here showed that the use of dynamic gate coupling can produce nearly the maximum NMOS ESD performance for a given technology.

V. Modeling, Simulations, and Design

The dynamic gate-coupled device reported here can be effective for output ESD protection. This section presents a better understanding of the device function through modeling and simulations.

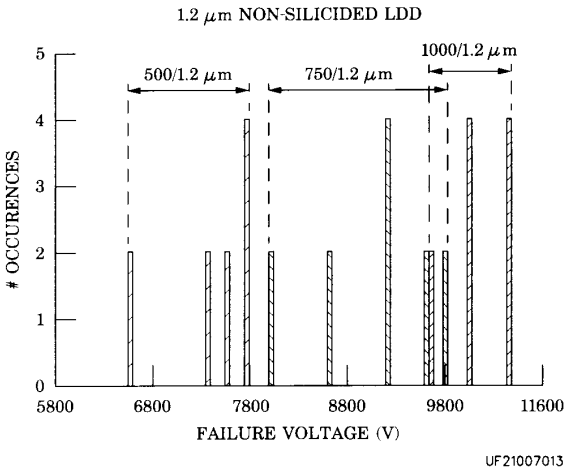


Figure 13. ESD-HBM performance of dynamic gate-coupled devices with grounded substrate for the 1.2-μm LDD process.

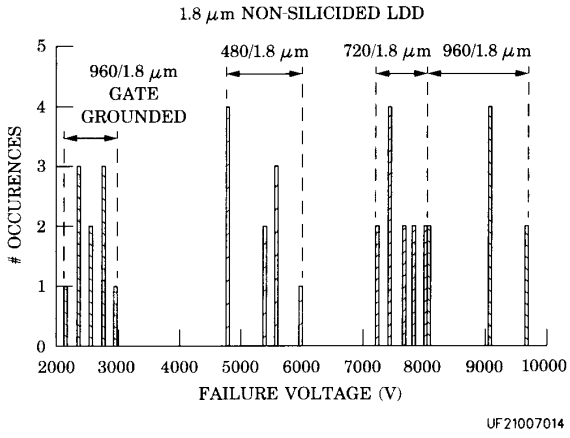


Figure 14. ESD-HBM performance of dynamic gate-coupled devices with grounded substrate for the 1.8-μm LDD process. A grounded-gate device is also shown for comparison.

To quantify the transient phenomena during an ESD event for the gate-coupled device in Figure 6, both device-level and circuit-level simulations were done. Figure 15 shows the equivalent circuit used for the simulations where the HBM stress model is represented by the 1,500-ohm resistor and the 100-pF capacitor. The figure presents MOS thin-oxide (ThinOx) devices and FODs with their parasitic bipolar transistors Q_1 and Q_2, respectively. The base resistors in the figure model the resistance from a depth of 2 μm below the silicon-silicon-dioxide interface down to the backside contact. Their value, per unit length of device width, is 5,882 ohm-μm. The capacitor C_{osc} represents the scope probe capacitance used to monitor the pad waveform. We assumed a 10-ns rise time as shown in the figure for the ESD waveform generated by the ESD tester. The circuit-level model parameters for

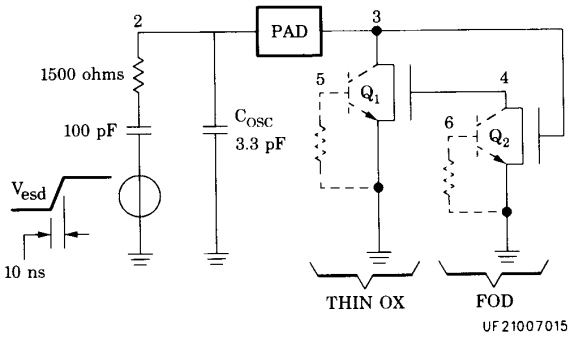


Figure 15. The equivalent circuit for modeling and simulation of a dynamic gate-coupled device. The ESD HBM model is represented by the 1,500-ohm resistor and the 100-pF capacitor. C_{osc} represents the scope probe capacitance.

the parasitic bipolar transistors were determined with two-dimensional (2-D) device simulations using PISCES–IIB.[21] Figure 16 shows the characteristic curves for a 3- by 2-μm cross section of the ThinOx parasitic bipolar transistor (Q_1) device. From these curves, the circuit level bipolar transistor parameters were computed and used for the iSMILE[22] circuit simulations. As expected, PISCES simulations for the FOD parasitic bipolar transistor (Q_2) revealed negligible current gain owing to the FOD's longer channel length.

Using the simulation and modeling techniques proposed in Reference 23, we simulated the equivalent circuit of Figure 15. Figure 17 shows the transient analysis results of a 5-kV ESD discharge on a 1,000/1-μm ThinOx device (10 fingers, V_t = 0.85 V) coupled with a 75/2-μm FOD (V_t = 15.0 V). Here, I_{esd} is the ESD current with the expected RC exponential decay of 150 ns. Note that the simulated pad voltage (V_{pad}) goes to more than 20 volts and decays with I_{esd}. For a qualitative comparison, the measured pad voltage waveform under similar conditions is shown in the inset of Figure 12. The peak pad voltage is determined by the peak ESD current, the ThinOX breakdown voltage, and the drain and source contact resistances of the ThinOX device. As the voltage drop across the drain and source contact resistance decreases with decreasing I_{esd}, the pad voltage also decays.

As will be shown, the ThinOx device conducts only for a short time. Therefore, once the ThinOx device's bipolar transistor moves out of snapback, there is no path to ground to continue the discharge process. The value eventually approached by the pad voltage is close to the snapback voltage , as explained in Reference 23. The exponential decay of the discharge current is also responsible for the waveform shape of the internal active base voltage (V_3) of the bipolar transistor up to the point where the base-collector avalanche process is non-negligible. Finally, note that the ThinOx gate voltage, V_4, increases initially as a result of the feedthrough but then is clamped once the pad voltage is high enough for the FOD to go above threshold, thus removing the charge out of the gate. As the pad voltage decays, the FOD goes below its threshold near 170 ns, leaving the ThinOx gate only capacitively coupled to the drain-source terminals. The pad voltage waveform of Figure 17 indicates the time points at which the FOD and the parasitic bipolar device of the ThinOx transistor (Q_1) stop conducting.

Figure 18a shows the net gate-source and active-base-source voltages of the ThinOx device. Figure 18b gives a magnified plot of the first 20 ns. The gate-source voltage increases due to feedthrough until the bipolar transistor goes into breakdown at approximately 1 ns. Eventually, at 3.5 ns when the pad voltage is large enough for the FOD to go above threshold, the gate begins to discharge. Overall, the FOD size and the capacitive coupling to

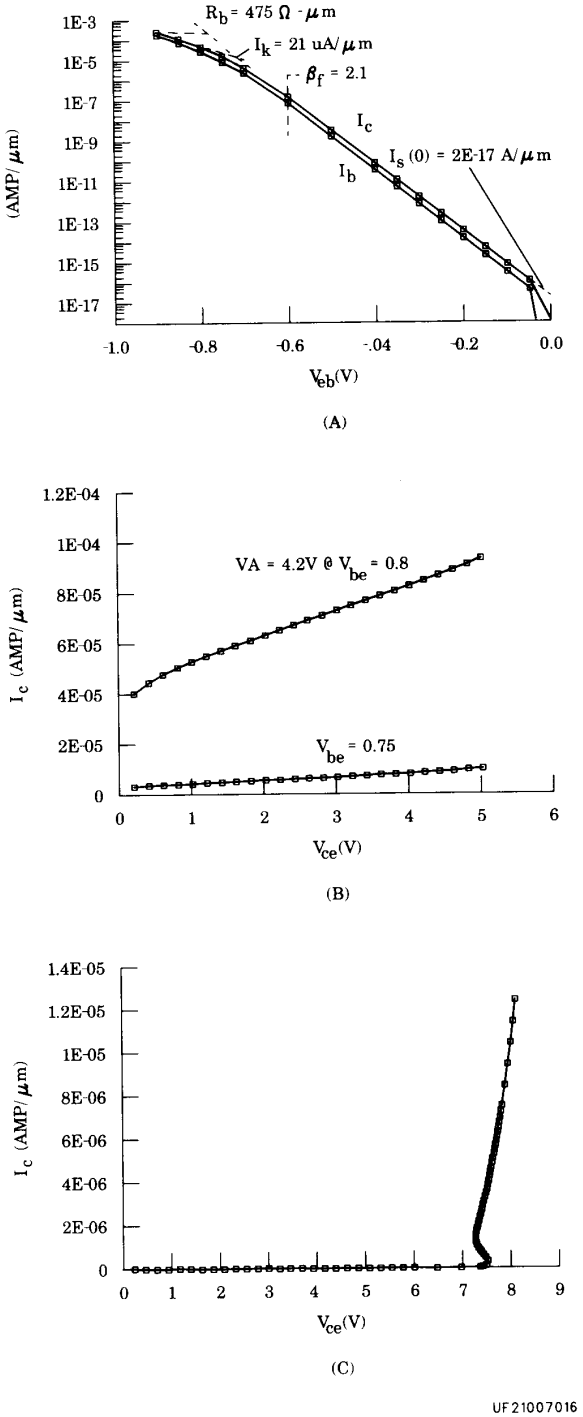


Figure 16. The PISCES dc bipolar characteristics for the ThinOx parasitic device bipolar transistor Q_1 in Figure 15. Base and collector currents versus V_{ce} as a function of V_{be} in (b), and collector current versus V_{ce} in (c).

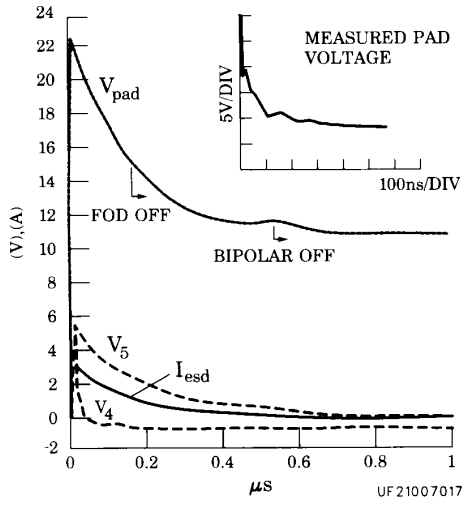


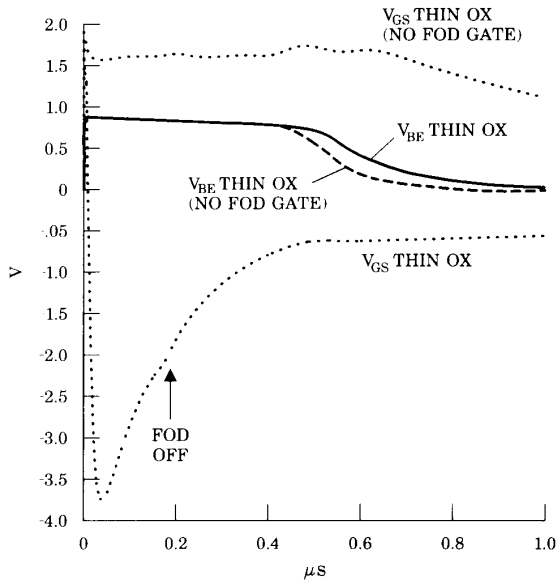
Figure 17. Simulated waveforms for the nodes indicated in Figure 15 for 1,000/1-μm silicided NMOS and 75/2-μm FOD. The ESD stress level is 5 kV. The measured waveform at the pad is shown in the inset.

the pad control the discharge rate of the ThinOx gate capacitance. As noted from Figure 17, the FOD remains on until about 170 ns. But since the ThinOx device gate goes above threshold only during the first 8 ns, the discharge process is completely controlled by its parasitic bipolar transistor action until it comes out of snapback at 0.5 us. After this point, the discharge is handled by the ThinOx drain-substrate junction without any transistor action. The base-emitter voltage waveform in Figure 18a clearly indicates the parasitic bipolar transistor conduction time period.

These simulations assumed that the substrate potentials of the ThinOx and the FOD devices are independent as reflected by the circuit topology used in Figure 15. In view of this, the negative-going waveforms for both the ThinOx device gate voltage V_4 and the ThinOx device gate-source voltage can be explained as follows.

Referring to Figure 17, the ThinOx gate voltage V_4 increases during the rise time of the ESD waveform in response to the combined effect of the gate feedthrough and the voltage drop across the ThinOx device's source contact resistance. At 3.5 ns, the FOD goes into conduction, initiating the ground discharge of node 4. At 40 ns, node 4 reaches the ground level and stays there until the FOD goes out of conduction at 170 ns. With the FOD off, the ThinOx gate (node 4) is only capacitively coupled and, therefore, is driven to a negative level as a result of the decreasing pad voltage. After reaching a minimum of about −0.654 volts at around 190 ns, the ThinOx gate (node 4) is slowly brought back to zero by the forward-biased FOD drain-substrate junction.

Referring to Figures 18a and 18b, during the first few nanoseconds of the discharge when none of the devices is conducting, the ThinOx gate-source voltage reaches a maximum value of 1.63 volts due to the feedthrough. Then, the ThinOx gate-source voltage starts decreasing once the FOD goes into conduction. At the point near 40 ns, the gate-source voltage reaches a minimum of −3.76 volts due to voltage drop across the ThinOx source resistance. Note that this minimum corresponds to the ThinOx gate voltage (V_4 in Figure 17) reaching the ground level as explained above. For the rest of the FOD conduction period and corresponding to the plateau observed in the ThinOx gate voltage waveform, the gate-source voltage increases due to the feedthrough of the decreasing pad voltage. When the FOD goes off, at



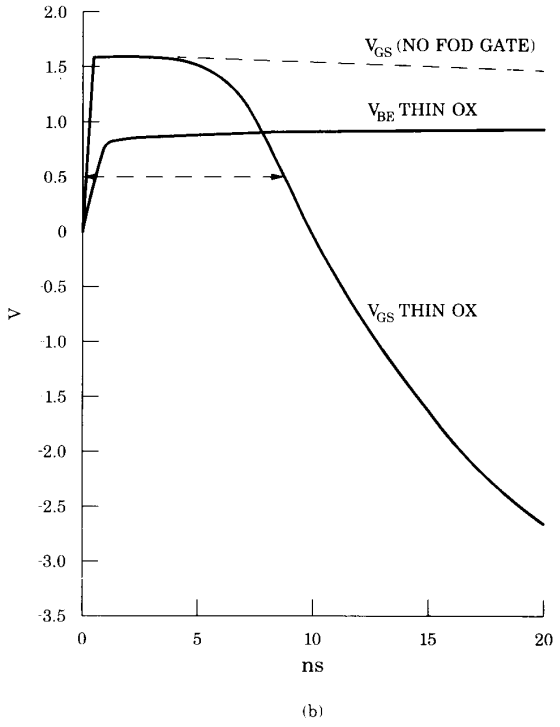


Figure 18. Simulated waveforms of the net gate-source voltage and V_{be} for 1,000/1-μm silicided ThinOx and 75/2-μm FOD in Figure 15. An expanded view for the first 20 ns is given in Figure 18b. In both 18a and 18b, the dashed lines represent the case where the FOD gate is disconnected.

approximately 170 ns, a small disturbance is observed in the ThinOx gate-source waveform (Figure 18a), which then slowly approaches the 0 volt level due to forward-biased FOD drain-substrate junction.

For comparison, Figures 18a and 18b also show the waveforms that would be observed if the FOD gate were disconnected. Note that the ThinOx device would remain above threshold all along the discharge. As a consequence, even though most of the discharge current would again be handled by the ThinOx parasitic bipolar transistor (Q_1), it is possible to observe an appreciable reduction in the conduction period of the parasitic bipolar transistor. Although not shown in Figure 17, the FOD with no gate would cause the pad voltage to approach 0 volt by the ThinOx MOS action.

Figures 19a and 19b correspond to a structure with a 300/2-μm FOD for the same ThinOx device and is shown here for comparison with Figure 18. Figure 19b again shows a magnified view of the first 20 ns. Note that the main differences between these two cases relate to the ThinOx device gate-voltage waveforms. Since the FOD size is much larger in Figure 19, not only is the ThinOx transistor gate-source peak voltage smaller but also the discharge rate of the gate oxide capacitance is considerably increased. For the 300/2-μm FOD case, the ThinOx device gate stays above threshold only during the first 2 ns. Although the individual bipolar device does turn on in about 1 ns, it is assumed that it will take a few nanoseconds for the multiple fingers of the ThinOX protection device to uniformly turn on. For this reason, it would seem that 5 to 10 ns should be allowed for the ThinOx gate to be above V_t. Indeed, ESD testing has shown that the gate-coupled device with 300-μm FOD had low-end failure distributions, while the device with 75-μm FOD showed consistently good results. If, on the other hand, we remove the FOD device gate (the dashed line in Figure 18b), the gate of the ThinOx would stay on too long and again result in low-end failure distributions. This was also verified with experiments. Therefore, the gate needs an optimum on-time for consistent ESD performance. This can be easily designed even using simple SPICE simulations. In actuality, how long the gate needs to stay above V_t is determined by parameters such as contact resistance, the number of fingers in the design, etc. For this reason, initial experimental results are needed to establish the appropriate simulation criterion.

The dynamic gate-coupling concept described in this paper can produce effective output ESD protection. The device of Figure 6 can either be a dummy protection device or the output transistor itself. In the former case, an n-well resistor to ground needs to be tied to the gate since, otherwise, any voltage trapped on the floating gate can result in output pin parametric leakage. However, as noted in this section, the gate of the protection device should ideally stay above V_t for 5 to 10 ns. Therefore, the chosen RC time constant of the resistor must meet this requirement. In the latter case, when used as the output device itself, the interference from the predrivers must be simulated. This is critical for CMOS outputs where V_{cc} comes on through the p-channel diode almost instantaneously with the ESD event and operates the predrivers. Then, detailed circuit level simulations become necessary to optimize this protection structure.

VI. Summary

The ESD performance of grounded logic chip outputs has been of a serious concern during the last decade with the introduction of LDD and silicided technologies. As described in this paper, the uniform trigger of all the parallel *npn*s of an output NMOS is the key to achieve good and consistent ESD performance. To improve the ESD levels of outputs in logic chips with grounded substrate, we reported a dynamic gate-coupling technique using an FOD. The size of the FOD controls the amount of gate coupling on the NMOS thin oxide transistor, as well as the transient pulse width of the gate above the transistor threshold voltage (V_t).

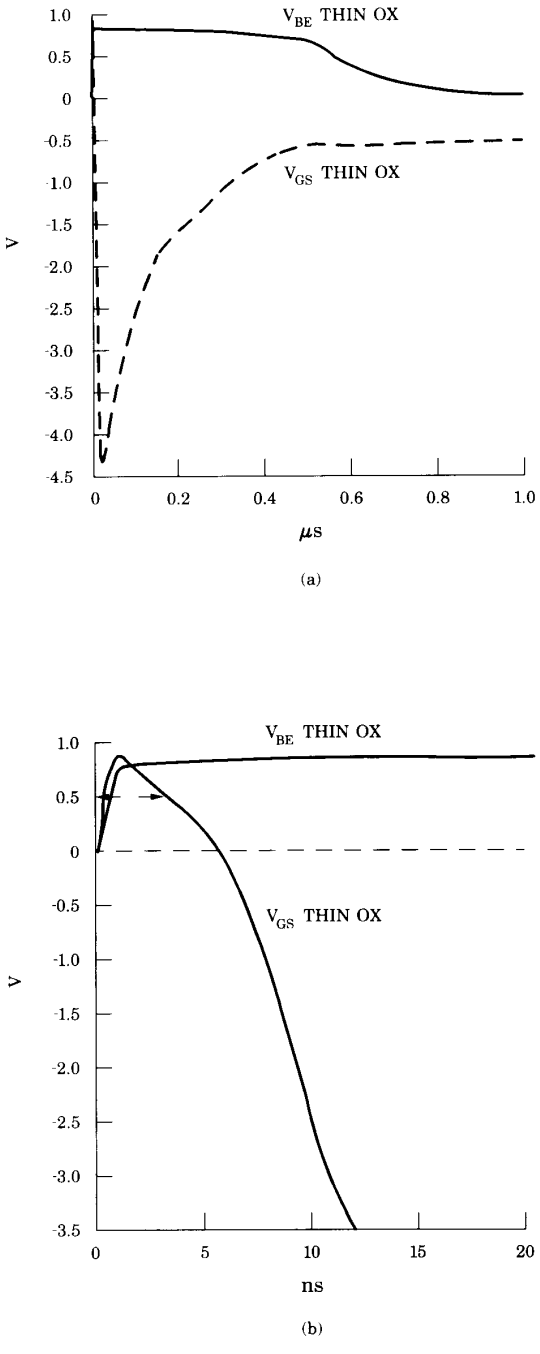


Figure 19. Simulated waveforms of the net gate-source voltage and V_{be} for 1,000/1-μm silicided NMOS and 300/2-μm FOD in Figure 15. An expanded view for the first 20 ns is given Figure 19b.

The use of this gate-coupling lowers the *npn* finger breakdown, allowing more of the NMOS fingers to participate in the ESD event. We demonstrated this with both pulsed I-V characteristics and the actual ESD stress data. For the silicided technologies, the proposed gate coupling technique resulted in more than 5 volts/μm with good device width dependence. Moreover, failure analysis results confirmed the multifinger turn-on for the silicided devices. For the nonsilicided devices also, this technique proved effective, resulting in more than 10 volts/μm of ESD performance.

To understand the device function and to investigate the design issues involved, this paper presented detailed device and circuit-level simulations. The results clearly indicated the dynamic nature of the gate transient and the role of the FOD size in controlling it. Coupled with experimental results, we concluded that for optimum ESD performance the gate transient needs to be such that the gate stays above V_t from 5 to 10 ns. Shorter times might make the uniform device turn-on ineffective and very long times will involve the MOSFET surface conduction after the bipolar *npn* turn-on, which increases the chances for low-end ESD failures. The design of the gate transient for optimum ESD, however, would depend on the technology used and the design of the output buffer itself. Combined with simulations, a matrix of test structures can be evaluated to find the optimum design for a given technology.

The dynamic gate coupling technique shown in this paper gave good ESD performance for even advanced process silicided output buffers. The technique can be effectively incorporated to the output buffer design since circuit-level simulations as proposed here might help the sizing of the FOD. An optimized use of this technique, as shown in this paper, can significantly enhance the output ESD of grounded substrate chips to the same level as the floating substrate DRAMs without having to incorporate additional protection devices.

Unless advances in the process technologies degrade the inherent ESD levels of *npn*s, there is promise that effective self-protection of outputs can be achieved. This protection concept could potentially also be useful for inputs or power bus protection. However, practical implementation would invariably involve experimental testing.

Acknowledgments

The authors would like to thank Mr. Bob Rountree, Dr. Amitava Chatterjee, Dr. Ajith Amerasekera, Dr. Shian Aur, and Dr. Ping Yang, all of Texas Instruments Incorporated; and Dr. Tom Polgreen of Dallas Semiconductor, for their valuable discussions. The authors would also like to express their gratitude to Professor Steve Kang of the University of Illinois for his support and direction on the modeling programs. Finally, the help of the Texas Instruments DSEG Publishing Services staff in preparing this manuscript is gratefully acknowledged.

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