Efficient On-Chip Delay Estimation for Leaky Models of Multiple-Source Nets

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ABSTRACT

On-chip interconnect nets are well modeled by RC trees. A *non-leaky* RC tree, containing no resistive paths to ground, is usually an adequate model for delay analysis. However, a *leaky* RC tree model, containing one or more resistive paths to ground, may be necessary for a net with more than one source gate. A source which is *inactive* must be modeled as a load on the *active* switching source, and it is this model for an inactive source which may contain a grounded resistor. This is particularly true in ECL "wired-or" circuits, where leakage effects due to the pulldown resistance of an output emitter-follower cannot be ignored. This paper consists of two main parts: 1) extension of circuit approximations for the driving-point admittance of a non-leaky RC tree to the case of a leaky RC tree; and 2) presentation of an efficient frequency-domain algorithm for computing the single-pole (Elmore) approximation for a voltage-transfer ratio in a leaky RC tree.

1. INTRODUCTION

On-chip interconnect delay consists of two components: 1) *"extra source" delay* through the active source gate, due to the loading effects of interconnect; and 2) *"propagation" delay* through the interconnect itself. Each component must be estimated accurately in order to produce an accurate estimate of the total delay due to interconnect.

Lumped circuit approximations for the driving-point admittance of a *non-leaky* RC tree have recently been developed [1]. These circuit approximations match the driving-point admittance of a non-leaky RC tree to a higher order in frequency than is possible using only a pure capacitance. Use of these higher-order approximations has proven to be important for accurately estimating the "extra source" component of interconnect delay, especially in nets where interconnect resistance is not dominated by the output impedance of the active source gate. In this paper, we show how to compute lumped circuit approximations for the driving-point admittance of a *leaky* RC tree.

The "propagation" component of on-chip interconnect delay is commonly estimated using a single-pole (Elmore) approximation [2,3] for the voltage-transfer ratio from the output of the active source gate to the input of a specified load gate. The presence of leakage resistance can greatly increase the computational cost of obtaining an Elmore approximation, since the resistance matrix (for a lumped network) can no longer be determined by inspection [4,5,6]. In [6], an algorithm with improved efficiency based on tree/link partitioning is presented, but it does not handle a leaky RC tree containing *distributed* segments. In this paper, we present a new algorithm for efficiently computing an Elmore approximation in a leaky RC tree which may contain any number of uniformly distributed RC segments. This algorithm works in the frequency-domain, and it owes much of its efficiency to the fact that intermediate results leftover from computation of the driving-point admittance approximation (discussed in the preceding paragraph) are reused.

2. DRIVING-POINT ADMITTANCE APPROXIMATIONS FOR LEAKY RC TREES

2.1 Computation of Lumped Circuit Parameters

We present three successively higher-order circuit approximations for the driving-point admittance of a leaky RC tree (see Fig. 1). Let $Y(s)$ denote the exact driving-point admittance of the tree. Within some circle of convergence, $Y(s)$ can be represented by its Taylor series expansion around $s=0$:

$$Y(s) = \sum_{n=0}^{\infty} y_n s^n. \tag{1}$$

For a non-leaky RC tree, $y_0=0$ and y_1 is equal to the total capacitance in the tree [1].

For $1 \le i \le 3$, the circuit approximation $Y_{APPi}(s)$ shown in Fig. 1 matches the expansion (1) to order i. The lumped circuit parameters for $Y_{APPi}(s)$ are a function of the first $i+1$ expansion coefficients, $\{y_0, \ldots, y_i\}$, of $Y(s)$:

$$i=1: \begin{cases} G = y_0 \\ C = y_1 \end{cases} \tag{2}$$

$$i=2: \begin{cases} G = y_0 \\ C = y_1 \\ R = -y_2/y_1^2 \end{cases} \tag{3}$$

$$i=3: \begin{cases} G = y_0 \\ C_1 = y_2^2/y_3 \\ C_2 = y_1 - \left(y_2^2/y_3\right) \\ R = -y_3^2/y_2^3. \end{cases} \tag{4}$$

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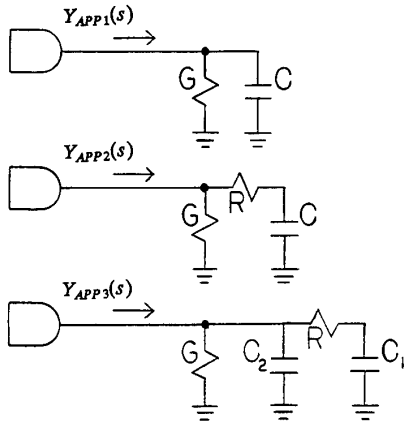

Figure 1: Lumped circuit approximations for the driving-point admittance of a leaky RC tree.

2.2 Computation of Series Coefficients

In (2)–(4), the first i+1 Taylor series expansion coefficients of $Y(s)$ are assumed to be known. In this section, we present an algorithm for computing up to the first four expansion coefficients. This algorithm starts at the leaf nodes of a leaky RC tree and works back to the source in a finite sequence of steps.

There are three rules which allow Taylor series expansion coefficients of the driving-point admittance *looking downstream of a given point in the tree* to be correctly propagated further upstream (see Fig. 2). Rules #1 and #2 involve upstream movement along a single branch, past respectively: a lumped conductance to ground (G), and a uniformly distributed RC segment (total resistance = R and total capacitance = C). Rule #2 also applies to upstream traversal of either a series lumped resistor (when $C = 0$) or a lumped capacitor to ground (when $R = 0$). Rule #3 involves combining two or more different admittance expansions in parallel at a branch point in the tree.

For each of these rules, denote the unknown admittance expansion (looking downstream from the point which is *immediately upstream* of the circuit element or branch point to be traversed) by:

$$Y_U(s) = \sum_{n=0}^{3} (y_U)_n s^n + o(s^4). \tag{5}$$

For rules #1 and #2, denote the known admittance expansion (looking downstream from the point which is *immediately downstream* of the circuit element to be traversed) by:

$$Y_D(s) = \sum_{n=0}^{3} (y_D)_n s^n + o(s^4). \tag{6}$$

For rule #3, let $B(\geq 2)$ denote the number of branches to be combined in parallel. Denote the B known downstream admittance expansions by:

$$Y_{Db}(s) = \sum_{n=0}^{3} (y_{Db})_n s^n + o(s^4) \; ; \quad 1 \leq b \leq B. \tag{7}$$

Rule #1 states that for upstream traversal of a lumped conductance to ground:

$$\begin{cases} (y_U)_0 = (y_D)_0 + G \\ (y_U)_n = (y_D)_n \; ; \quad 1 \leq n \leq 3. \end{cases} \tag{8}$$

Rule #2 states that for upstream traversal of a uniformly distributed RC segment:

$$\begin{cases} (y_U)_0 = (1+x)^{-1}(y_D)_0 \\ (y_U)_1 = (1+x)^{-2}\left[(y_D)_1 + C(1+x+\frac{1}{3}x^2)\right] \\ (y_U)_2 = (1+x)^{-2}(y_D)_2 - (1+x)^{-3}R\left[(y_D)_1^2 + C(y_D)_1(1+\frac{1}{3}x) + \frac{1}{3}C^2(1+x+\frac{2}{5}x^2+\frac{1}{15}x^3)\right] \\ (y_U)_3 = (1+x)^{-2}(y_D)_3 - (1+x)^{-4}R\left[2(y_D)_1(y_D)_2(1+x) + C(y_D)_2(1+\frac{4}{3}x+\frac{1}{3}x^2)\right] + (1+x)^{-4}R^2\left[(y_D)_1^3 + \frac{4}{3}C(y_D)_1^2(1+\frac{1}{4}x) + \frac{2}{3}C^2(y_D)_1(1+\frac{3}{5}x+\frac{1}{10}x^2) + \frac{2}{15}C^3(1+\frac{7}{6}x+\frac{4}{7}x^2+\frac{1}{7}x^3+\frac{1}{63}x^4)\right], \end{cases} \tag{9}$$

where the non-negative dimensionless quantity $x \equiv R(y_D)_0$. In the absence of leakage, $x = 0$ and (9) reduces to results presented in [1]. The expansion coefficient $(y_D)_1$ is first divided by $(1+x)^2$ and then is incremented by only a fraction, $\frac{1}{3} < \frac{(1+x+\frac{1}{3}x^2)}{(1+x)^2} \leq 1$, of the traversed capacitance (C). Hence, y_1 is typically *less than* the total capacitance in the tree.

Rule #3 states that for a parallel combination of B downstream admittances:

$$(y_U)_n = \sum_{b=1}^{B} (y_{Db})_n \; ; \quad 0 \leq n \leq 3. \tag{10}$$

Parallel admittances simply add together, and so do corresponding terms of their Taylor series expansions.

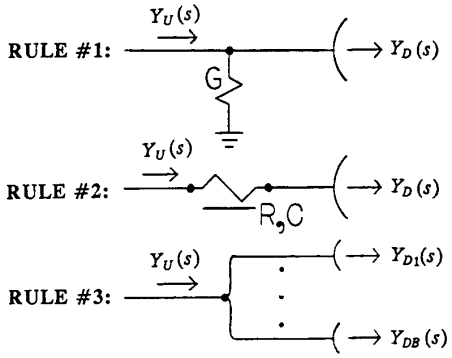

Figure 2: Three rules for upstream propagation of driving-point admittance expansion coefficients.

3. ELMORE APPROXIMATION FOR LEAKY RC TREES

Our algorithm for computing an Elmore approximation starts at the output of the active source gate and proceeds downstream, in a finite sequence of steps, to the input of a specified load gate. Two parameters, A and B, in an approximate voltage-transfer ratio, $H(s)=(A+sB)^{-1}$, are initialized to $A=1$ and $B=0$. Using information leftover from the upstream sweep for driving-point admittance coefficients (discussed in Section 2.2), the parameters A and B are modified as they are propagated downstream.

At each point in this downstream sweep, $H(s)$ represents the Elmore approximation (correct to first-order in the denominator) for the voltage-transfer ratio from the output of the active source gate to the present location. The parameter A is equal to the reciprocal d.c. gain. The "Elmore time constant" is equal to the ratio B/A. The rule for correctly propagating the parameters A and B downstream, past a uniformly distributed RC segment (total resistance = R and total capacitance = C), is illustrated in Fig. 3. This rule also applies to downstream traversal of just a series lumped resistor (when $C=0$).

Denote the unknown voltage-transfer ratio (from the output of the active source gate to the point which is *immediately downstream* of the segment to be traversed) by:

$$H_D(s) = (A_D + sB_D)^{-1}. \tag{11}$$

Denote the known voltage-transfer ratio (from the output of the active source gate to the point which is *immediately upstream* of the segment to be traversed) by:

$$H_U(s) = (A_U + sB_U)^{-1}. \tag{12}$$

Let $Y_D(s)$ denote the driving-point admittance looking downstream from the point which is *immediately downstream* of the segment to be traversed. If any lumped conductances and/or capacitances to ground are located immediately downstream of the segment to be traversed, these are also included in $Y_D(s)$. The expansion coefficients of $Y_D(s)$ are known, since driving-point admittance expansion coefficients have already been computed *at all points in the tree* during the upstream sweep described in Section 2.2. For the purpose of computing an Elmore approximation, it is necessary to reuse the first two expansion coefficients of $Y_D(s)$: the zeroth-order coefficient $(y_D)_0$, and the first-order coefficient $(y_D)_1$.

The rule for downstream propagation of an Elmore approximation expresses A_D and B_D as a function of:

1) A_U and B_U,
2) $(y_D)_0$ and $(y_D)_1$,
3) R and C of the traversed segment.

This rule states:

$$\begin{cases} A_D = A_U\left[1+R(y_D)_0\right] \\ B_D = A_U R\left\{(y_D)_1 + \frac{1}{2}C\left[1+\frac{1}{3}R(y_D)_0\right]\right\} \\ \qquad + B_U\left[1+R(y_D)_0\right]. \end{cases} \tag{13}$$

In the absence of leakage, the parameter A remains equal to 1 since $(y_D)_0 = 0$ in (13). In the absence of any *distributed* RC segments, an Elmore approximation computed using (13) with $C=0$ is consistent with the results of earlier works which apply only to *lumped* RC networks [3,4,5,6].

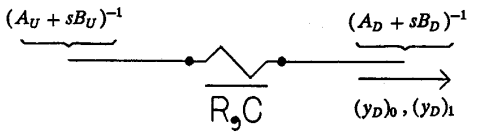

Figure 3: Rule for downstream propagation of an Elmore approximation.

4. RESULTS

The algorithms described in this paper have been implemented in software described in [7]. We show results of using these algorithms on an example ECL "wired-or" net shown in Fig. 4. The active source gate (between points A and B) drives a net containing an inactive source gate output (at point D) and a load gate input (at point C). Results are shown for a range of different metal lengths, L ($0 \le L \le L_{MAX}$), between points E and C. The distance between points B and E is equal to the distance between points D and E, and this distance remains fixed (at $L_{MAX}/28$). The RC model for our example net consists of:

1) a grounded capacitor at point B and a ramp voltage source attached to point B through a resistor (to model the active source gate),

2) the parallel combination at point D of a grounded resistor, a grounded capacitor, and a grounded d.c. current source (to model the inactive source gate output),

3) a grounded capacitor at point C (to model the load gate input),

4) 3 uniformly distributed RC segments (to model metal lengths between points B and E, D and E, and E and C).

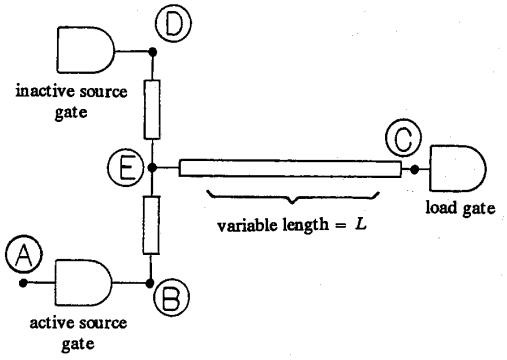

Figure 4: Example ECL "wired-or" net.

Figures 5, 6, and 7 plot respectively, as a function of the variable metal length L: delay through the active source gate from point A to point B (T_{AB}), propagation delay through metal interconnect from point B to point C (T_{BC}), and total net delay from point A to point C ($T_{AC} = T_{AB} + T_{BC}$). All plotted delays are for a rising transition, are measured at a *fixed* voltage threshold (near the middle of each waveform), and are normalized to $T_{AB}(0)$ (the value of T_{AB} when $L = 0$). In each plot, exact delay (in the RC model for Fig. 4) is compared to three different estimates. Three different estimates are obtained by using each of the three different driving-point admittance approximations described in Section 2.1. In Figures 6 and 7, the Elmore approximation described in Section 3 is used in conjunction with the three different driving-point admittance approximations.

In each of the three plots, the exact curve is nearly identical to the estimate curve obtained by using the third-order driving-point admittance approximation. As can be seen in the plots, the major source of error is estimation of T_{AB}, which requires use of the *third-order* driving-point admittance approximation to achieve acceptable accuracy over the entire range of lengths we consider. On the other hand, the *first-order* Elmore approximation is quite adequate for predicting T_{BC}; errors displayed in Fig. 6 are actually due to inaccurate waveforms at point B (obtained by using either the first- or second-order driving-point admittance approximation for too large a value of L).

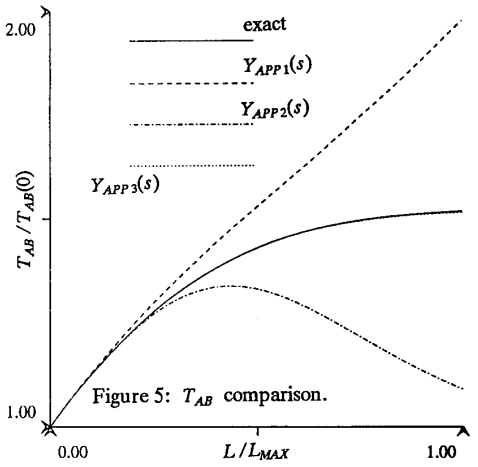

Figure 5: T_{AB} comparison.

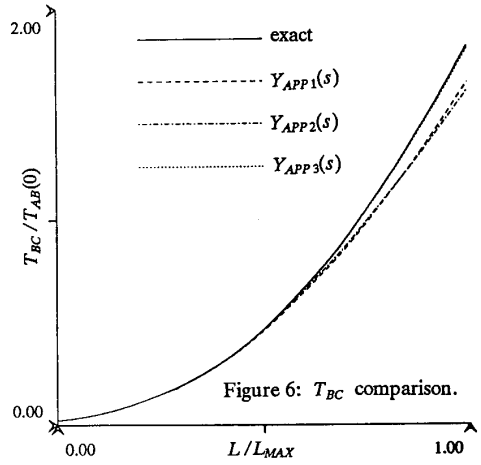

Figure 6: T_{BC} comparison.

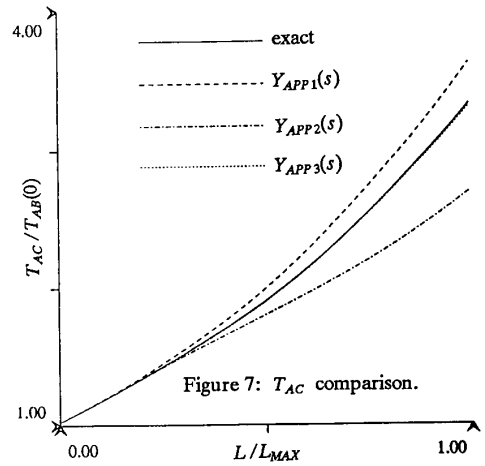

Figure 7: T_{AC} comparison.

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