SESSION 8: Static RAMs

TPM 8.4: A 20ns 4Mb CMOS SRAM with Hierarchical Word Decoding Architecture

Toshihiko Hirose, Hirotada Kuriyama, Shuji Murakami, Kojiro Yuzuriha, Takao Mukai,
Kazuhito Tsutsumi, Yasumasa Nishimura, Yoshio Kohno, Kenji Anami
Mitsubishi Electric Corp.
Itami, Japan

THIS 20ns 4Mb CMOS SRAM with both 4M x 1 and 1M x 4 organizations is fabricated using a quadruple polysilicon, double-metal and twin-well 0.6μm CMOS process technology. A word-decoding architecture and a sensitive sense amplifier combined with an address transition detector (ATD) technique realize high-speed, low-power operation.

In high-density SRAMs reported to date, the divided word line (DWL) structure accompanied by a block-sectioned memory cell array is widely adopted as a high-speed and low-power decoding method[1-4]. However, in SRAMs with more than 4Mb capacity, increase of block numbers will result in a large capacitance load on the global word line which drives local word decoders of each block. Therefore, conventional DWL structure will not be sufficient to realize the high-speed and low-power word decoding in future megabit SRAMs. Hierarchical word decoding (HWD) overcomes this problem.

Figure 1 shows a block diagram of the RAM. The 4Mb memory cell array which consists of 1024 rows and 4096 columns is divided into 32 blocks. Each block includes 1024 rows and 128 columns with two redundant columns. Figure 2 shows the HWD architecture used for the RAM. In this architecture, the word line (row select line) is divided into three levels: global, sub-global, and local. The global word line is selected by the global row decoder. The sub-global word line is activated by the sub-global row decoder according to the global word line and the block-group select signal. The local word line is selected by the local row decoder which generates logical AND of sub-global word line and block select signal. Though this architecture requires an extra decoding stage, the load capacitance of the global and sub-global word lines are reduced compared to the conventional DWL structure. Therefore, both propagation delay and charging/discharging current of word decoding path are reduced.

Figure 3 shows the bit line peripheral circuit. Signals BEQ, IOEQ, and SEQ are generated by the address transition detector (ATD) circuit and are used as equalization pulses for the read operation[5]. BEQ and IOEQ equalize bit lines and I/O lines, respectively. SEQ equalizes output nodes of sense amplifiers. Bit line loads consist of PMOS and NMOS in parallel connection. The voltage swing of bit line is determined by the PMOS load because the NMOS load is cut off with the bit line above Vcc-Vth. Therefore, the NMOS load, which has drive capability, can precharge bit lines rapidly after a write operation. The sense amplifier has two stages. The first stage is cross-coupled NMOS type, and second is a modified CMOS current-mirror type.

Figure 4 shows the data bus. Each block includes 16 sense amplifiers/write drivers, that is, a sense amplifier/write driver is placed in every eight columns and 16 internal data buses operate simultaneously. A 16-bit parallel test mode reduces test time.

The RAM has a fast address mode using the 16-bit parallel data bus scheme. As shown also in Figure 4, the fast address pins (Y3, Y4, Y5 and Y6 for 4Mx1/Y3 and Y4 for 1Mx4) are used to select the data bus connected to data-out buffer[3]. In the case 4Mx1 organization, one of 16 read data bus signals is transferred to the data-out buffer. In the case of 1Mx4, four of 16 data bus signals are transferred to data-out buffers. In both cases, the read data bus signals are selected by the I/O decoder. Using this function, under 10ns access time has been realized.

The RAM is fabricated using quadruple polysilicon, double metal twin-well 0.6μm CMOS process[6]. The 3.5x5.3μm high-resistance-load memory cell has stability and alpha-particle immunity. Figure 5 shows a schematic cross sectional view of the memory cell. The first polycide is used for the gate of MOSFET. The second polysilicon is self-aligned silicide and is used for the contact pad and the GND line. This layer is electrically isolated from the first polycide and is laid over the first polycide, reducing the memory cell size. The third polysilicon is for interconnection and the Vcc line. The fourth polysilicon forms the 10-tera-ohm load.

Figure 6 shows a micrograph of the memory cell after the second polysilicon formation. Figure 7 shows a chip micrograph. The die size is 8.35x18.0mm. Figure 8 shows a typical address access time of 20ns. Active current is 70mA at 40MHz. Characteristics of the RAM are summarized in Table 1.

Acknowledgment

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[4] Yoshimoto, M., et al., "A Divided Word-Line Structure in the Static RAM and its Application to a 64k Full CMOS RAM", *IEEE J. Solid-State Circuits*, Vol. SC-18, p. 479-485; Oct., 1983.

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[6] Yuzuriha, K., et al., "A New Process Technology for a 4Mb SRAM with Polysilicon Load Resistor Cell", *VLSI Symposium Technical Digest*, p. 61-62; May, 1989.

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Organization	4Mx1 / 1Mx4
Process	4 poly-Si (including 1 polycide), 2Al 0.6μm N-sub twin-well CMOS
Gate length	0.6μm (NMOS), 0.8μm (PMOS)
Gate oxide thickness	15nm
Cell size	3.5 x 5.3μm
Chip size	8.35 x 18.0mm
Supply voltage	3.3V
Address access time	20ns (normal) 9ns (fast address mode)
Active current	70mA at 40MHz
Standby current	1.5μA
Redundancy	64 columns

TABLE 1—RAM characteristics.

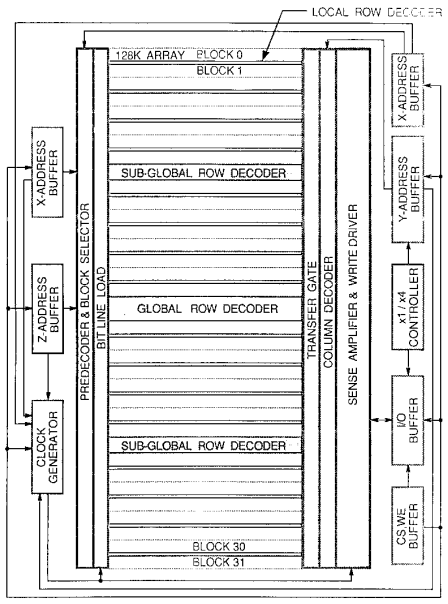

FIGURE 1—RAM block diagram.

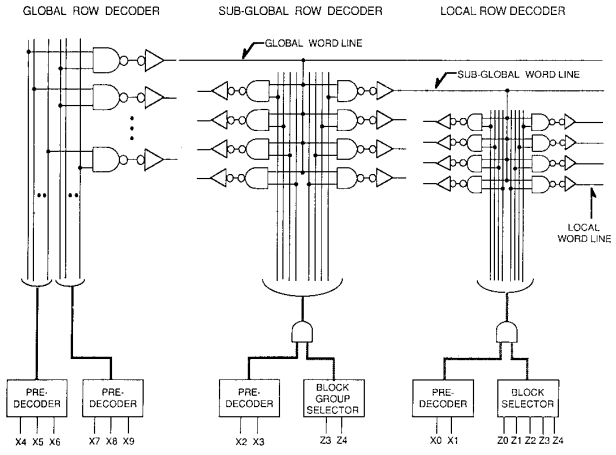

FIGURE 2—Hierarchical word decoding architecture.

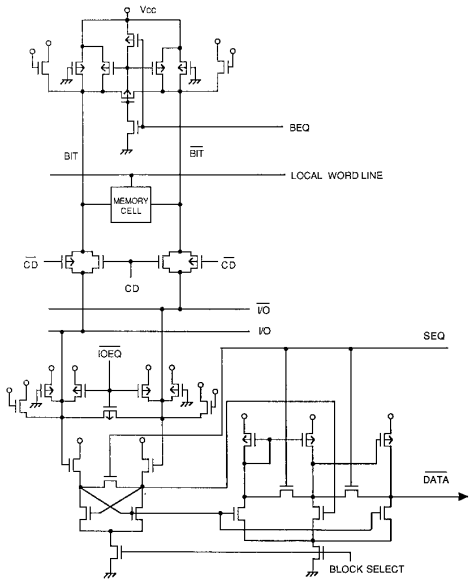

FIGURE 3—Bit line peripheral circuit.

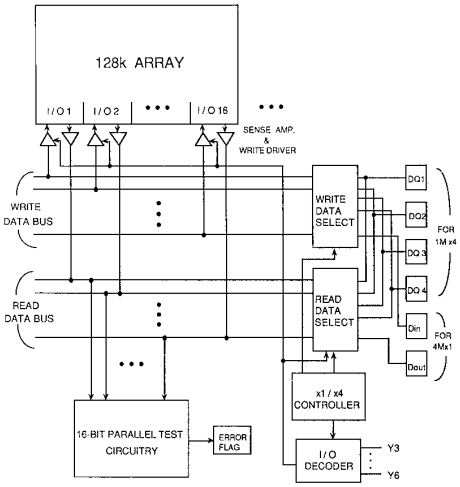

FIGURE 4—Data bus configuration.

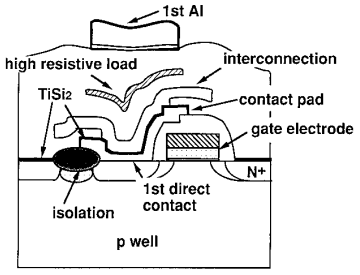

FIGURE 5—Schematic cross section view of memory cell.

FIGURES 6, 7 — *See page 281*