An Integrated Active-Quenching Circuit for Single-Photon Avalanche Diodes

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Abstract—We introduce the first integrated active quenching circuit (I-AQC) that drives an avalanche photodiode (APD) above its breakdown voltage, in order to detect single photons. Based on the I-AQC, we developed a compact and versatile photon-counting module suitable for applications in which very weak optical signals have to be detected, as for instance, photon correlation spectroscopy, luminescence measurements, and laser ranging. The prototype photon-counting module features quenching pulses up to 60 V amplitude, minimum dead time of less than 36 ns, corresponding to a saturated counting rate exceeding 25 Mcounts/s, user-controllable hold-off time, for reducing the afterpulsing effect, and nanosecond gating capability. The power dissipation is 60 mW in stand-by conditions, and the module size is less than 1 cm × 2 cm.

Index Terms—Active-quenching circuit (AQC), application specific integrated circuit (ASIC), avalanche photodiode (APD), photon detection module, photon counting, single-photon avalanche diode (SPAD), single-photon detection.

I. SINGLE-PHOTON DETECTION

SINGLE-PHOTON detection is a widely employed technique for the measurement of very faint optical signals [1]. The intensity of slow varying optical signals is obtained by the number of single photons detected during the measurement time (photon counting). The waveform of fast optical signals is achieved by collecting a histogram of the arrival time of single photons, in a time-correlated-photon-counting set up (photon timing) [1]. In recent years, significant experimental results have been obtained with photon counting and timing techniques in various fields: noninvasive testing of fast CMOS circuits [2]; luminescence microscopy [3], [4]; fluorescent decays and luminescence in physics, chemistry, biology [5]–[7]; laser diode characterization [8]; optical fiber testing in communications [9]–[11] and in sensor applications [12], [31]; laser ranging in space applications and in telemetry [13], [14]; photon correlation techniques in laser velocimetry and dynamic light scattering [15], [16]; basic quantum mechanics [17]; cryptography [18]; astronomy [19], [20]; and single molecule detection [21].

Avalanche Photodiodes (APDs) have numerous advantages when compared to other photodetectors: compactness, ruggedness and low operating voltages are distinct advantages over Photo Multiplier Tubes (PMTs) [22]; the absence of read-out noise, and the possibility of fast parallel read-out, make an array of APD more suitable than CCDs in many applications, such as adaptive optics [20]. Moreover APDs can be easily switched on and off with nanosecond transitions, which allow the detector to be gated by suitable electronics, synchronised to the optical excitation.

For single-photon detection, the APD can be operated either in the analog-multiplying regime, biased close to but below the breakdown voltage, or in the so-called Geiger-mode, above breakdown. In this paper, we will deal only with the latter regime, where a proper electronic circuit biases the APD above breakdown voltage and quickly quenches the avalanche current, as soon as a diverging multiplication process is triggered, e.g., due to the absorption of a single photon in the visible and near-infrared wavelength range [23]. In the literature, an APD operated in the Geiger-mode is known as single-photon avalanche diode (SPAD).

The duration of the SPADs avalanche current must be as short as possible for three main reasons: 1) self-heating; 2) trapping; and 3) optical cross talk. These are discussed in further detail below.

1) Excessive power dissipation leads to the heating of the diode and the shift of its breakdown voltage [24]. The latter effect causes a change in the quantum efficiency of the detector, thus introducing severe nonlinear distortion in photon counting.

2) Carriers participating to the avalanche current can be trapped near the junction and are subsequently released, thus re-triggering the APD [23]. This correlated after pulse, which causes nonlinear distortion in the counting, can be reduced by minimizing the total number of carriers crossing the junction during the avalanche, that is, its intensity and its duration.

3) Avalanche hot-carriers emit secondary photons due to Bremsstrahlung and radiative relaxations [25]. These photons can be absorbed in neighboring SPADs, thus triggering a spurious avalanche therein. Such optical cross talk is of primary importance in a monolithic array of SPADs, if a suitable optical isolation among the diodes is not employed [26], [27].

A simple way to self-limit the avalanche current is to place a high-value resistor in series to the SPAD, thus setting up a so-called passive quenching [23]. The advantage of such a configuration is that the avalanche is quickly self-quenched within a few nanoseconds, but at the expense of a slow recovery transition, in the microsecond range, due to stray capacitances [23].
Instead, when the detector is controlled by a suitable active quenching circuitry (AQC), both the quenching and reset transitions are fast, well defined and reproducible, thus leading to the improvements already reported in [23]. In order to speed up the quenching of the avalanche, the detection of the onset of the avalanche current and the quenching of the photodiode must be performed as soon as possible. Therefore, the SPAD must be mounted close to the electronics and both the comparator (which detects the avalanche ignition) and the drivers (that actually control the SPADs bias) must have propagation times of a few hundreds of picoseconds. In order to further reduce the duration of the avalanche current, we decided to adopt a mixed passive-active quenching, as reported in our previous paper in [28].

In this paper, we describe the design, the realization, and the characterization of the first integrated circuit reported in literature for driving SPADs in Geiger-mode, with high performance in terms of achievable counting rate, linearity, small dimensions, low power consumption, and general purpose use. The main goal was the integration of a large part of the electronic circuitry into one chip, the Integrated Active Quenching Circuit (I-AQC), which senses the triggering of the SPAD and provides all the controls needed for quenching the avalanche and resetting the diode to its initial conditions. Besides the I-AQC, only a few external discrete components are needed to assemble the compact stand-alone single-photon detection module herewith reported. This module can be used for all the aforementioned counting applications, thanks to the general-purpose criteria used in its design and development.

In Section II, we describe the integrated circuit and its building blocks, and in Section III we provide the guidelines for its design. Then, in Section IV, we show the whole schematic of the single-photon detection module and we describe its assembly. The experimental results are reported in Section V, where we quote the performance obtained by this module when using a commercial SPAD. Section VI deals with some perspectives on future improvement of the I-AQC, with the integration of the high-voltage switches and the application to arrays of SPADs.

II. INTEGRATED ACTIVE QUENCHING CIRCUIT

The basic blocks of the whole module are shown in Fig. 1. We used a mixed passive-active circuit configuration [28], which can be generally divided in three parts: 1) the comparator, that senses the avalanche onset; 2) the logic blocks, that generate the commands for quenching and resetting the SPAD; and 3) the high-voltage driver, that generates the actual voltage signal applied to the SPAD. The first step toward a monolithic AQC was the integration of the comparator and logic block into one chip, named I-AQC, shown in Fig. 1 within a dashed box. Since the SPAD can be biased tens of volts above breakdown, while the integrated circuit is limited to a standard single +5 V power supply, a few discrete external components are needed.

As shown in Fig. 1, the SPAD is biased at the voltage $V_{\text{high}}$ higher than the photodiode’s breakdown voltage $V_b$. The choice of the excess bias voltage, a trade off between the required quantum efficiency and the dark counting rate of the detector, dictates the choice of the excess bias voltage $V_{\text{high}} - V_b$. In fact, the overall photon detection efficiency of SPADs operated in Geiger-mode tends to saturate at an excess bias voltage of about 10% of $V_b$, while the dark counts drastically increase with the excess bias [28]. Therefore, the useful excess bias voltage ranges from a few volts for planar SPADs (with $V_b$ of about 20 V), up to some tens of volts for reach-through SPADs (with $V_b$ well above 300 V). We decided to work with excess bias ranging from 2 V to 60 V, in order to provide a module, which could be used with most of the commercial SPADs.

As soon as the detector is triggered, the high-value ballast resistor $R_b$, provides the swift passive quenching of the avalanche. The low-value sense resistor $R_s$, and the detector’s internal resistance, $R_D$, of a few hundred ohms, are negligible. The avalanche current causes the potential at the diode anode to rise, thus reducing the multiplication process itself. The rise is exponential, toward a value slightly lower than the excess bias. If the final steady-state avalanche current, given by

$$I_{\text{SPAD}} = \frac{V_{\text{high}} - V_b}{R_D + R_b + R_s} \approx \frac{V_{\text{high}} - V_b}{R_b}$$

(1)
is below a few tens of microamps, the statistical multiplication process can fail to sustain itself; thus, the avalanche eventually self-quenches and the current turns to zero. With an excess bias of 10 V, a ballast resistor $R_b$ of 220 kΩ is enough to cause the SPAD to self-quench. This is the basic principle of the passive quenching, which has two main disadvantages: 1) the process is statistical, so the time needed to quench the avalanche is uncertain and 2) after the quench, the anode potential slowly returns to zero, with a long time constant in the microsecond range, due to the high-value ballast resistor and the anode stray capacitances. The latter effect leads not only to a long dead-time between the detection of subsequent photons, but also to the possibility that the SPAD might be triggered in perturbed conditions, with a reverse voltage between $V_b$ and the nominal $V_{high}$, yielding to nonlinearity in the detection [23].

In order to avoid all the detrimental effects of passive quenching, we introduced the active feedback via the I-AQC. The SPADs signal is sensed across the resistor $R_s$ by the INPUT of the I-AQC, which consists of a fast comparator. The comparator is used both for providing an OUTPUT pulse to the external electronics, i.e., counters or time-to-amplitude converters, and for triggering an internal monostable multivibrator (namely, $M_{hold-off}$ in Fig. 1). As soon as the monostable is set (high-to-low transition), the QUENCH output buffer is enabled. Its output closes the external quench switch, $S_{quench}$, which swiftly increases the anode potential to $V_{quench}$, thus forcing the definitive quenching of the SPAD. Of course, $V_{quench}$ must be higher than the excess bias $V_{high} - V_b$.

During the hold-off time period imposed by the $M_{hold-off}$ monostable, the SPAD remains quenched and no photon can be detected. When $M_{hold-off}$ resets (low-to-high transition), the quench switch $S_{quench}$ is opened and the monostable $M_{reset}$ is triggered. The latter monostable forces the RESET output buffer to close the switch $S_{reset}$, which quickly lowers the anode potential back to ground, discharging any stray capacitance hanging at the anode. After the transition of the $M_{reset}$ monostable, the switch $S_{reset}$ is opened and the SPAD is left correctly biased in quiescent condition, ready to detect another photon.

The time taken from the ignition of the SPADs current to the subsequent return to quiescence (i.e. the anode potential at ground), is called dead-time $T_{dead}$. It is given by the sum

$$T_{dead} = T_{delay} + T_{hold-off} + T_{reset}$$

where $T_{hold-off}$ and $T_{reset}$ are the well-controlled durations of the respective monostables, and $T_{delay}$ is the propagation delay between the ignition of the avalanche current in the SPAD and the closure of $S_{quench}$. The latter contribution depends on: 1) the stray load at the detector’s anode (some picofarads, depending on the device and the connections); 2) the capacitance of the input stage of the I-AQC, well below 1 pF; 3) the comparator commutation time; 4) the propagation times of the QUENCH monostable and of the driver; and 5) the speed of the switch $S_{quench}$ employed. In the design, we devoted particular care to reduce all the delays internal to the I-AQC, and in the assembly we kept the SPAD close to the I-AQC.

For the clarity of the presentation, Fig. 2 shows the SPICE simulation of the whole I-AQC with the external components that will be discussed in detail in the next Section IV. The SPAD used both in the circuit simulations and in the experimental set-up is a super low ionization $k$ (SLIK™) APD by EG&G Optoelectronics, Canada [29], with a breakdown voltage $V_b = 390$ V, an internal series resistance $R_D$ of 480 Ω, and a total device capacitance of 2 pF. The stray capacitance between anode and ground is 2 pF, according to the measurements performed in our lab. We used $V_{high} = 400$ V and $V_{quench} = 24$ V, $R_b = 220$ kΩ and $R_s = 4.7$ kΩ.

In SPICE, we modeled the SPAD as a series connection of a voltage source $V_b$, a series resistance $R_D$, and a voltage-controlled switch that closes when a photon is absorbed and opens when the voltage across the model becomes smaller than $V_b$. Moreover, two stray capacitances were added: the total device capacitance across the model and the stray capacitance between anode and ground.

At rest, the detector’s anode is at 0 V, i.e. the SPAD is reversed bias 10 V above breakdown. At $t = 5$ ns, a photon is absorbed and triggers the avalanche current that swiftly rises to about

$$I_{peak} = \frac{V_{high} - V_b}{R_D} = 20.8 \text{ mA}$$

since the stray and device capacitances force the 10 V-excess bias across the SPAD. This value is confirmed by the simulation in Fig. 2(b). Then the capacitances discharge, with a time constant given by $\tau = (2 \text{ pF} + 2 \text{ pF}) \cdot R_D \approx 1.7$ ns. The voltage drop across $R_b + R_s$ increases, as shown in Fig. 2(a), in the range 5–20 ns. After about $6 \cdot \tau \approx 10$ ns the exponential transition is almost over and the SPADs steady-state cur-
Fig. 3. Responses of the circuit with a SPAD biased (a) 5 V, (b) 10 V, (c) 15 V, and (d) 25 V above breakdown and $V_{\text{breakdown}} = 29$ V. The anode potential is shown together with QUENCH and RESET outputs.

Fig. 4. Response of the circuit in gated mode: only when the gate input is low, the SPAD can detect photons (the anode potential shows the typical transitions), otherwise the detector is held off (the anode potential is kept at $V_{\text{breakdown}} = 29$ V).

rent is $I_{\text{SPAD}} = 45 \mu$A; the avalanche current could passively self-quench.

In the meantime, the comparator was triggered and set the monostable $M_{\text{hold-off}}$ that, finally, at $t \approx 18$ ns closes $S_{\text{quench}}$ causing the anode potential to rise up to $V_{\text{quench}} = 24$ V. The SPAD is definitively quenched, since it is biased at a reverse voltage $V_{\text{high}} - V_{\text{quench}} = 376$ V, lower than its 390 V breakdown voltage. The active quenching remains set as long as the duration of the hold-off monostable (20 ns in Fig. 2(a), from about 18 ns to 38 ns). Then the reset switch is closed and the anode potential returns to zero, within 8 ns.

Note that as long as $S_{\text{reset}}$ is closed, the SPAD can be triggered, since the bias voltage is increased above the breakdown [after about 40 ns in Fig. 2(a)], but the I-AQC cannot detect the current. In fact, the avalanche current bypasses the I-AQC by flowing through $S_{\text{reset}}$. For this reason, the pulse duration of $M_{\text{reset}}$ must be set with accuracy: it should be as short as possible in order to avoid avalanche triggering, but long enough to ensure complete restoration of the SPAD voltage.

It is worth stressing that the active quenching can happen slightly before or after the completion of the passive quenching of the SPAD, depending on the time constants and delays introduced in the circuit. In every case, the active loop drives the voltage across the SPAD down to $V_{\text{high}} - V_{\text{quench}}$, a level lower than the nominal breakdown voltage $V_b$ by a few volts, thus avoiding re-ignition due to nonuniformity of $V_b$ over the detector active area [29]. Fig. 3 shows the detector’s anode voltage waveform at a different excess bias. As can be seen,
with low excess bias, the passive quenching is almost over when the active quenching pulse is applied to the SPAD at about 22 ns [Fig. 3(a)]. This is because the low signal sensed at the I-AQC's INPUT causes a slow triggering of the comparator. Conversely, at high excess bias the active quenching is compulsory for switching off the SPADs current (see Fig. 3(d), at 20 ns and Fig. 4).

The nand gate in Fig. 1 was introduced to operate the detection module in the so-called gated mode. When the GATE input is enabled (low level, 0 V), the I-AQC behaves as described above and the SPAD can detect photons. Instead, when the GATE input is disabled (high level, +5 V) the QUENCH output is set and is closed, thus keeping the detector biased below breakdown: no photon can be detected.

III. DESIGN GUIDELINES

In order not to limit the design of the I-AQC to a specific fabrication technology, we decided to use a general-purpose CMOS process. Even if the I-AQC operation is mainly analog, we adopted a more standard digital 1 µm-CMOS single-polysilicon, double-metal process by ES2 [30]. Since this technology withstands a maximum operating voltage of 6 V, we had to leave a few discrete components outside the I-AQC, dealing with the higher voltage of the quenching bias, \( V_{\text{quench}} \).

The comparator is the critical block of the whole I-AQC. It must sense the triggering of the avalanche with a low threshold, and it must load the sensing node with the smallest parasitic capacitance. Since the sensing resistance \( R_s \) that feeds the comparator is of the order of a few kΩ, a stray capacitance of 1 pF would be enough to introduce a 1 ns-time constant, comparable to the rise time of the avalanche current. We designed a simple p-MOS differential stage, with a threshold adjustable by the external THRESHOLD pin. The propagation delay obtained from the simulations was 300 ps. The partition between \( R_b \) and \( R_e \) can be changed for increasing the comparator overdrive, i.e. its speed, but higher \( R_e \) leads to longer time constants. A trade off must be found, depending also on the stray capacitances of the printed circuit board and the SPAD.

The three monostables have two pins each for connecting an external resistor, in order to customly set the respective pulse duration: from 100 Ω to 100 kΩ, the duration spans from nanoseconds to a few microseconds. In this way, the hold-off duration can be shortened (for very high counting rates) or increased (if the afterpulsing effect needs to be reduced [24]). Finally, the width of the OUTPUT pulse can be chosen according to the requirements of the electronics fed by the I-AQC.

After having been triggered, each monostable is insensitive to any other pulse applied to its input, as long as the output is active, i.e. until the capacitor is discharged. If the duration of the input pulse is longer than the duration of the output pulse, the monostable cannot be triggered until the input returns to the quiescence state (high). In this way, any re-triggering of the monostables is avoided. Fig. 5 shows the schematic of one monostable. Note the internal 3 pF capacitor, the external resistor, and the n-channel MOS transistor in parallel to the capacitor, in order to speed up its discharge during the reset transition.

The output buffers for QUENCH and RESET must be designed to carry sufficient currents for driving the external switches that, as will be discussed in the next section, are made with power DMOS transistors. The OUTPUT buffer was designed to stand the capacitive load of a one-meter coaxial cable.

The whole I-AQC has only 82 MOS transistors. The dimensions of the bare chip are 1.1 mm × 1.4 mm, mostly occupied by the pads and the three 3-pF capacitors internal to each monostable, as shown in Fig. 6. The chip was not optimized for a reduced area occupation, because at this stage the size of the detection module is limited by the external components. The integrated circuit needs a single +5 V power supply and has a quiescent power dissipation of 60 mW.
IV. THE DETECTION MODULE

Besides the I-AQC discussed in the previous sections, a few other external components are needed for the detection module, as shown in Fig. 7. In Fig. 7(a), all the switches are discrete n-channel DMOS transistors (model SST-215 by Siliconix) with low parasitic capacitances, commonly used for high-voltage/high-speed applications. Their electrical characteristics are: 1 V-threshold voltage, 40 mA-maximum drain current, and 40 V-maximum drain-source voltage. For the switch, instead of using only one p-channel MOS, we preferred to use two n-channel DMOS transistors, due to their better speed of response. In this way, since the DMOS2 is closed when a low TTL-level is applied to the gate of DMOS3, we used the inverted signal of the QUENCH output, named, already present in the I-AQC shown in Fig. 1.

Instead, the RESET DMOS1 behaves as a closed switch when a high TTL-level is applied to its gate, as described in Section II. In order to keep DMOS2 in its triode region of operation, when in conduction, we introduced a bootstrap capacitor and a blocking diode. When the circuit is in the quiescent state, the capacitor charges up to about 11 V (12 V minus the 0.5 V drops across each of the two Schottky diodes). When becomes active (low TTL-level, 0 V), the bias of the gate of DMOS2 rises, thus turning DMOS2 in conduction and bootstrapping the potential at its gate. Due to this behavior, when the DMOS2 is closed, its source is at and its gate is about 11 V higher. Since the same voltage is applied to the drain of DMOS3, it turns out that the absolute rating of the SST-215 DMOS limits the maximum to 40 – 11 = 29 V. The maximum excess bias must be accordingly limited to below 29 V.

Higher excess bias can be easily attained with other DMOS transistors or by eliminating the bootstrapping. For instance, in Fig. 7(b) we used two discrete n-channel DMOS' and a p-channel power MOS by STMicroelectronics with maximum drain-source rating of 60 V. With this solution we built a compact detection module that operated the SPAD 60 V above its breakdown voltage of 390 V.

This is to stress that the limitation to the high-voltage side is due only to the discrete transistors used as switches and not to the I-AQC. It is worth noting that also in Fig. 7(b), the p-channel MOS is driven by an n-channel transistor, via the QUENCH control.

In both Fig. 7(a) and (b), the Schottky diode HP2800 is slightly forward biased in order to stop the avalanche current from flowing toward DMOS2, during the avalanche ignition.

We assembled the I-AQC and the external surface mounting devices of Fig. 7(a), as shown in Fig. 8 in a compact module of 1 cm × 2 cm, in close proximity to the SPAD. We performed an extensive characterization of the detection module with commercial detectors. The results proved to be in very good agreement with the simulations.

The current consumption of the I-AQC is 12mA at steady state. The peak in the current supplied by is due to the transitory cross conduction through DMOS2 and DMOS1. Finally, the +12 V power supply sources the quiescent 10 mA current to the pull-down transistor DMOS3 that keeps DMOS2 open. Only during the hold-off period is this current nil.

V. EXPERIMENTAL RESULTS

We have tested the module with the SLIK (detector biased at , i.e. 20 V above breakdown, and ). Fig. 9 shows the results. The detector was illuminated with a high light level, as can be seen from the frequent ignitions occurring after the first avalanche, as soon as the detector is reset. The hold-off time was reduced to about 10 ns, for a total dead time of 40 ns. The corresponding maximum counting rate is 25 MHz.
We have measured the dark-counting rate of the detector at various voltages, ranging from 0 up to 20 V above breakdown. The results are shown in Fig. 10. For this SPAD, with a very high breakdown voltage, the increase of the dark counts appears almost linear. We verified with other SPADs that the increase can be more abrupt, and dark counting can increase exponentially above a few volts of excess bias. In that case it will be necessary to limit the operating voltage in order to reduce these unwanted ignitions.

In order to assess the presence of trapping effects in the detector under test and to prove the adjustability of the module hold-off time, we performed the set of measurements reported in Fig. 11. The SLIK™ detector was illuminated at a constant light level and the I-AQC hold-off time was varied from 10 ns to 8 µs. The flatness of the counting rate is clear evidence that the detector is not affected by significant afterpulsing [24].

We decided to modify the module, by adopting the switches shown in Fig. 7(b). We operated the SLIK™ at $V_{\text{high}} = +430$ V, i.e. 40 V excess bias, with $V_{\text{q}} = +45$ V. Fig. 12 shows the anode potential when the SPAD is operated in the dark. The hold-off duration was deliberately increased, for a total dead time of about 75 ns.

As a final test, we operated the module with the switches shown in Fig. 7(b) and a quenching voltage $V_{\text{q}}$ of 65 V. Fig. 13 shows that the active quenching and reset transitions at the SPAD anode are performed within 50 ns. Even with these extreme conditions, the module proved to be reliable and performing.

VI. CONCLUSIONS AND PERSPECTIVES

We have reported the design and characterization of a compact detection module based on the first I–AQC reported in literature and with few external components. With the DMOS transistors that we used, this module can drive avalanche photodiodes up to 60 V above their breakdown voltage, with a minimum dead time of 40 ns, corresponding to a maximum measured counting rate of 25 MHz. This module proved to be reliable and easy to operate.
Fig. 13. Measurement of the active quench and active reset transitions at 60 V of excess bias and $\tau_{\text{ramp}} = 46.5$ V. The dead time is about 45 ns.

Studies aiming at a complete monolithic integrated circuit, which would include the analog comparator, the control logic and the switches, are in progress: remarkable problems have to be solved, mainly concerning the technological compatibility between high-voltage components and low-voltage logic circuitry. The goal will be the use of such integrated chips in linear and matrix arrays of planar APDs [26].

REFERENCES


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