Department of Electrical Enginering
Columbia University
EE 3082. Digital Electronics Lab

Laboratory 1. Basic Digital Circuit Elements

Note You will receive a "box" from the laboratory manager containing a breadboard and a set of working chips that you will use for the projects through the end of the semester. Please store your board in the cabinet in the back of Mudd 1227 between lab sessions. This will allow you to "save" your breadboard wiring between lab sessions if you wish.

Introduction: Digital circuits can be built in different technology, diode-transistor logic (DTL), transistor-transistor logic (TTL), emitter-coupled logic (ECL), and CMOS. In addition, digital chips are often characterized by the degree of integration. SSI (small-scale integration) chips often consist of single gates or registers. MSI (medium-scale integration) chips would include larger functions such as counters or decoders. VLSI (very large scale integration) chips are now used to characterize designs with up to hundreds of millions of transistors. In modern VLSI chips, digital circuits are implemented (almost) exclusively with CMOS logic, which can be scaled in current technologies to geometries as small as 65 nm, and operate internally with supply voltages as low as 900 mV. External interfaces commonly operate at 5 V, 3.3 V, or 2.5 V. SSI and MSI chips, to maintain historical consistency, are either TTL or CMOS, operating at 5 V. Standard TTL chips were first introduced in 1965. Common TTL families are the 74F, 74ALS, and 74LS, all originally introduced in the 1980's.

5V TTL chips of the 74F family have the characteristics shown below which are fairly typical of TTL SSI and MSI chips.

Min V_{OH}/Max V_{OL}	2.7 V/0.5 V
Min V_{IH}/Max V_{IL}	2.0 V/0.8 V
Min I_{OH}/Min I_{OL}	-1.0 mA/20 mA
Max I_{IH}/Max I_{IL}	20 μA/-0.6 mA
Typical propagation delay time	2.5 nsec
Typical power dissipation per gate	4 mW

Because of the logic levels, 5V TTL logic is immediately compatible with 3.3V CMOS logic levels, which are sometimes referred to as "TTL logic levels" (that is, one can drive TTL gates from 3.3 V CMOS chips or drive 3.3 V CMOS chips from TTL chips without any special interfacing issues). When interfacing 5 V CMOS logic to TTL, a simple direct connection can be used. The CMOS driver must have a strong enough pull down to sink I_{IL} when the input to the TTL gate is low (~ 0.5 V). Similarly, the CMOS driver must have a strong enough pull up to source I_{IH} when the input to the TTL gate is high (~ 2.7 V). When interfacing the other way (from TTL to 5 V CMOS logic), a pull-up resistor (~ 10 kΩ) is generally used to give higher output high voltage levels as shown below.

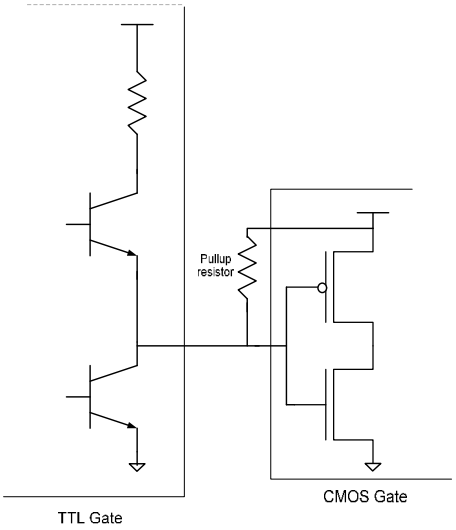

Figure 1. Interface between a TTL gate and a 5-V CMOS gate.

5V CMOS SSI/MSI logic families include the 74HC/HCT, 74AC/ACT, and 74VHC/VHCT families.

Goals:

1. To understand the basic voltage transfer characteristics of SSI/MSI TTL and CMOS digital logic gates and how these determine the logic levels and noise margins for digital logic gates.
2. To measure the propagation delays for SSI/MSI TTL and CMOS digital logic gates.
3. To build a basic RS latch structure from TTL SSI gates and use this RS latch to construct a switch debouncer.
4. Leveraging MSI components, design simple frequency dividers and counter circuits.

P We will first study the transfer characteristic of a TTL-NAND gate using the 74F00 parts. Connect one input of the NAND gate to 5 V and the other input to a triangular wave between 0 and 5 V. Please refer to the datasheets which are available on the EE E3082 website for information on the pin-outs of the 74F00 DIP (dual inline package).

Q1 Record the dc transfer characteristic (V_{out} as a function of V_{in}) using the X-Y capability on the scope. To do this, you will use the Agilent IntuiLink software installed on the lab computers; the TA or lab assistant will show you how to use this. Determine V_{IH}, V_{IL}, V_{OH}, V_{OL}, and the magnitude of the worst-case static noise margins NM_H and NM_L. Do you expect that these values will change with output load capacitance? Explain.

Q2 Applying a 1 MHz square wave to the gate, determine t_{pLH} and t_{pHL} for 66 pF of

output load. Repeat for 0.1 μF of output load. Record the waveforms from the oscilloscope for your lab report.

Q3, Q4 Repeat Q1 and Q2 using the CMOS 74HC00 parts.

Let us consider some circuits using 74F74 positive-edge-triggered flip-flops.

Q5 Construct the circuit shown in Fig. 2. Driving the input with a 5 V peak-to-peak square wave of 1 kHz, what is the frequency of the output signal relative to the input signal? Keep increasing the input signal frequency. What is the maximum frequency of operation of the circuit? Record appropriate oscilloscope traces for your lab report.

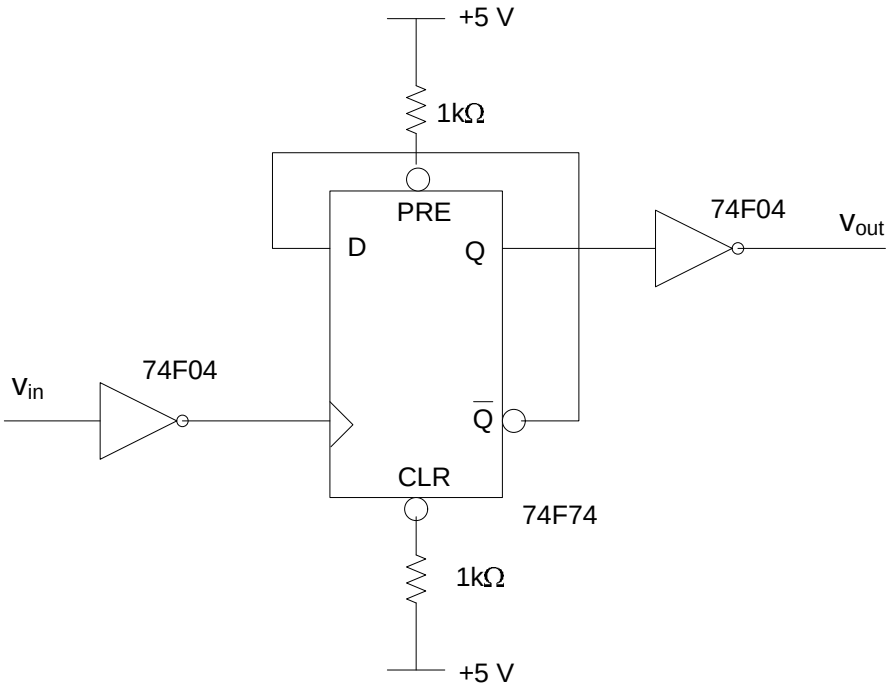

Figure 2. Frequency divider circuit.

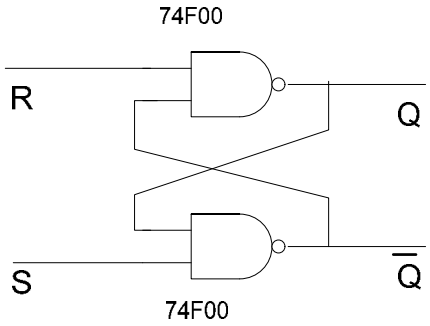

Figure 3. RS latch

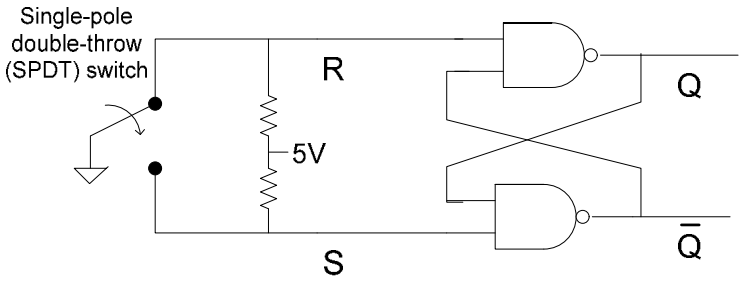

Figure 4. Switch debouncer

P Construct the RS latch of Fig. 3 from 74F00 NAND gates. A common application of this circuit is in the switch debouncer circuit shown in Fig. 4.

Q6 Construct and measure the behavior of the switch debouncer and explain how it operates. To understand how the circuit works, make sure you look at the voltages on R, S, and Q in the oscilloscope. Include your oscilloscope traces in your lab report.

D Using HCF4511B, 74AC161, and 74F04 chips (data sheets for these chips are available on the EE E3082 website), design a circuit that counts from 0-9 and then restarts from 0, displaying the results on the seven-segment LED (NKR141). Trigger the count from a debounced switch input. Don't forget to use resistors in series with all your LEDs; there is a chip in your kit that contains 8 individual resistors. *Please have the TA check your design and sign-off on your lab sheet, which you should include with your lab report.*