

Department of Electrical Engineering
Columbia University
EE 3082. Digital Electronics Lab

Lab 6. Electric piano design using Xilinx FPGAs, Part II

1 Programming the FPGA

As FPGAs store their configuration bits in SRAM, they lose their configuration after every power cycle. To allow for persistent configuration, the FPGA is programmed at power up by non-volatile memory. Our board includes a Serial FLASH device for this purpose.

The PROM and FPGA are wired together in a boundary scan chain, more commonly called the JTAG. To implement your design you may either program the flash device or the FPGA. While debugging your device it is best to just program the FPGA because it is faster (takes around 5 seconds). Once you have debugged the design you can program (or "burn") it into the flash device (takes around 1-2 minutes) by creating a **.MCS** file.

Board Setup

The required jumper settings are:

- Jumper JP2 installed on USB position. This means that power will be provided through the micro USB cable
- Jumper JP1 installed in **JTAG** if programming the FPGA, or **QSPI** if programming the flash memory.

Refer to the figure 4 at the end of the handout for jumper positions

Synthesis and Implementation

After you have verified your design by running simulation, continue on with the rest of the *design flow*. Click Run Synthesis under the Synthesis tab, and upon its completion, click Run Implementation under the Implementation tab. You do not have to change any setting for this lab.

, For more details on Synthesis and Implementation, refer to:

- [Synthesis User Guide](#)
- [Implementation User Guide](#)

Programming the FPGA

Before proceeding, check your JP1 jumper position.

To program the FPGA, you need to generate a .bit file by clicking **Generate Bitstream** under **Program and Debug** tab. Next,

1. Expand Hardware Manager tab under Program and Debug tab, and click Open New Target. Next
2. Connect your FPGA to the computer. Select local server. Next
3. Your devices should be automatically detected. Next, Finish
4. Finally, click Program Device under Hardware Manager tab. Select the *.bit file you generated. Program

All of the outlined procedure above can be executed from inside the red box in lower left corner of Figure 1.

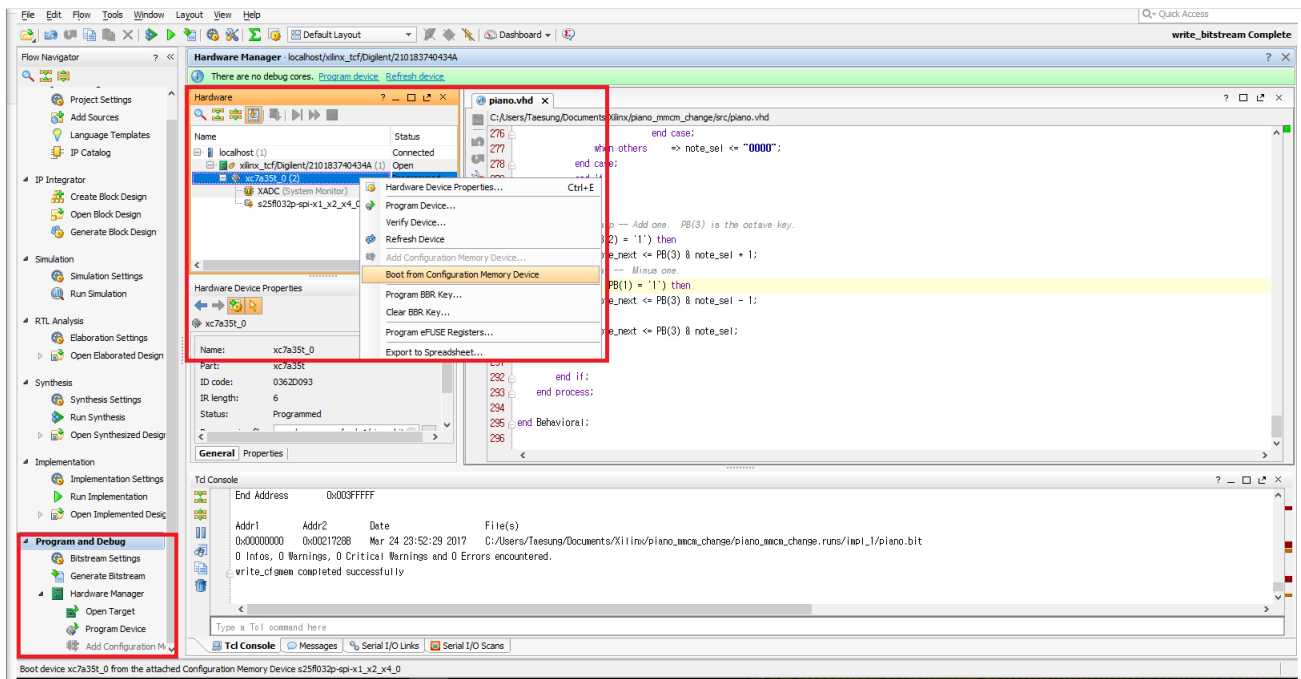


Figure 1.

Programming the Flash Device

Before proceeding, check your JP1 jumper position.

After verifying that the FPGA operates as intended, you are in good shape to program your design in flash device. To do so,

1. Go to Tools $\rightarrow$ Generate Memory Configuration File from top menu bar. There are several things to configure in the next window. Please refer to Figure 2.

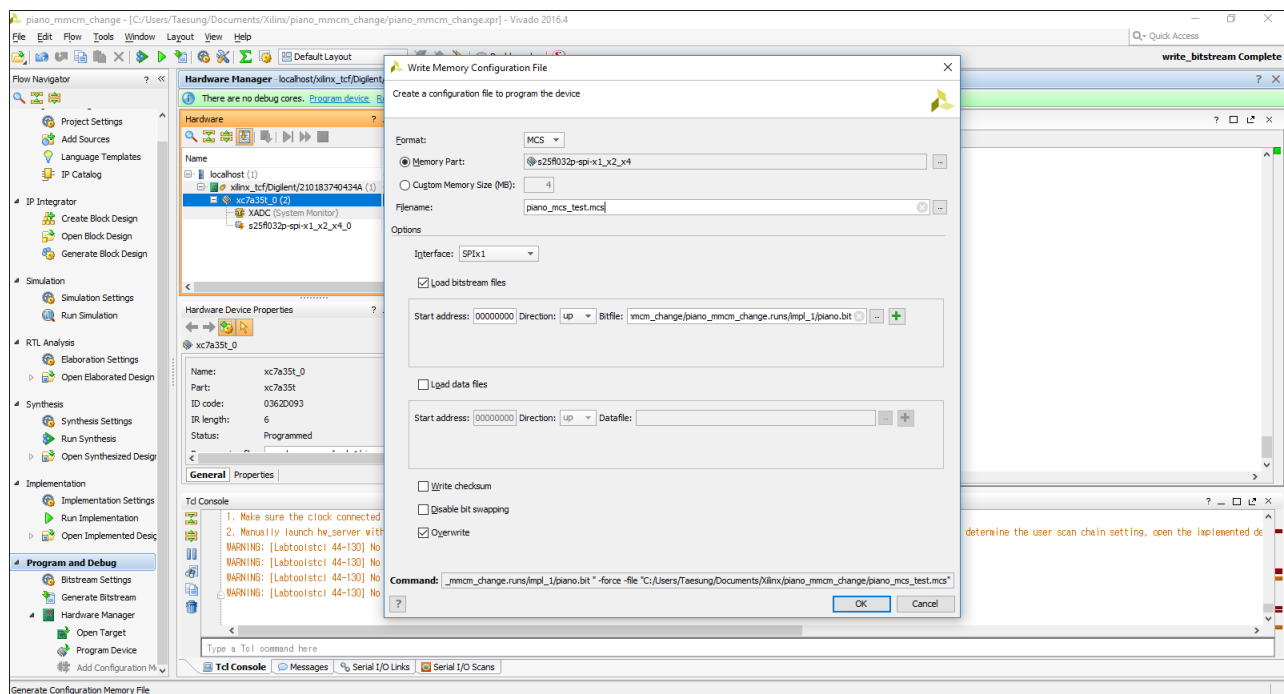


Figure 2.

2. Select Format: MCS. Select Find Memory Part by searching S25FL032, which is the part number of Spansion flash memory on Basys 3 board. Give an appropriate file name inside an appropriate directory. Set Interface: SPIx1, where x1 is the programming speed of S25FL032. Check "Load bitstream files" and locate your .bit file in "Bitfile" tab
3. Click OK to generate your .MCS file
4. Refer to the top red box in Figure 1. Right click "s25fl023p-spi-..." and click Program Configuration Memory Device
5. Locate your .MCS file and click OK to program your flash device. Refer to Figure 3.
6. Right click "xc7a35t_0" and click "Boot from Configuration Memory Device"

2 Testing

Now you can actually check the functionality of your piano against a tone generator.

There are plenty of online tone generators out there which you can utilize. Here is [one](#) as an example. Please recall that 440Hz corresponds to the note A4. If your speaker sounds flat/sharp, there may be an off-by-one error in the counter.

D Modify your user interface to support automatically playing a short song of your choosing (converter your design into a "player" piano). Be creative. Simulate and synthesize your design. Demonstrate your design to the instructor or TA.

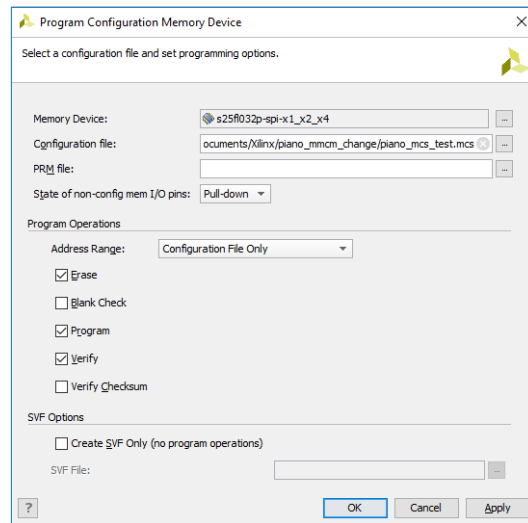


Figure 3.

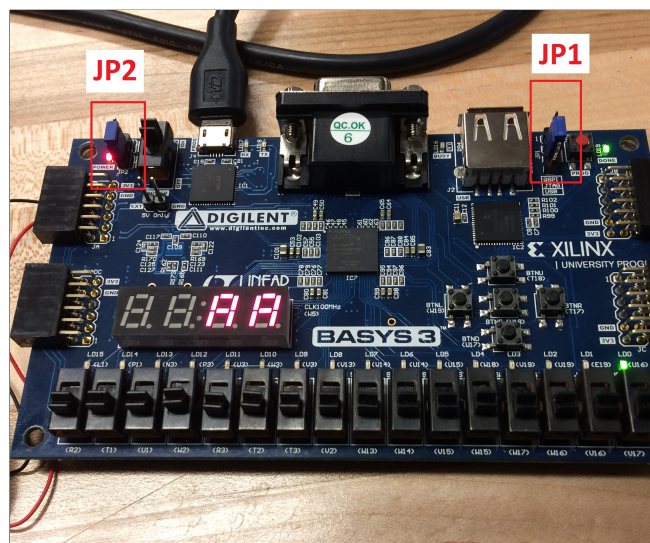


Figure 4.